A Spectroscopic Baseband Processor for CSMC with 5μV DAC Precision and 1μV BGR Noise

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Abstract*—Chip-scale molecular clock (CSMC) is an "atomic clock" grade, low-cost time-base for wireless and navigation. Its frequency servo-control demands a baseband processor, including a low-noise, high-precision analog voltage generator and a digital spectroscopic demodulator. This work presents the first baseband processor SoC for CSMC. The digital part integrates a wavelength modulation spectroscopy (WMS) demodulator, a programmable PID controller, a temperature compensation unit with lookup-table and linear interpolation, and a disciplining module with Kalman filtering. To eliminate flicker noise, a current-mode bandgap reference (BGR) with dual-chopping is employed. Besides chopping the Op-amp at 1kHz, the BGR core and output current mirror are also chopped, which effectively improves the accuracy of current duplication. A 16-bit resistive DAC, buffered by a 3.0V low-dropout regulator (LDO), functions as the voltage generator. The DAC adopts a segmented R-2R ladder scheme, with 63-bit thermal code and 10-bit binary code. To reduce the temperature drift, each resistor of DAC consists of a rppolywo and a rnwsti resistor with opposite temperature coefficient. Next, a 3rd-order, 15-bit delta-sigma modulator (DSM) is employed to achieve μV grade voltage resolution. Fabricated in 65nm CMOS process, the BGR achieves a measured noise density of 512 nV/√Hz at 1 Hz and 1.164 μV integrated noise (0.1-10 Hz). The DAC achieves a precision of 5 μV within the 1 mV tuning range required for the locking of CSMC. The proposed baseband processor meets all CSMC locking requirements with fully on-chip baseband processing, representing a system-level integration breakthrough for portable atomic-grade clocks.

Keywords—chip-scale molecular clocks (CSMC), bandgap reference (BGR), digital-to-analog converter (DAC), Delta-Sigma Modulator (DSM), low noise

I. INTRODUCTION

The growing demand for precise timing in wireless communications and distributed sensor networks is driving research into compact, high-stability frequency sources. Chip-scale molecular clock (CSMC) have emerged as a promising alternative to atomic clocks, particularly for applications requiring rapid startup and robust long-term stability [1].

As shown in Fig. 1, the CSMC follows a closed-loop frequency-servo control principle. A voltage-controlled crystal oscillator (VCXO) generates the base frequency, which is multiplied to the millimeter-wave range and directed into an OCS gas cell. Molecular absorption produces a characteristic dip at the resonant frequency. This signal is received, down-converted, and digitized by an external high-precision analog digital converter (ADC). The mixed-signal baseband SoC then performs digital demodulation (FM or FSK) to extract a frequency error signal. A digital Proportional-Integral-Derivative (PID) controller calculates the required correction, which is converted to an analog tuning voltage by an on-chip high-resolution digital analog converter (DAC). This voltage is

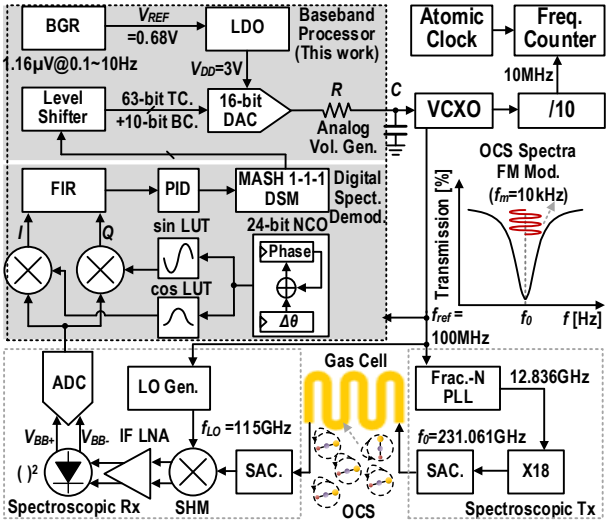


Fig. 1. Architecture of the baseband processor chip for CSMC.

applied to the VCXO, completing the feedback loop and disciplining its output to the invariant molecular transition.

This paper presents a fully-integrated CSMC baseband chip implemented in 65nm CMOS. The digital spectroscopic demodulator implements FM demodulation and configurable PID control. The key innovation in analog voltage generator is a current-mode BGR with dual-chopping. In addition to chopping the operational amplifier at 1 kHz, the BGR core and output current mirror are also chopped, which likewise enhances the accuracy of current duplication. Because of this, BGR achieves a measured noise density of 512 nV/$\sqrt{\text{Hz}}$ at 1 Hz. Analog voltage generator also integrates a 16-bit resistor ladder (R-2R) DAC with a segmented 6-bit thermometer-coded plus 10-bit binary-weighted architecture. A delta-sigma modulator (DSM) enhances the effective resolution of the DAC. Measurement results show the implemented DAC achieves a precision of 5 μV within the 1 mV tuning range required for molecular clock locking.

II. SPECIFICATION OF BASEBAND PROCESSOR OF CSMC

The core functionality of a CSMC relies on a baseband system-on-chip (SoC) to generate an ultra-low-noise analog control voltage that disciplines a VCXO against a molecular absorption reference. The spectral purity and long-term stability of the final output are fundamentally limited by the noise and drift of this control voltage, imposing stringent specifications on the baseband chip's analog core, specifically its BGR and DAC.

The target CSMC system specifications directly determine the required performance of the baseband chip. The VCXO output frequency is 100 MHz, with a frequency tuning sensitivity $k_c = 1\times10^{-5}$ Hz/V . The loop bandwidth

f_{BW} covers 0.1Hz to 10kHz. The operating temperature range is -40 to 80°C.

The DAC is employed to generate the tuning voltage for the VCXO. Accordingly, its output range is set to 0–3V to cover the full control range of the VCXO. The target frequency stability of the molecular clock is 10^{-10}, and the VCXO pullability is 10^{-5} Hz/V. To achieve this stability, the required voltage precision of the DAC is calculated to be 10 μV. The noise requirement is derived from the molecular clock phase noise specification through the noise transfer function of the loop, leading to an integrated noise constraint of $\leqslant$ 40μV over 0.1-10 Hz. The temperature drift requirement is obtained by analyzing the relationship between DAC output drift and long-term frequency stability, resulting in a drift limit of $\leqslant 1\times10^{-4}$ V/°C. These four key specifications are summarized in Table I.

These derived specifications—particularly the noise and temperature drift requirements—form the design targets for the BGR and DAC presented in this work.

TABLE I. SPECIFICATION OF THE BASEBAND PROCESSOR.

Constraint	Specification	This Work
Full-scale Range	0-3V	0-3V
Voltage Precision	≤ 10μV	5μV
Integrated Noise @0.1Hz-10Hz	≤ 40μV	10μV
Temperature Drift	≤ 66.7ppm/°C	16.68ppm/°C

III. BASEBAND CIRCUIT IMPLEMENTATION

A. Low Noise Bandgap Reference (BGR)

The bandgap reference presents a critical bottleneck in the analog signal chain. Conventional BGRs exhibit flicker noise on the order of several tens of $\mu V/\sqrt{Hz}$, which directly couples into the DAC output. This noise modulates the VCXO tuning voltage, degrading output phase noise and limiting achievable frequency stability. While 16-bit DAC architectures are well-established, their effective resolution and temperature drift are ultimately bounded by the purity of the reference voltage.

When no noise cancellation techniques are applied, the op-amp constitutes the dominant noise source. Chopping the op-amp is a well-established technique to mitigate its low-frequency noise. However, after applying op-amp chopping, the current mirror transistors—M1, M2, M3, and M4—become the primary noise contributors. Their flicker noise directly corrupts the mirrored current.

To address this, a current-mode bandgap reference incorporating a current-mirror noise cancellation technique is proposed. As illustrated in Fig. 2, a chopper is inserted at the drain nodes of the cascode transistors within the current mirror. The design employs two 1:1 current replication branches with matched load resistance, ensuring the chopper does not disturb the DC operating point. The chopper up-modulates the low-frequency noise of the current mirror devices to higher frequencies, where it is filtered.

Following op-amp chopping alone, approximately 97% of the remaining low-frequency noise originates from the current mirror transistors. After applying the proposed current-mirror chopping, this contribution is reduced to only 3% of its original value.

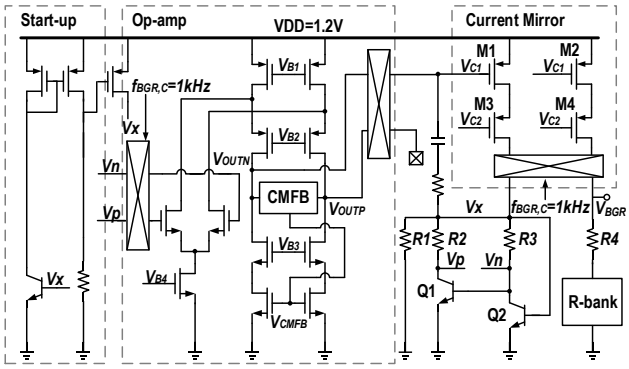


Fig. 2. Schematic of the proposed BGR.

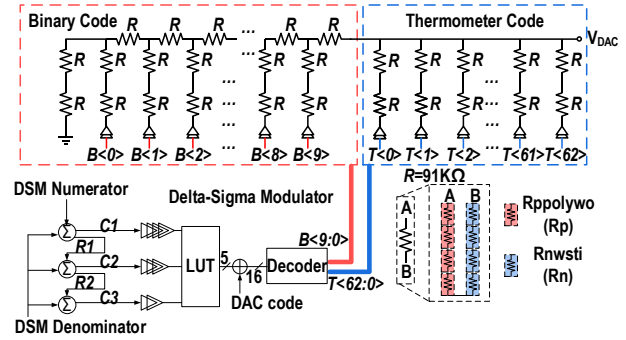
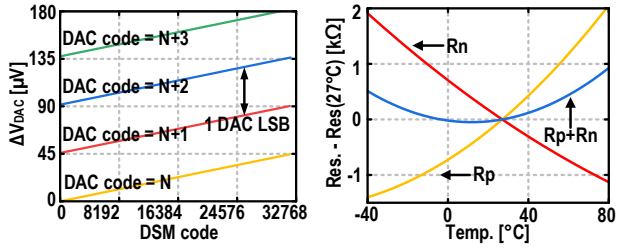


Fig. 3. Schematic of the proposed 16-bit R-2R DAC with DSM.



(a) (b)

Fig. 4. Simulated (a) ΔV_{DAC} controlled by DSM (b) The resistance values of rppolywo, rnwsti, and their series combination.

B. 16bit R-2R DAC with DSM

The 16-bit R-2R DAC converts the digital frequency control word into an analog tuning voltage. Linearity is addressed through a segmented architecture: the 16-bit input code is partitioned into 6 thermometer-coded MSBs (controlling 63 switches) and 10 binary-weighted LSBs, as shown in Fig. 3, minimizing mismatch effect [2]. To minimize temperature drift, the unit resistors in the R-2R ladder are implemented as series positive-temperature-coefficient and negative-temperature-coefficient resistors.

To achieve finer frequency resolution, a DSM is employed. The digital PID controller outputs a 16-bit integer part and a 15-bit fractional part. The integer part is applied directly to the core R-2R DAC, while the fractional part is fed into the DSM. The DSM generates a high-speed dithered output toggling between adjacent integer DAC codes, such that its time-averaged value equals the desired fractional value. This pushes quantization noise to higher frequencies, where it is subsequently filtered by an off-chip low-pass filter placed after the DAC output, effectively enhancing the resolution of the tuning voltage, as shown in Fig. 4(a).

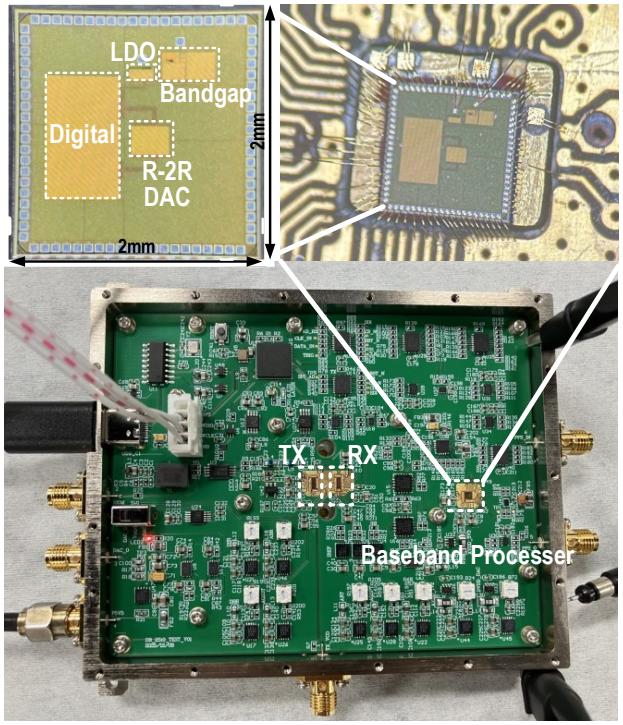


Fig. 5. Die photo and packaging of the 65nm CMOS baseband processor.

C. Digital Spectroscopic Demodulator

The digital baseband processor performs real-time spectroscopic demodulation, servo control, temperature compensation, and clock disciplining for the CSMC. The FM demodulator supports 1st-, 3rd-, and 5th-order wavelength modulation spectroscopy (WMS) using three independent NCOs to generate quadrature references, followed by programmable FIR filters to extract in-phase and quadrature error signals. A digital PID controller with six independently programmable PI coefficient pairs (for the three demodulation orders) processes these error signals and produces a 16-bit integer part and a 15-bit fractional part control word, which is fed to the delta-sigma modulator (DSM) for high-resolution DAC driving.

The temperature compensation unit employs a 1 °C-step lookup table with 121 entries to correct both system-level frequency drift and DAC drift. The disciplining module accepts an external 1 PPS input, performs coarse time-difference measurement with the 100 MHz system clock, and executes a Kalman filter followed by a PID-based steering law, outputting a fine tuning word and generating a TRIG signal for MCU readout; it also supports holdover when the 1 PPS is temporarily lost. The entire digital core operates at 100 MHz and interfaces with off-chip ADC/DAC via SPI, achieving a closed-loop locking time of <10 s under typical conditions.

IV. Measurement Results

Fig. 5 shows the die micrograph. The active area of the analog core is 0.2mm^2, while the total chip area including pads is 2.0mm×2.0mm. The measurement setup consists of a voltage source, a signal generator, a lock-in amplifier, an 8-digit multimeter, and an external MCU.

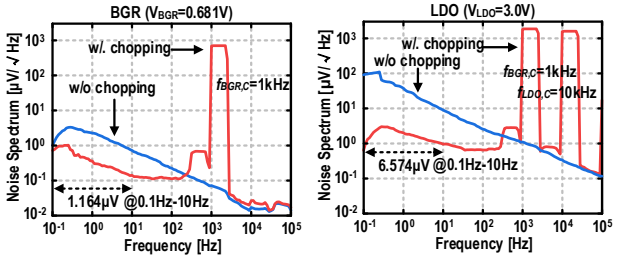


Fig. 6. Measured output noise of (a) BGR and (b) LDO.

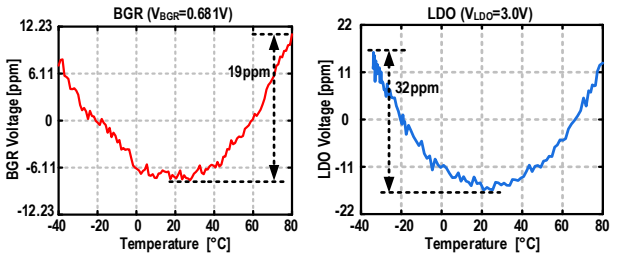


Fig. 7. (a)Measured BGR drift; (b)Measured LDO drift.

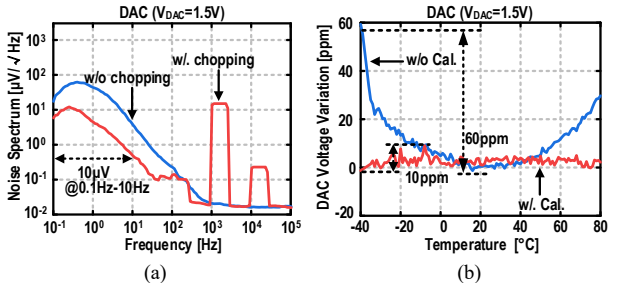


Fig. 8. Measured (a) output noise and (b) drift of 16-bit R-2R DAC.

A. Performance of BGR and LDO

Fig. 6 presents the measured output noise spectral density. With the proposed dual-chopping, the bandgap reference achieves a noise density of 512nV/$\sqrt{\text{Hz}}$ at 1 Hz, compared to 3.186μV/$\sqrt{\text{Hz}}$ without chopping. The integrated noise from 0.1 Hz to 10 Hz is 1.164μV. The LDO achieves a noise density of 2.96μV/$\sqrt{\text{Hz}}$ at 1 Hz, compared to 54.68μV/$\sqrt{\text{Hz}}$ at 1 Hz without chopping. The integrated noise of LDO from 0.1 Hz to 10 Hz is 6.574μV.

The temperature drift is shown in Fig. 7. Over -40°C to 80°C, the bandgap reference exhibits a temperature coefficient of 19ppm/°C.

B. Linearity and Noise of 16-bit DAC with DSM

The noise performance of the 16-bit R-2R DAC was measured using a lock-in amplifier. The static linearity of the 16-bit R-2R DAC was measured using an 8-digit multimeter. As shown in Fig. 8, the output noise spectrum shows a density of 4.95μV/$\sqrt{\text{Hz}}$ at 1 Hz and an integrated noise of 10μV from 0.1 Hz to 10 Hz. From −40 °C to 80 °C, the DAC output drift is less than 3 mV. As shown in Fig. 9, after off-chip calibration, the deviation between the output voltage and the ideal voltage can be maintained within 5 μV over a 1 mV range for all three output levels.

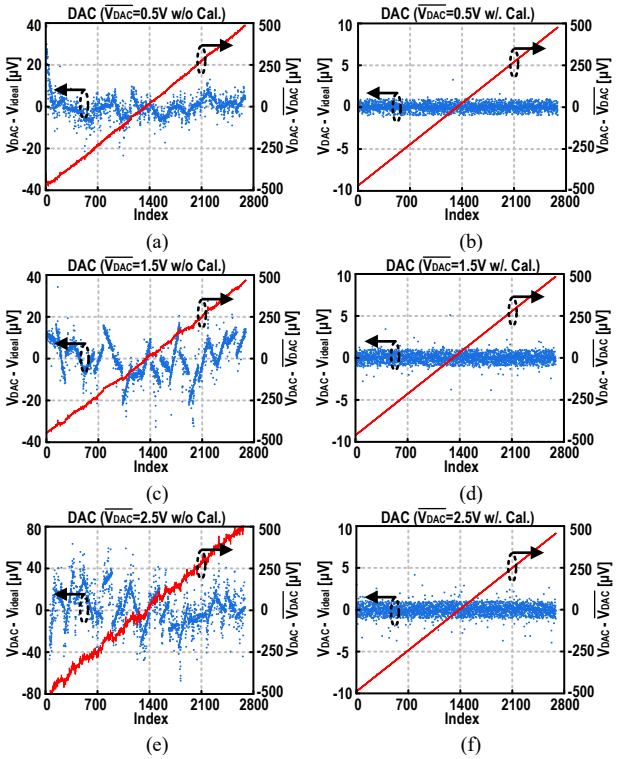


Fig. 9. Measured voltage error with the DSM calibration: (a) and (b) at V_{DAC}=0.5V; (c) and (d) at V_{DAC}=1.5V; (e) and (f) at V_{DAC}=2.5V.

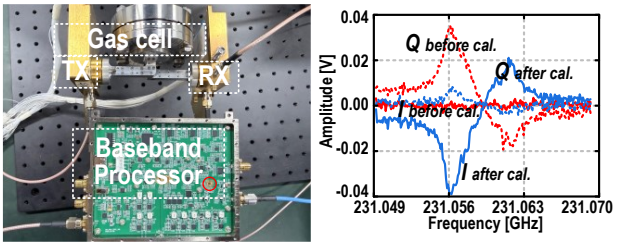


Fig. 10. Spectroscopic validation: (a) Test setup of WMS; (b) Demodulated I and Q baseband.

C. WMS Demodulation using Digital Baseband

Fig. 10(a) shows the measurement setup where the baseband chip is integrated with the TX, RX, and gas cell. In Fig. 10(b), the red curve represents the first spectrum sweep result, where the phase is random. The blue curve is the result of a second spectrum sweep after phase alignment following the first sweep. It can be observed that the I component is large while the Q component is small, indicating that the frequency has been aligned. This also indicates that the spectral detection function is operating normally.

V. Conclusion

This work presents the first baseband processor SoC for chip-scale molecular clocks in 65nm CMOS. The digital baseband integrates FM demodulation, PID control, temperature compensation, and clock disciplining. The dual-chopping BGR achieves 1.164 μV integrated noise (0.1–10 Hz). The 16-bit R-2R DAC with 3rd-order DSM maintains <5 μV deviation after calibration within 1 mV range. Together, they meet the 10^{-10} frequency stability target, demonstrating a self-contained solution for high-stability references.

TABLE II. Performance Comparison of the BGR.

Parameters	This Work	JSSC'25[3]	JSSC'24[4]	ISSCC'26[5]
Supply Voltage [V]	1.2	3-5	1.2-2.5	1.5-3.3
Ref.Voltage [V]	0.68	1.192	1.001	1.222
Noise Voltage [μV] @ 0.1Hz-10Hz	1.164	1.5	457	44
Temp. Range [°C]	-40 to 80	-55 to 125	-40 to 120	-40 to 125
Temp. Drift [ppm/°C]	19	3-8	18.6-28.8	1.02
DC Power [μW]	960	2360	0.9	22.5-49.5
Technology [nm]	65	180	65	180
Chip Area [mm^2]	0.125	0.55	0.04	0.068

TABLE III. Performance Comparison of the DAC.

Parameters	This Work	JSSC'26[2]	GLSVLSI'19[6]	AD5683[7]
DAC Arch.	R-2R	R-2R	R-2R	R-2R
DAC Res. [bit]	16	18	16	16
Range [V]	0-3	0-1.2	4.096	0-2.5/5
Voltage step w/. DSM [μV]	5	N/A	N/A	N/A
Voltage step w/o DSM [μV]	45	4.58	62.5	38.1/76.3
Noise [μV] @ 0.1Hz-10Hz	10	N/A	N/A	6
Temp. Drift [ppm/°C]	16.68	N/A	N/A	2
Technology[nm]	65	65	250	N/A
Area[mm^2]	0.2	0.754	8.4	N/A

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