A 12mW 7.8 Gb/s NRZ/PAM-4 Dual-Mode Digital Spectrum Shaping Signaling Transmitter for Multidrop Interfaces in 28 nm CMOS

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***Abstract*—This paper presents a *channel* (CH)-reconfigurable NRZ/PAM-4 dual-mode digital spectrum shaping signaling (DSSS) transmitter (TX) fabricated in 28 nm CMOS for multidrop bus (MDB) applications. The DSSS TX employs a $2\times$ repetitive block transmission to reshape the transmitted spectrum, effectively avoiding periodic spectral notches in MDB channels and achieving data rates exceeding $4\times$ the first channel notch frequency without requiring any receiver (RX) equalization. A reconfigurable multi-CH architecture supporting NRZ 2/3/4-CH and PAM-4 2-CH modes enables adaptive operation across MDB channels with different first notch frequencies. The TX also supports NRZ/PAM-4 1-CH mode for point-to-point (P2P) interfaces, ensuring compatibility across different link topologies. The prototype achieves 7.8 Gb/s (NRZ 4-CH) and 6.8 Gb/s (PAM-4 2-CH) over MDB channels with first notches at 1.8 GHz and 1.6 GHz, respectively. It consumes 12.3 mW and 9.5 mW from a 0.9 V supply, corresponding to energy efficiencies of 1.58 pJ/b and 1.40 pJ/b, respectively, while occupying an active area of 0.0243 mm^2.**

***Index Terms*—Multidrop interface, memory interface, SERDES, NRZ, PAM-4.**

I. Introduction

The multidrop bus (MDB) enables multiple nodes to share a single communication medium, providing an area- and cost-efficient alternative to point-to-point (P2P) topologies. However, MDB experiences severe signal integrity degradation due to impedance discontinuities introduced by multiple stubs along a shared bus. These discontinuities result in significant time-domain reflections and periodic spectral notches, limiting the achievable data rate [1]. Compensating for such reflective inter-symbol interference (ISI) typically requires multi-tap decision feedback equalizers (DFE) [2], which introduce significant power and area overhead. Alternative approaches have been proposed to mitigate these limitations [3]–[6], including analog multi-tone modulation [1] and phase-difference modulation (PDM) for spectral notch avoidance [7], and echo-canceling feed-forward equalization (EC-FFE) for the suppression of time-domain reflections [8]. However, these schemes come with considerable circuit complexity and lack compatibility with conventional P2P interfaces, limiting their applicability to dedicated MDB systems.

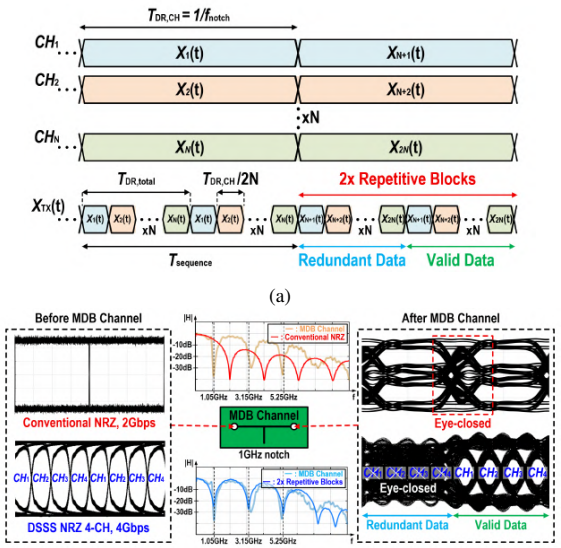

Fig. 1: A $2\times$ repetitive block transmission and CH structure of the DSSS scheme (a), and comparison between conventional NRZ and DSSS NRZ 4-CH over an MDB channel with a 1 GHz first notch.

This work presents a reconfigurable NRZ/PAM-4 dual-mode transmitter (TX) that employs digital spectrum shaping signaling (DSSS) for MDB while maintaining compatibility with conventional P2P interfaces. As shown in Fig. 1, DSSS applies a $2\times$ block repetition to each *channel* (CH), which reshapes the transmitted signal spectrum such that it avoids the impact of spectral notches in MDB channels [9]–[11]. For the NRZ 4-CH example in Fig. 1(b), when the symbol rate of each CH is aligned with the first spectral notch frequency of the MDB channel, reflections produce both constructive and destructive superposition in the time domain, resulting in one open and one closed eye among the two repeated symbols [10]. The proposed DSSS TX supports NRZ/PAM-4 1-CH mode for conventional P2P link operation, as well as reconfigurable NRZ 2/3/4-CH and PAM-4 2-CH modes for MDB operation,

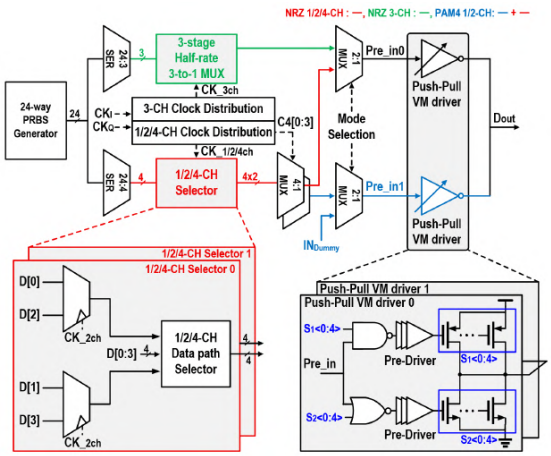

Fig. 2: Overall block diagram of the proposed CH-reconfigurable NRZ/PAM-4 dual-mode DSSS TX.

enabling flexible data rate scaling and spectral notch alignment for a given target data rate.

II. DSSS TX Architecture

Fig. 2 illustrates the overall architecture of the proposed CH-reconfigurable NRZ/PAM-4 dual-mode DSSS TX. The test chip receives in-phase (CK_{I}) and quadrature (CK_{Q}) quarter-rate clocks, which are distributed through separate clock paths to support NRZ 3-CH mode and all other modes. For NRZ 1/2/4-CH and PAM-4 1/2-CH modes, the PRBS data is serialized by a 24-to-4 serializer (SER), followed by a CH selector and a 4-to-1 MUX that generates the final serialized output using four-phase quarter-rate clocks. The output is then buffered by a pre-driver and delivered to a push-pull voltage-mode driver (PPVM-DR). To enable operation without a linear termination resistor, the PPVM-DR employs a NAND/NOR-based structure instead of a stacked-transistor topology [12], with digitally controlled on-resistance via S_1 and S_2. For PAM-4 operation, two parallel 4-to-1 MUX and PPVM-DR paths are combined to generate multi-level outputs. The same architecture can also support NRZ 2-tap FFE by adjusting the on-resistance of the PPVM-DR.

Similarly, for the NRZ 3-CH mode, the PRBS data is serialized by a 24-to-3 SER, followed by a 3-to-1 MUX that generates the final serialized output. To support high-speed operation in DSSS NRZ 3-CH mode, a three-stage half-rate 3-to-1 MUX structure is proposed instead of a conventional full-rate architecture, as shown in Fig. 3. The three input data streams are first re-timed in stage-1, then aligned through a MUX using clocks at one-third the reference clock frequency in stage-2, and finally reordered sequentially in stage-3 to complete the half-rate 3-to-1 MUX operation. This half-rate operation reduces the required clock frequency by half compared to a conventional full-rate 3-to-1 MUX, simplifying the clock distribution. Then, the 3-to-1 MUX output is forwarded to the PPVM-DR.

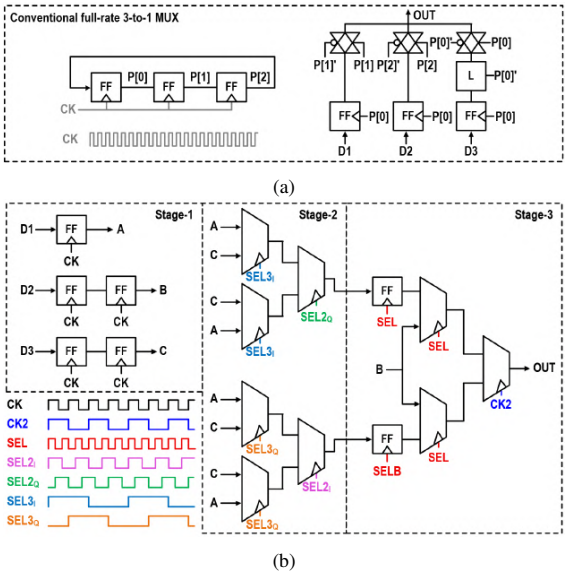

Fig. 3: Conventional full-rate 3-to-1 MUX (a) and proposed 3-stage half-rate 3-to-1 MUX for NRZ 3-CH mode (b).

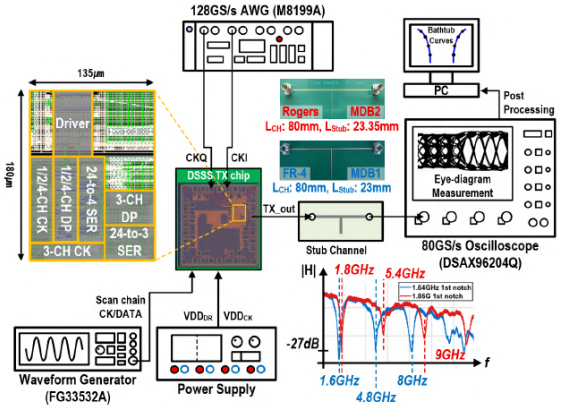

Fig. 4: Measurement setup of the proposed DSSS TX prototype and frequency responses of the two MDB channel boards.

Through CH-reconfigurable architecture, the proposed DSSS TX supports NRZ 1-CH and PAM-4 1-CH for conventional P2P interfaces, as well as NRZ 2/3/4-CH and PAM-4 2-CH for high-speed operation over MDB channels. The multi-CH modes enable spectral null alignment with different channel notch frequencies, maintaining a consistent target data rate across MDB channels.

III. Measurement Results

The proposed DSSS TX is fabricated in 28 nm CMOS process and characterized using wafer probe needles on the probe station, with the TX chip occupying $135 \times 180\,\mu m^2$, as shown in Fig. 4. The TX output is transmitted through an MDB channel board and captured by a DSAX96204Q real-time oscilloscope. The eye diagrams are observed on the oscilloscope, while the bit error rate (BER) bathtub curves

TABLE I: Summary and comparison of the proposed CH-reconfigurable NRZ/PAM-4 dual-mode DSSS TX with prior-arts.

	This work	[2]	[7]	[8]	[14]
Technology	28 nm CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS	40 nm CMOS
Supply voltage (V)	0.9	0.9	1.0	1.0	1.0
Architecture	TX	RX	TRX	TX	RX
I/O type	Single-ended	Single-ended	Single-ended	Single-ended	Single-ended
Compatibility with existing systems	Yes	Yes	No	Yes	Yes
First notch frequency	1.8 GHz first channel notch	0.4 GHz first channel notch	1.5 GHz first channel notch	0.4 GHz first channel notch	N/A
Signaling	NRZ/PAM-4 dual-mode	NRZ	PDM	NRZ	NRZ
Equalization	-	20-tap DFE	-	EC-FFE	*Self-Cal. DFE
Data pattern	PRBS15	PRBS7	PRBS7	N/A	N/A
Data rate (Gb/s/pin)	7.8	7.8	7.8	12	12.8
Energy efficiency (pJ/b)	1.58	2.88	1.96	**1.52	0.64
Area (mm^2)	0.0243	0.014	0.0078	0.01	0.018

*Self-Cal. DFE: Self-training calibration DFE. **Energy efficiency is obtained from the data path power only.

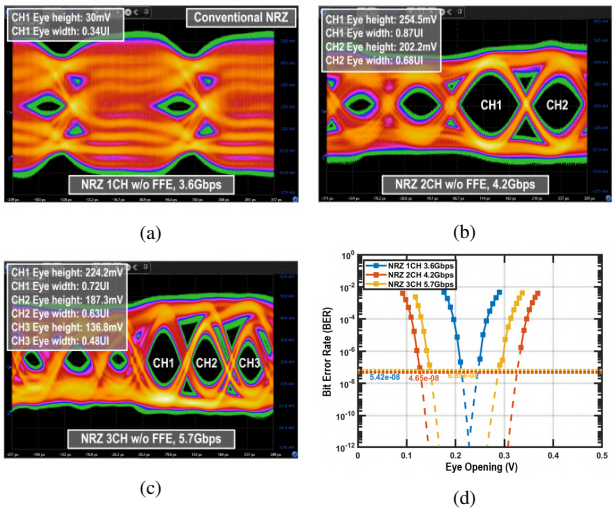

Fig. 5: Measured eye diagrams over MDB2 (1.8 GHz first notch): (a) conventional NRZ 1-CH (3.6 Gb/s), (b) DSSS NRZ 2-CH (4.2 Gb/s), (c) DSSS NRZ 3-CH (5.7 Gb/s), and (d) the corresponding vertical bathtub curves at the best decision phase for NRZ 1/2/3-CH.

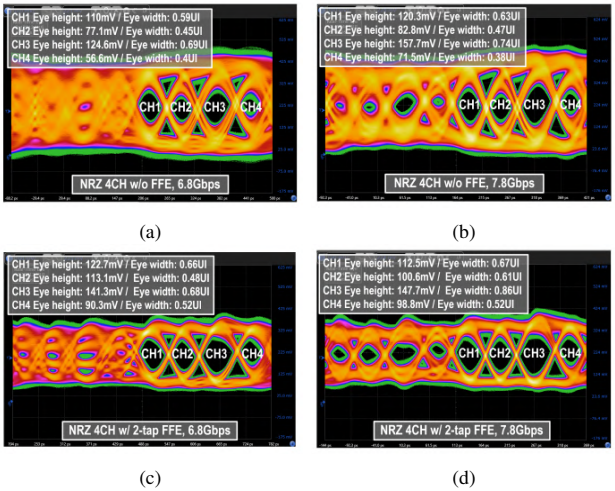

Fig. 6: Measured DSSS NRZ 4-CH eye diagrams over MDB1 (6.8 Gb/s) (a) without and (c) with 2-tap TX FFE, and over MDB2 (7.8 Gb/s) (b) without and (d) with 2-tap TX FFE.

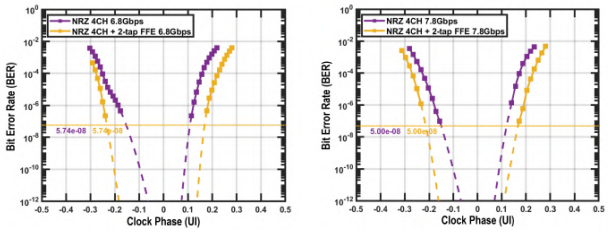

Fig. 7: Horizontal bathtub curves at the best decision phase for DSSS NRZ 4-CH without and with 2-tap TX FFE over (a) MDB1 (6.8 Gb/s) and (b) MDB2 (7.8 Gb/s).

are obtained through off-line processing by recording the waveform at an 80 GS/s sampling rate and counting bit errors for each measurement using a PRBS-15 pattern [13]. Two MDB channel boards are evaluated, as shown in Fig. 4, where MDB1 is fabricated on FR-4 with a first notch at 1.6 GHz and MDB2 is fabricated on Rogers material with a first notch at 1.8 GHz.

Fig. 5 shows the NRZ 1/2/3-CH eye diagrams and vertical bathtub curves over MDB2. Conventional NRZ 1-CH at 3.6 Gb/s exhibits an extrapolated BER of 1E-12 with a near-zero eye opening, whereas the NRZ 2-CH and 3-CH modes achieve the same BER with vertical openings of 152 mV and 103 mV at 4.2 Gb/s and 5.7 Gb/s, respectively, by mitigating the impact of the spectral notch. Fig. 6 shows the NRZ 4-CH results over both MDB channels. Over MDB1 (Fig. 6(a), (c)), the DSSS TX achieves 6.8 Gb/s, consuming 11.2 mW and 12.1 mW without and with 2-tap TX FFE, respectively, from a 0.9 V supply, corresponding to more than 2× the data rate of conventional NRZ. Over MDB2 (Fig. 6(b), (d)), the TX achieves 7.8 Gb/s, exceeding 4× the first channel notch frequency, while consuming 12.3 mW and 13.0 mW without and with 2-tap TX FFE, respectively. The corresponding horizontal bathtub curves in Fig. 7(a), (b) show that applying 2-tap TX FFE improves the horizontal eye margin by 0.1 UI on both channels.

Fig. 8 shows the PAM-4 1-CH and 2-CH eye diagrams over both MDB channels. Conventional PAM-4 achieves 5.2 Gb/s and 5.6 Gb/s over MDB1 and MDB2, respectively, consuming 6.8 mW and 7.0 mW, while the PAM-4 2-CH mode increases the data rate to 6.8 Gb/s and 7.4 Gb/s with improved multi-level eye openings enabled by DSSS. The corresponding hor-

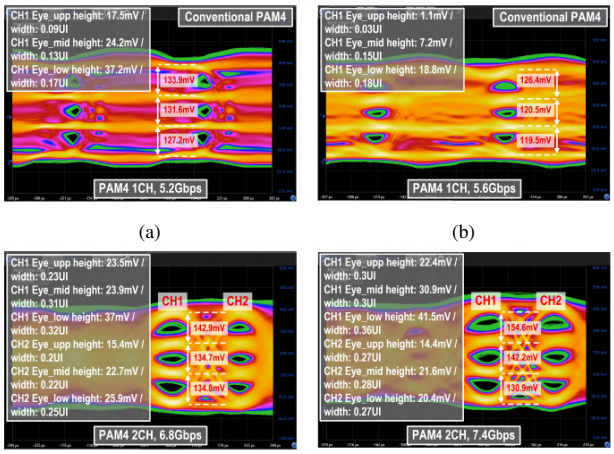

Fig. 8: Measured PAM-4 eye diagrams: (a) conventional PAM-4 1-CH over MDB1 (5.2 Gb/s) and (b) MDB2 (5.6 Gb/s), and (c) DSSS PAM-4 2-CH over MDB1 (6.8 Gb/s) and (d) MDB2 (7.4 Gb/s).

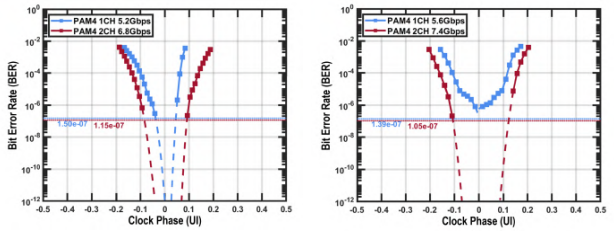

Fig. 9: Horizontal bathtub curves at the best decision phase for conventional PAM-4 1-CH and DSSS PAM-4 2-CH over (a) MDB1 and (b) MDB2.

izontal bathtub curves in Fig. 9 confirm improved horizontal eye margins for PAM-4 2-CH across both channels.

Table I summarizes the performance of the proposed TX and compares it with prior MDB designs. The DSSS TX achieves 6.8 Gb/s (PAM-4 2-CH) and 7.8 Gb/s (NRZ 4-CH), both exceeding $4\times$ the first channel notch frequencies of 1.6 GHz and 1.8 GHz, respectively, with energy efficiencies of 1.40 pJ/b and 1.58 pJ/b from a 0.9 V supply and an active area of 0.0243 mm^2.

IV. Conclusion

This paper presents a CH-reconfigurable NRZ/PAM-4 dual-mode DSSS TX implemented in 28 nm CMOS, supporting both MDB and P2P interfaces through multiple operating modes to adapt to different channel conditions. The DSSS TX employs a $2\times$ repetitive block transmission to reshape the transmitted spectrum, effectively avoiding periodic spectral notches in MDB channels and achieving data rates exceeding $4\times$ the first channel notch frequency. The TX core occupies 0.0243 mm^2 and achieves up to 7.8 Gb/s (NRZ 4-CH) and 6.8 Gb/s (PAM-4 2-CH) over MDB channels with first notch frequencies of 1.8 GHz and 1.6 GHz, respectively, with energy efficiencies of 1.58 pJ/b and 1.40 pJ/b from a 0.9 V supply. To the best of our knowledge, this is the first reported DSSS TX with an integrated clock and data path, providing a low-complexity solution that enables high-speed data transmission over notch-limited MDB channels without relying on power-hungry long-tap DFE, thereby overcoming a fundamental limitation of conventional NRZ and PAM-4 signaling.

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