A 25% PAE 14 dBm Harmonic-Shaping 110 GHz Power Amplifier using modified EMCC as 4-Way Power Combiners in 22 nm FDSOI CMOS

Rui Zhou, Sarah Koop-Brinkmann, Victor Lasserre, Finn Stapelfeldt, Vadim Issakov
Institute for CMOS Design, Braunschweig University of Technology, Germany
r.zhou@tu-braunschweig.de

***Abstract* — This work presents a highly efficient 110 GHz power amplifier in CMOS. By means of harmonic termination of fundamental (H1) and third harmonic (H3) offered by a multi-resonant fourth order filter, we boost the power per stage and efficiency. This is achieved by modification to an Enhanced Magnetic Coupling Cavity (EMCC) power combiner, enabling not only low-loss combinig, but also enhanced harmonic loadline matching. The circuit is realized in 22 nm FDSOI CMOS. It achieves 25% PAE and 14 dBm P_{sat}. To the best of author's knowledge, this is the highest reported PAE at this frequency range in CMOS.**

***Keywords* — power amplifiers, CMOS, D-Band, slotline.**

I. Introduction

Recently, frequencies around 120 GHz attract strong research interest, particularly for consumer and industrial radar applications. To cover distances up to tens of meters, a sufficiently high saturated output power P_{sat} above 10 dBm at the antenna feed-point is required. Further, most consumer radars require a very high efficiency, especially for battery operated application scenarios. Luckily, a frequency-modulated continuous wave (FMCW) modulation has a constant envelope and thus the power amplifier (PA) is operated at P_{sat} [1], which removes the requirement on back-off efficiency as in amplitude modulation schemes.

Since a high power >10 dBm is needed at frequencies above 100 GHz, a natural choice would be to use a III/V technology. However, CMOS is strongly preferred because of the integration capabilities with digital baseband.

Yet, it is very challenging to realize a millimeter-wave (mm-wave) PA at frequencies above 100 GHz in advanced CMOS nodes for several reasons. First, the low breakdown voltages and long-term reliability considerations prevent developing a high voltage swing. Second, ratio of f_T/f_{max} to the operating frequency is low, degrading the achievable G_{max}, limit the output power and efficiency per stage. To increase the output power, one can normally a) use large size MOS transistors; and/or b) combine multiple amplifier stages by passive power combining. However, a) increasing transistor size (to increase maximum current swing) or stacking multiple transistors (to increase voltage swing) suffers from severe parasitics [2], which greatly reduce gain and achievable power added efficiency (PAE). And, b) on-chip power combiners at mm-wave frequencies have high insertion loss and degrade the PAE. Hence, these techniques help only to a limited extent, proving inefficient for a large number of combined stages.

Therefore, most works focus on optimizing the passive combining network, including three-conductor self-shielding load-open balun [3], subquarter-wavelength transmission line [4], and slotline-based combiner [5].

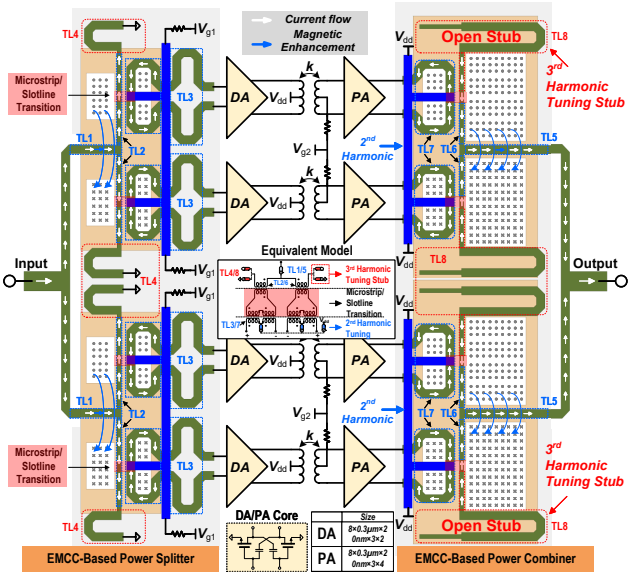


Fig. 1. Top level block diagram of the proposed high efficiency PA with modified EMCC structures for H1 and H3 harmonic termination.

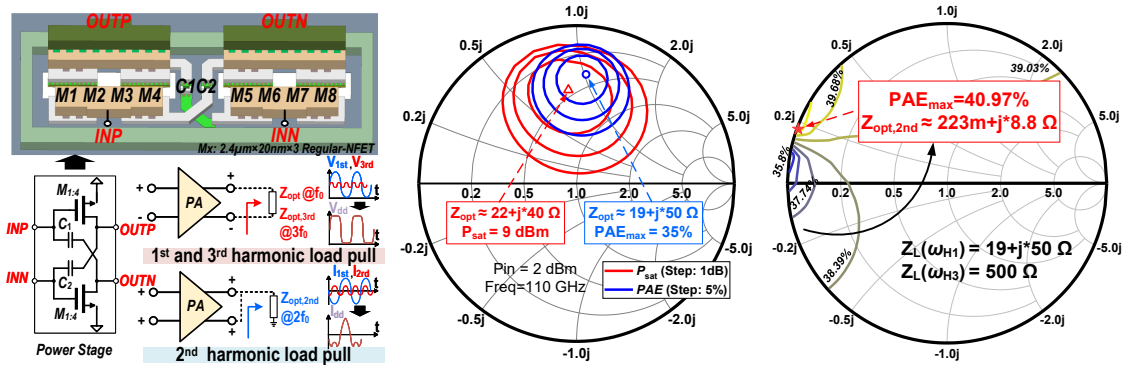
The slot-slite EMCC power combiner in [6] offers a very low insertion loss at mm-wave frequencies and is a promising candidate for an efficient N-way power combining. However, the work in [6] achieves a low PAE of 6%. In this work, we propose to use the EMCC structure not only as a power combiner, but also for multiple harmonics impedance termination simultaneously. By modifying EMCC to provide the optimal impedances simultaneously at H1, H2 and H3, we achieve harmonic shaping and strongly increase efficiency.

II. Circuit Design and Analysis

Fig. 1 presents the top level diagram of the proposed high-efficiency D-Band PA based on harmonic impedance tuning. This PA includes two differential common-source stages with a 4-way differential power combining/splitting network. To simultaneously achieve fundamental (H1) , second (H2), and third (H3) harmonic matching at the PA output, an EMCC-based microstrip/slotline transition network is adopted, which also provides a low insertion loss.

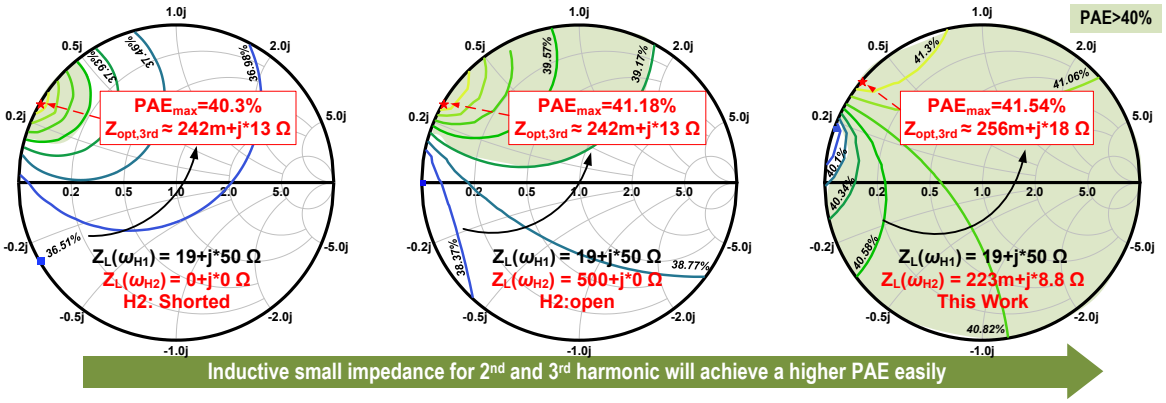
A. Power Cell Design and Harmonic Load-Pull

The layout sketch of the power core is shown in Fig. 2(a) using 8 parallel 2.4 µm×20 nm×3 regular NFET transistors



(a) (b) (c)

Fig. 2. (a) Layout sketch of the power core. (b) Fundamental load-pull contour. (c) Second harmonic load-pull contour.



(a)

Fig. 3. 3rd harmonic load-pull with different 2nd harmonic load impedance (a) 0+$j\times$0 Ω; (b) 500+$j\times$0 Ω; (c) 223m+$j\times$8.8 Ω.

M_1 to M_8 with two MOM capacitors C_1 and C_2. Small parallel transistors are used here for better gain and power performance. Meanwhile, the power core operates in an under-neutralized state by designing capacitors C_1 and C_2 smaller than the Miller capacitor C_{gd}. This approach not only achieves high gain and output power, but also ensures stability [3]. Fig. 2(b) shows the simulated load-pull contour of the power stage for the H1 impedance. During simulation, the source load at the fundamental frequency is set to the conjugate of input impedance and the other harmonic impedance is initially set to 500 Ω. With 2 dBm input power, the proposed power stage can provide a peak output power of 9 dBm and a maximum PAE of 36 %. The optimal differential load impedance is about 19 + $j\times$ 50 Ω at 110 GHz.

To further improve power efficiency, harmonic shaping can be used. Due to the limited f_T and f_{max}, it is challenging to develop a strong H3 component. Hence, it is impractical to form a quasi-square drain voltage v_{ds} waveform for class-F operation (H2 short, H3 open). Similarly, it is difficult to realize an inverse class-F (F^{-1}), due to the H2 component [7], since it requires H2 open and H3 short. However, even if we cannot achieve a perfect short or open, controlling harmonic load impedances is still useful to improve efficiency, because one can reduce the overlap of v_{ds} and i_{ds}. In that case, i_{ds} is high when v_{ds} is low, or i_{ds} low when v_{ds} is high, thus reducing power dissipation, as shown in Fig 4.

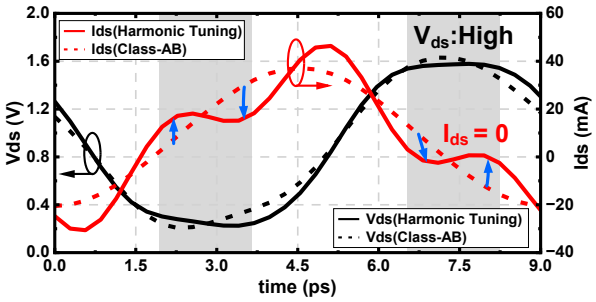


Fig. 4. Simulated drain voltage and current waveforms for power core.

In this work we directly perform a harmonic load-pull on H1, H2, and H3. Fig. 2(c) shows the H2 load-pull contours under loading condition $Z_L(\omega_{H1})$ at $Z_{opt,H1}$ = 19 + $j\times$ 50 Ω (obtained from Fig. 2b) and $Z_L(\omega_{H3})$ at 500 Ω. A low inductive load impedance at H2 is needed for efficiency boosting. To further estimate the impact of H2 and H3 on efficiency, we perform load-pull on H3 for different H2 load impedances, as illustrated in Fig. 3. It can be seen that when H2 load impedance is close to $Z_{opt,H2}$ = 223m + $j\times$ 8.8 Ω, the impact of the H3 harmonic load will be reduced. This means, the

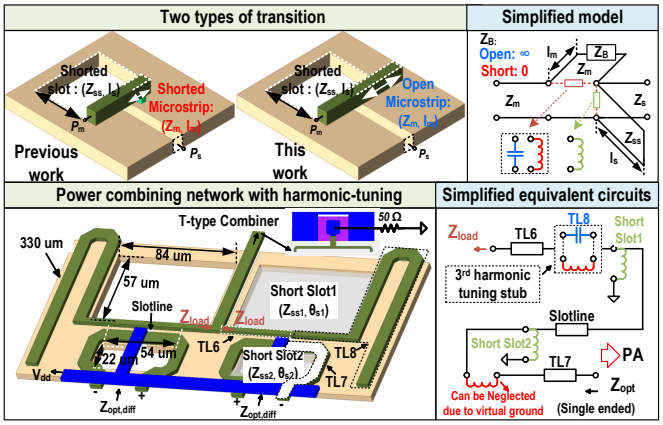


Fig. 5. Two types of microstrip/slotline transition and the proposed power combining network with harmonic-tuning, and their simplified equivalent circuits.

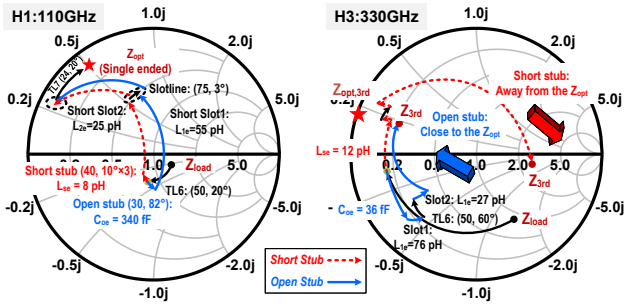


Fig. 6. Impedance transformation trajectory through different types of transition at fundamental and third harmonics.

selection of the H3 load impedance will be easier and design more robust. Also, we see that the optimal load at H3 is close to an inductive low impedance, regardless of the H2 load.

Therefore, the most reliable way is to terminate both harmonics (H2, H3) close to the low inductive impedance simultaneously. This minimizes the impact of uncertain factors, such as DC feed at the common mode impedance at H2. Fig. 4 shows the simulated v_{ds} and i_{ds} with conventional Class-AB and the proposed harmonic tuning. The gates are biased at $V_{gs} = 0.5\,\text{V}$, the drains are supplied by $V_{dd} = 0.9\,\text{V}$ for an input power of 2 dBm in both cases. Compared to class-AB, the v_{ds} and i_{ds} are closely shaped into a quasi-square waveform and half-sinusoidal, reducing overlap and power dissipation.

B. EMCC-based Impedance Matching Network Realization

Based on the above design requirements, an output network needs to be designed to meet impedance matching, while ensuring a low insertion loss. Here, an EMCC-based power-combining structure is utilized [6]. Compared to single or coupled transmission line (TL) power combining networks, a slotline solution can provide a better common-mode rejection due to the boundary-condition-enforced odd-mode fields: it offers a higher common-mode rejection, which results in a better decoupling between differential and common modes. This is crucial for adjusting different harmonic impedances

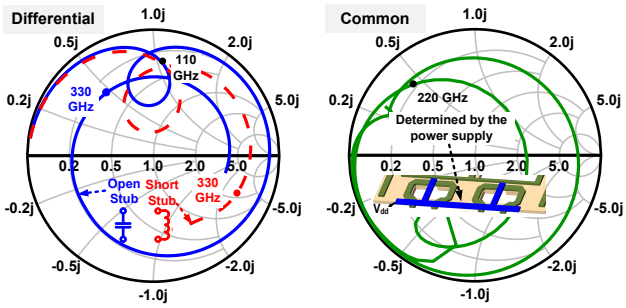


Fig. 7. Simulated input impedance at one of the differential ports.

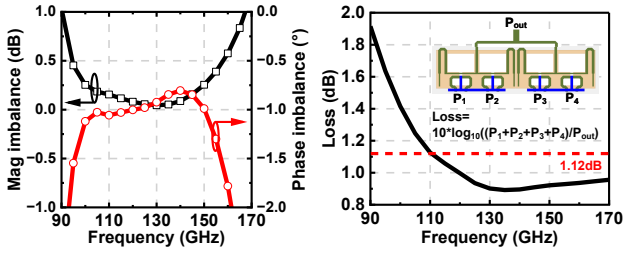
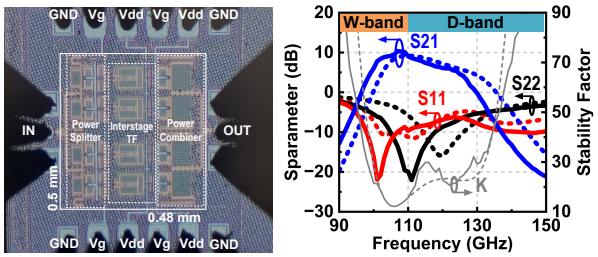


Fig. 8. Simulated results of (a) magnitude/phase imbalance and (b) combining loss.

separately. Therefore, the non-predictable H2 load will not affect H1 and H3 loading realized by the same network.

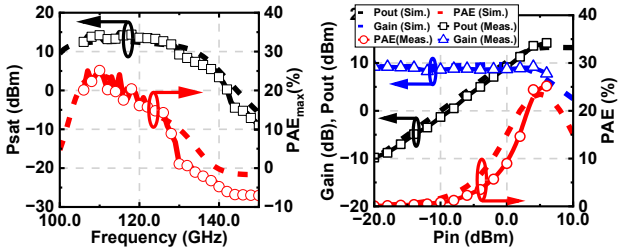
Fig. 5 presents a detailed illustration of the EMCC-based power combining network. Instead of using a typical *shorted* microstrip line [6], we propose using an *open* microstrip, to achieve an improved H3 load impedance. Here, a simplified model with uniform microstrip and slotlines is utilized [8]. With this model, the equivalent circuit can be simplified to a multi-resonant fourth order filter, which has the ability to load harmonics. Fig. 6 shows the impedance transformation trajectory using this equivalent circuit. At H1 both state of the art [6] and our solution achieve similar impedance transformations. However, at third harmonic the H3 impedance is transformed to different regions. The open stub, used in this work, transforms the Z_L closer to the optimum impedance region, which we have analyzed above, while the short stub [6] moves away from it. In such a case, any deviation in the second-harmonic impedance will lead to a rapid efficiency degradation. Fig. 7 shows the EM simulation results of the EMCC-based network with different types of stubs. It matches the theoretical results very well. For the 2^{nd}-harmonic impedance, it is adjusted primarily by tuning the length of the V_{dd} feed line at the center-tapped junction due to the high common-mode suppression of the microstrip/slotline transition, to keep the impedance within the desired region.

Fig. 8 presents simulation results using 3D full-wave HFSS solver of the implemented 4-way EMCC-based differential power combining network in 22 nm FDSOI CMOS. It achieves a combining loss less than 1.12 dB within the whole D-band, and it also exhibits a minimum magnitude imbalance of 0.05 dB and a phase imbalance of 0.8°.



(a) (b)

Fig. 9. (a) Die micrograph of the PA. (b) Measured (solid) and simulated (dashed) S-parameters and stability factor (K) of the proposed PA.



(a) (b)

Fig. 10. (a) Measured (solid) and simulated (dashed) P_{sat} and PAE_{max}. (b) Measured (solid) and simulated (dashed) P_{sat}, PAE and gain at 110 GHz.

III. Measurement Results

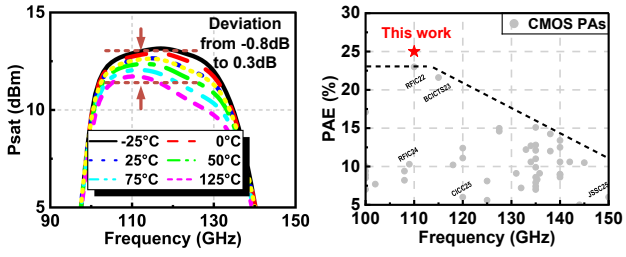
The proposed high efficiency PA is designed and fabricated in a 22 nm FDSOI CMOS technology. Fig. 9(a) shows the PA die micrograph. The chip occupies 0.8×0.7 mm^2 with a core area of 0.5×0.48 mm^2. The gates are biased at 0.32 V for first stage and 0.5 V for output stage. The drain supply is 0.9 V.

Fig. 9(b) shows the simulated and measured S parameters. The proposed PA achieves a small signal bandwidth of 3 dB from 100 to 124 GHz. The measured peak small signal gain is 10 dB. In large-signal continuous-wave measurements, the D-band RF signal is generated by a Keysight analog signal generator with a D-band frequency extender and an attenuator for accurate input power sweeping. This PA has a maximum output power of 14 dBm with a 3 dB large signal bandwidth from 100 to 130 GHz, as shown in Fig. 10(a). Thanks to the harmonic tuning method, the PA achieves a peak PAE of 25% at 110 GHz. Fig. 10(b) demonstrates the measured output power P_{out}, power gain, and PAE versus input power at 110 GHz. Fig. 11(a) shows robustness of the proposed approach versus temperature variation in simulation. Fig. 11(b) positions this work compared to the state of the art.

Table 1 summarizes and compares the performance with the state-of-the-art PAs. It can be seen that the proposed PA achieves 25% PAE with 14 dBm output power and low static power consumption. To the best of authors' knowledge, this is the highest reported PAE at this frequency range in CMOS.

IV. Conclusion

We have presented a PA using a modified EMCC-based power combining network, which enables robust control of H1 and H3 to achieve highest PAE in 22 nm FDSOI CMOS.



(a) (b)

Fig. 11. (a) Simulated P_{sat} over temperature and (b) performance comparison.

Table 1. Performance summary and comparison

Reference	**This work**	CICC'25 [6]	ISSCC'20 [9]	BCICT'23 [4]	ESSC'22 [10]
Technology	**22nm FDSOI**	28nm CMOS	16nm FinFET	22nm FDSOI	22nm FDSOI
Frequency(GHz)	**110**	120	130	115	125
3dB-BW (GHz)	**24**	28	24	15	38
P_{sat}-BW (GHz)	**30**	40	40	38	N/A
Gain (dB)	**10**	20	20	12	13.5
P_{sat} (dBm)	**14**	21.2	15	18.6	17.5
OP1dB (dBm)	**13**	16.6	9.2	14	N/A
PAE_{max} (%)	**25**	6.1	12.8	21.6	16.5
Supply (V)	**0.9**	1	1	1	1.1
P_{dc} (mW)	**50**	N/A	207	N/A	N/A
Area (mm^2)	**0.24**	0.62	0.062	0.183	0.113

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