An Auxiliary Receiver with Enhanced Close-In Blocker Tolerance

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***Abstract*—An auxiliary receiver for self-interference cancellation is proposed. It includes a second-order filtering transimpedance amplifier based on a single op-amp with positive feedback to improve the compression point at small frequency offsets from the carrier. The receiver has a baseband bandwidth of 10 MHz, NF of 3.8 dB and a blocker induced 1 dB compression point of -10 dBm at 20 MHz offset and up to 0 dBm at 80 MHz offset. The power dissipation is 37 mW in the signal path and 10 mW/GHz for clock generation. The chip is implemented in a 28nm CMOS technology and occupies an area of 0.6 mm^2.**

Keywords— SAW-less, blocker-tolerant receiver, second-order transimpedance amplifier (TIA), positive feedback

I. Introduction

With the proliferation of operating bands in the sub-7 GHz frequency range, mobile receivers need to tolerate large blockers that are located close to the receive band. In Frequency-Division-Duplex (FDD) bands the transmitter leakage is often the largest interferer, causing both compression and sensitivity degradation due to noise leakage. Duplexers face conflicting requirements between size, insertion loss and TX-RX isolation. To address these challenges self-interference cancellation (SIC) architectures have been proposed, including auxiliary receiver paths that perform interference cancellation at RF, in the analog baseband or in the digital domain, as depicted in Fig. 1 [1][2]. In this work we propose an auxiliary receiver that can be used for TX noise leakage cancellation in channels with small duplex frequency separation thanks to its enhanced linearity with respect to signals at small frequency offsets from the carrier. Noise leakage cancellation relaxes duplexer isolation requirements. Duplexers TX-RX isolation is typically in the order of 55 dB. Relaxing this by 10-15 dB or more could open the way to tunable or non-SAW/BAW duplexers.

II. Auxiliary Receiver Architecture

A. Self-Interference Cancellation Requirements

Injecting the SIC signal into the main receiver path introduces noise from the auxiliary path. In SIC architectures TX-RX isolation requirements are determined by the auxiliary receiver power handling capabilities and by its own noise (N/B_{1dB}), rather than by the TX noise-to-carrier (N/C) ratio. For a transmitter power of 27 dBm and a noise leakage of -180 dBm/Hz, a TX N/C of -152 dBc/Hz requires 55 dB isolation. An auxiliary RX with N/B_{1dB} of -167 dBc/Hz (e.g. -5 dBm B_{1dB} and 4 dB NF) gives the same leakage with only 40 dB isolation.

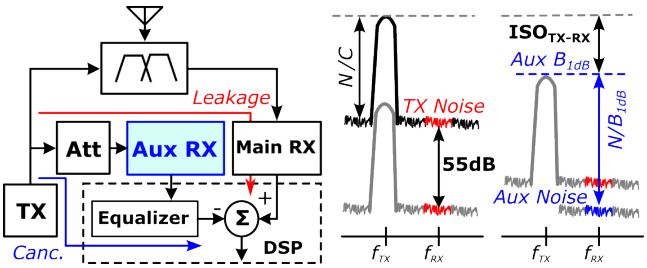

Fig. 1. FDD receiver with self-interference canceling architecture

B. Blocker-Tolerant Front-End Design

To improve blocker resilience several works have adopted mixer-first architectures with high order baseband filters [3]-[6]. Others have introduced an N-path feedback loop around the LNA with sharp filtering [7]. Both architectures are not appropriate for auxiliary receivers since the low input impedance in the transmit band and LO leakage can harm the transmitter. For these reasons an LNA-first solution was adopted in this work.

C. Highly Linear LNA

A LNA with high linearity and good reverse isolation is desirable. The large TX signal can lead to compression right at the LNA stage. An inductively degenerated LNA can be optimized for linearity instead of noise by choosing a large source degeneration inductance [8]. This solution suffers from noise folding from the harmonics, but this effect can be mitigated with a resonant cross-coupled common-gate second LNA stage. Overall, this results in a moderate NF, but a high compression point, minimizing the B_{1dB}/N ratio, which is the key metric for auxiliary receivers. The two-stage LNA in Fig. 2 achieves 3.2 dB NF and 3 dBm B_{1dB} while dissipating 9.5 mW.

D. Highly Linear Baseband Designs

At small offset frequencies blocker tolerance is dominated by the transimpedance amplifier (TIA) following the mixer. To improve TIA linearity different solutions have been introduced, mostly focusing on high order filtering [3][4][8] (Fig. 3.a-c). In these works, the impedance at the TIA input is not a virtual ground as in classical first-order TIAs, but is instead shaped to introduce higher order filtering. This tends to place a relatively large capacitance at the TIA input. In our work a TIA is proposed which implements a 2nd order low-pass filter while preserving a

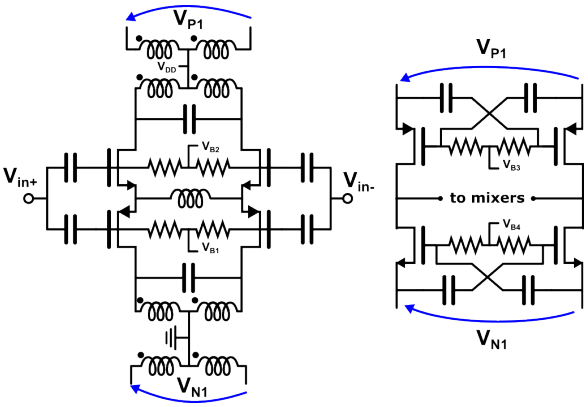

Fig. 2. Two-stage LNA schematic

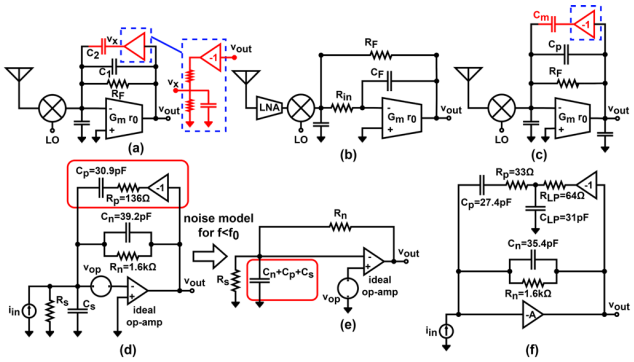

Fig. 3. TIA in [3] a) Rauch filter [8] b) TIA in [4] c) TIA with a series RC in positive feedback d) noise model e) and TIA with an extra RC filter f)

virtual ground at its input exploiting a positive-feedback passive network. The virtual ground ensures: 1) maximum current transfer from the mixer to the TIA; 2) linearity improvement of the LNA and mixers, as the blocker-induced LNA output voltage is minimized; 3) low TIA input capacitor, thus improving noise.

III. TIA Circuit Implementation

A. Second-Order Low-Pass TIA Design

If a series RC in positive feedback is introduced in a standard TIA (Fig. 3.d), a 2nd-order low-pass filter with complex-conjugate poles at frequency f_0 is obtained which has a parasitic high-frequency zero at f_z. Assuming an ideal operational transconductance-amplifier (OTA), the transfer function is:

$$\frac{v_{out}}{i_{in}} = -R_n \cdot \frac{1 + sR_pC_p}{1 + \frac{1}{\omega_0 Q}s + \left(\frac{s}{\omega_0}\right)^2} \quad (1)$$

$$\omega_z = \frac{1}{R_pC_p} \quad (2)$$

$$\omega_0 = \frac{1}{\sqrt{R_pC_pR_nC_n}} \quad (3)$$

$$Q = \frac{\sqrt{R_pC_pR_nC_n}}{C_pR_p + C_nR_n - C_pR_n} \quad (4)$$

Targeting complex poles with a Q = 0.7 and $\omega_z/\omega_0 = 4$, C_p is slightly smaller than C_n. Compared with [3], where a resistive divider and an extra capacitor are used in the positive feedback path, the total capacitance is reduced by roughly a factor of four. The zero at f_z can be pushed to higher frequency, but this trades-off with the noise introduced by the OTA. It can be shown that in single-OTA biquads using a positive feedback capacitor, the OTA noise t.f. has 2 real zeroes, f_{z1} and f_{z2}, with $f_{z1}<f_0<f_{z2}$. For frequencies $f<<f_0$ it can be proved that the OTA noise can be modelled as in Fig. 3.e. Capacitor C_p appears in parallel with C_n between virtual ground and ground, leading to a zero in the OTA noise t.f.. Increasing f_z while simultaneously keeping f_0, Q and R_n constant forces C_p and C_n to increase, thus, simultaneously, f_{z1} decreases, boosting the OTA noise. Hence, the addition of the positive-feedback capacitor C_p to a standard TIA leads to an increment of the OTA average in-band noise. Minimizing C_n and C_p is important to minimize OTA noise.

B. Addition of an Extra RC in the Positive-Feedback Loop

The positive-feedback TIA in Fig. 3.d can be modified by introducing an extra RC filter (R_{LP} and C_{LP}) in the positive-feedback loop as depicted in Fig. 3.f. The closed-loop transimpedance t.f. now has 3 poles and 2 zeroes. The additional pole and zero can be set well outside the band (in this work at 400 MHz). More importantly, the introduction of R_{LP} and C_{LP} allows to lower the sum of C_n and C_p (from 70.1 pF to 62.8 pF) for the same f_0, Q, R_n and f_z which is beneficial for noise since f_{z1} increases (from 1.39 MHz to 1.57 MHz), using moreover same total capacitance (including C_{LP}) in a fully-differential implementation. Hence, this topology improves the trade-off between noise and filtering in single OTA-biquads based on positive capacitive feedback.

C. OTA Implementation

The chosen design approach has benefits, but entails several design challenges: 1) the virtual ground must be ensured up to the blocker frequency f_B to track the fast blocker current variations, forcing the TIA loop-gain to have a unitary gain frequency much larger than f_B; 2) the reduced input capacitor forces the OTA to absorb most of the blocker current; 3) TIA stability must be ensured. Points 1) and 2) are solved using a 3-stages OTA with a class-AB 3rd stage. This ensures large loop gain and the capability to absorb the large currents. The OTA has been implemented as depicted in Fig. 4. It consists of the cascade of 3 stages: the 1st and 2nd stages are fully-differential to suppress any common-mode signals thanks to current sources MCS1 and MCS3. Transistor MCS2 in the 1st stage is controlled by a CMFB network. The 2nd stage is a differential pair with PMOS load. In dc the PMOS are diode-connected with large RCMFB, so no extra CMFB network is required. To increase the short-circuit transconductance at higher frequencies, a high-pass filter C_{HP} R_{HP} has been introduced. The 3rd stage is a class-AB differential circuit: considering the slewing condition, if out_m2 undergoes a large swing, MP4 can deliver a much larger current than its quiescent current. Although it is class-AB, the 3rd stage can have good CMRR with proper design: excited by common-mode input signals, the small-signal currents in MP4 and MN4 have the same sign, so if they are approximately equal, cancel each other.

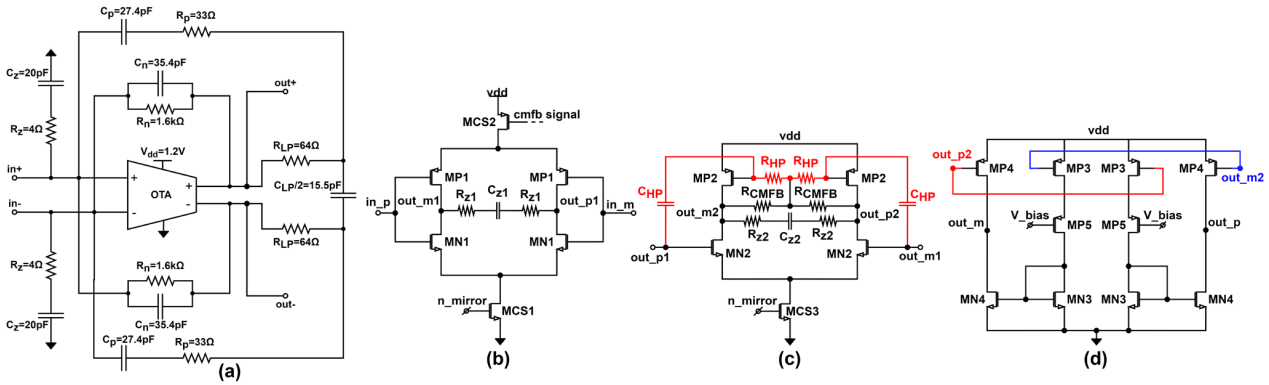

Fig. 4. Differential TIA schematic a) and three-stages OTA circuit diagram: first stage b) second stage c) third stage d)

D. TIA Stabilization

Since the OTA consists of the cascade of 3 stages, at least 3 poles are introduced in the TIA loop-gain. As the feedback network introduces 3 zeroes and 2 poles, the loop-gain will have at least 5 poles and 3 zeroes, complicating stabilization. A stable response is accomplished by introducing a series RCR branch at the output of the 1st stage (R_{z1} and C_{z1}) and 2nd stage (R_{z2} and C_{z2}). The introduction of a series RC load pushes the pole of each stage to lower frequencies and introduces an extra zero-pole doublet. The zero can be pushed to lower frequencies to compensate the pole, whereas the extra pole must be placed at frequencies much larger than the unitary BW of the loop. A resistance R_z is connected in series with the large capacitance (C_z in Fig. 4.a) present at the TIA virtual ground to absorb signals at the mixer harmonics. This creates an extra negative zero that can be placed around the unitary BW to improve the phase margin. Applying this stabilization methodology, a dc loop gain of roughly 50 dB is achieved, with a 75° phase margin at the 2.1GHz unitary-gain bandwidth f_U. More than 35 dB loop-gain is obtained up to 80 MHz, which ensures a good virtual ground and a high compression point at all blocker frequencies.

IV. Measurements Results

The chip was realized in a 28nm CMOS technology and has an active area of 0.6 mm2. The receiver includes an inductively-degenerated two-stage LNA, down-conversion mixers, positive-feedback based TIAs and frequency dividers for on-chip quadrature LO generation. A chip microphotograph is shown in Fig. 5.b. The chip was wire-bonded on a board for testing purposes. The measurement setup is depicted in Fig. 5.a and includes an external balun used to provide a differential input signal.

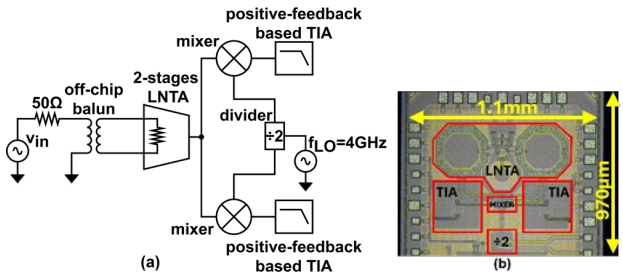

Fig. 5. Measurement setup a) and chip microphotograph b)

The measured down-conversion gain versus output frequency for f_{LO} = 4GHz is reported in Fig. 6.

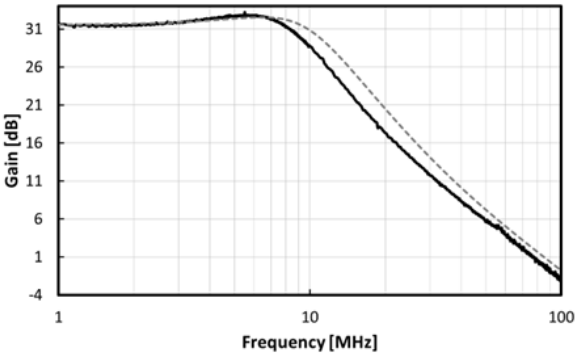

Fig. 6. Measured (solid) and simulated (dashed) down-conversion gain

In-band down-conversion gain is 31.5 dB. Thanks to second order filtering provided by the positive feedback-based TIA, the front-end provides an attenuation of 20 dB 20 MHz away from the RX band. The large signal handling capability of the receiver was tested measuring the 1dB in-band gain reduction versus blocker power (B_{1dB}) as a function of the blocker's frequency offset from the carrier (Fig. 7). At the band edge of 10 MHz the B_{1dB} corresponds to a 0.7 Vpp voltage swing at each TIA output. Up to 40MHz offset the measured B_{1dB} increases roughly by 12dB/octave, suggesting that compression is dominated by the 2nd order filtering of the TIA. Higher B_{1dB} could be achieved lowering the down-conversion gain. At larger frequency offsets the LNA limits the compression. Fig. 8 compares the measured and simulated NF over the signal bandwidth [1MHz; 10MHz]. The average measured NF is 3.84 dB. The receiver meets the B_{1dB}/N requirements for a 40 dB TX-RX isolation at an offset of 40MHz. An IIP3 of 13dBm has been measured using 2-tones at 2.08GHz and 2.157GHz with a 2 GHz carrier frequency. A summary of the measurement results and a comparison with state-of-the-art implementations is reported in Table I. The proposed solution improves the B_{1dB} for close-in blockers and has similar or lower NF compared with other LNA-first solutions. The B_{1dB} at $\Delta f/BW=2$ is comparable to mixer-1st solutions with similar gain. The difference in B_{1dB} compared to [3] is mostly due to the gain difference while compared to [8] is due to both lower gain and much larger offset frequency.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RECEIVERS

	This work	ISSCC'21 [7]	ESSCIRC'22 [8]	ISSCC'23 [10]	JSSC'18 [3]	JSSC'25 [9]	RFIC'24 [11]
Architecture	LNA-1st	LNA-1st	LNA-1st	Mixer-1st	Mixer-1st	Mixer-1st	Mixer-1st
Frequency [GHz]	1.5-3	0.4-3.2	1.9-2.1	0.25-2.5	0.2-8	1.2-7.2	0.4-2.6
RF BW (2BW) [MHz]	20	160	20	12-30	20	40	4-10
Gain [dB]	31.5	36	25	35	21	32	35
IIP3 [dBm] (Δf/RF_BW)	13 (4)	13 (2.5)	N/A	2 (1)	16 (1)	18-25 (1)	15.4 (2)
B1dB [dBm] (Δf/BW)	-10 (2)	-17 (2)	7 (8)	-13 (2)	0 (2)	-9 (2)	-10 (8)
NF (dB)	3.8	2.7-3.6	6	3.5-5.5	2.3-7.2	6.6-10	2.4-3.5
Static Pdiss (mW)	37	58.5	27	32-54	50	9.7	5-12
P_{LO} (mW/GHz)	10	17.5	10	N/A	30	2.7	3
Technology	CMOS 28nm	CMOS 40nm	CMOS 28nm	CMOS SOI 45nm	CMOS SOI 45nm	FDSOI 22nm	CMOS 55nm
Active Area [mm²]	0.6	0.6	0.5	0.65	0.22	0.22	0.29

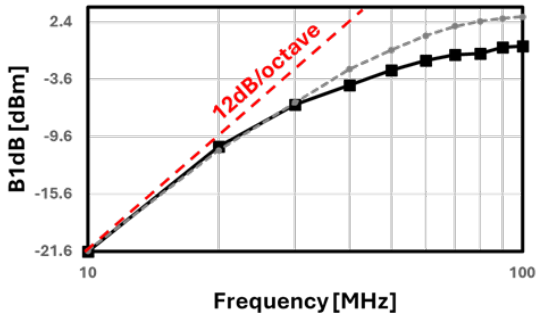

Fig. 7. Measured (solid) and simulated (dashed) B1dB

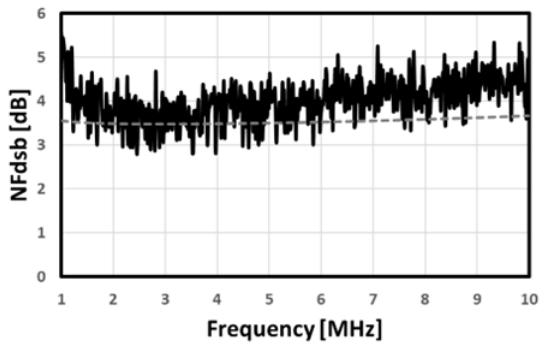

Fig. 8. Measured (solid) and simulated (dashed) NF

V. CONCLUSIONS

An auxiliary receiver for TX noise leakage cancellation in digital SIC architectures is proposed. Improved noise and blocker resilience at small frequency offset are achieved thanks to a second-order filtering TIA based on a single op-amp with a passive positive feedback network.

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