Ferroelectric Schottky Barrier FETs with a Metal Interlayer for Neuromorphic Applications

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***Abstract*—The integration of ferroelectric hafnium-zirconium oxide into field-effect transistors continues to pose challenges related to interface trap states and memory window stability. This work presents a metal-ferroelectric-metal-insulator-semiconductor structured Schottky barrier field-effect transistor designed for neuromorphic computing. By decoupling ferroelectric switching from the interfacial layer through a TiN floating gate, we demonstrate highly tunable, multi-state conductance. Transfer characteristics exhibit clockwise hysteresis with a threshold voltage shift of $\pm$1.4 V, while pulsed measurements reveal distinct long-term potentiation and depression characteristics suitable for synaptic weights. A combined physical model is proposed, attributing the device behavior to the interplay between remnant polarization and charge injection into the metal layer. Reliability assessments confirm functional endurance up to 10^6 cycles. These results validate the investigated devices as a viable candidate for hardware-based neural networks and non-volatile logic.**

***Index Terms*—Ferroelectric field-effect transistors, hafnium zirconium oxide, Schottky barrier FET, floating gate, synaptic devices.**

I. Introduction

The demand for high-density memory in artificial intelligence (AI) and neuromorphic computing has driven a resurgence in ferroelectric field-effect transistors (FeFETs) [1]. While hafnium-zirconium oxide (HZO) enables CMOS-compatible scaling below $10\,\mathrm{nm}$ [2] gate lengths, state-of-the-art FeFETs face trade-offs between memory window (MW), retention, and the HZO/interfacial layer (IL) stability [3]. The metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gate stack mitigates these issues by introducing a floating gate (FG), which decouples ferroelectric switching from IL interface traps and ensures uniform field distribution [4], [5]. TCAD simulations have demonstrated that this stack configuration is extremely promising for the realization of functional, highly-scaled ferroelectric devices, despite the drastically reduced number of ferroelectric domains, thanks to the interplay between the ferroelectric polarization and the charge in the metal interlayer [6].

Concurrently, ultrathin-body Schottky barrier (SB) FETs (SBFETs) offer a promising path for Beyond-CMOS and More than Moore applications by replacing doped junctions with metallic source/drain (SD) contacts and introducing intrinsic or lowly doped channels, thereby eliminating random dopant fluctuations [7], [8]. Integrating ferroelectric functionality into an SBFET (FeSBFET) creates opportunities for multi-state synaptic devices [9]–[12].

In this study, we present an MFMIS-structured FG-FeSBFET that addresses field uniformity issues. By combining charge tunneling into the FG with ferroelectric HZO switching, we demonstrate highly tunable device characteristics for synaptic weight modulation. We evaluate the underlying physical mechanisms through a systematic, detailed analysis of current flows within the proposed transistor, confirming domain switching and multi-state pulsed operation. Finally, we assess the endurance and retention of these devices, providing a strategy to mitigate trap-charge effects and improve stability in future non-volatile neuromorphic hardware.

II. Fabrication

The FG-FeSBFETs were fabricated on SOI wafers (20-nm lightly p-doped Si (B, $1 \times 10^{15}/\mathrm{cm}^3$) on 100-nm BOX). The Si mesa-structures (700 nm wide) were patterned via laser lithography and subsequent anisotropic Reactive Ion Etching under a SF_6/O_2 plasma. A $6\,\mathrm{nm}$ SiO_2 gate dielectric was formed by dry oxidation at $1173\,\mathrm{K}$ for $4\,\mathrm{min}$, followed by an in-situ N_2 post-oxidation anneal to reduce interface defects. The MFMIS gate stack was formed by first sputtering a $40\,\mathrm{nm}$ TiN layer and patterning the FG via wet-chemical etching in RCA-1 solution at $348\,\mathrm{K}$. A $10\,\mathrm{nm}$ ferroelectric HZO layer was then conformally deposited via ALD at $523\,\mathrm{K}$ using TEMAHf/TEMAZr precursors and H_2O oxidant, beginning with three ZrO_2 seeding cycles to promote lateral growth. A TiN top gate (TG) was deposited and patterned using the same sputtering and RCA-1 etch processes as described above. To induce the ferroelectric phase, the HZO was crystallized via RTA at $823\,\mathrm{K}$ for $120\,\mathrm{s}$ under N_2 atmosphere [13].

Finally, SD contacts were defined by removing HZO via Ar^+ sputtering and etching the underlying SiO_2 with buffered HF. Aluminum was then deposited via sputtering. The Schottky junctions were established via an Al-Si exchange reaction using RTA at $773\,\mathrm{K}$, resulting in monolithic crystalline Al replacing Si and forming an abrupt metal-semiconductor interface [14].

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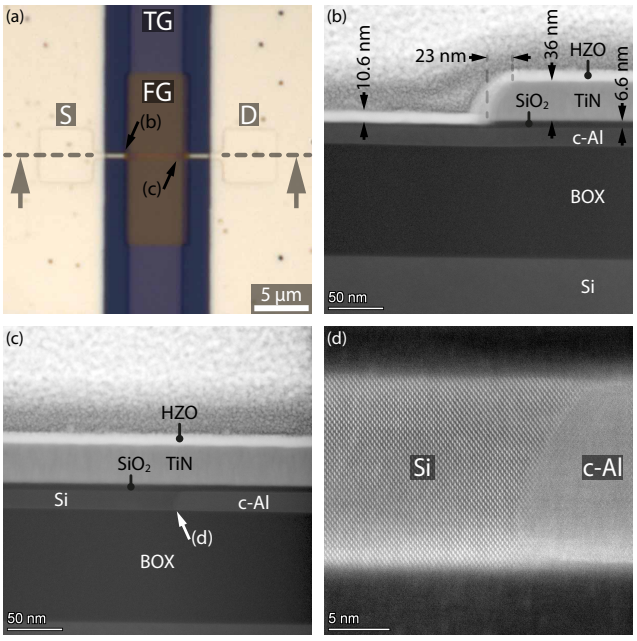

Fig. 1. (a) Optical microscope image with indicated TEM cut location (dashed line). HAADF STEM image of (b) floating gate edge, (c) gate stack over Schottky barrier, and (d) Si/Al interface.

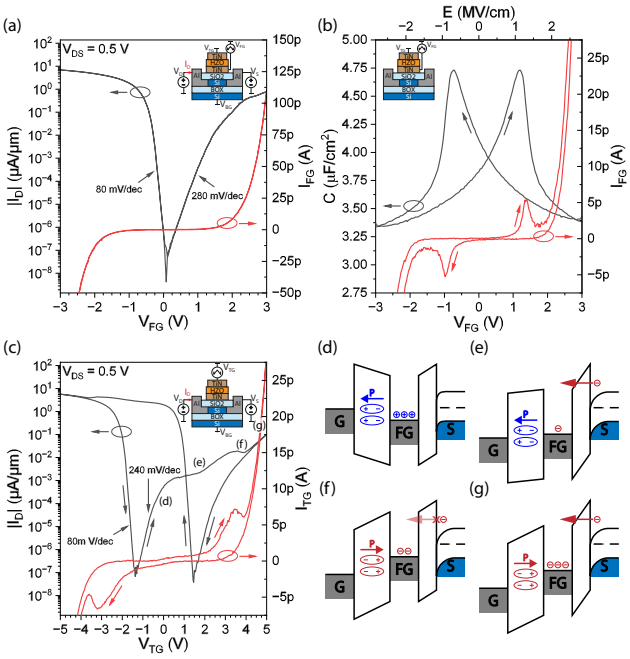

Fig. 2. (a) Transfer characteristic and TG leakage IV of SBFET reference structure with S_{th} values indicated. b) CV and IV measurements between FG and TG terminals creating an MFM capacitor. c) Transfer characteristic and TG IV of the fabricated FG-FeSBFET. Band structure of the gate-oxide stack. (d) Programmed state at 0 V. (e) High charge injection rate. (f) Injection is prevented by ferroelectric domain switching. (g) Extremely high voltages can cause further injection.

III. Results and Discussion

A. Structural Analysis

The relative dimensions of the fabricated device are evidenced by the optical microscope image shown in Fig. 1(a), which highlights the overlap between the FG and the TG. The image features the Al source/drain pads covering the rectangular regions of the etched Si mesa where the Al-Si diffusion process is initiated. Beneath the gate stack, a clear distinction can be made between the Al and Si regions of the exchanged portion of the layer. As the TiN color changes with increasing layer height, the TG and FG can be clearly distinguished in this 2D view.

A high-angle annular dark field (HAADF) scanning transmission electron microscope (STEM) image of the FG layer edge is shown in Fig. 1(b). As expected for purely chemical isotropic RCA-1 etching, a slope can be identified for the patterned TiN FG layer, yielding a sidewall slope of 0.6. The rounded edge is most likely connected to the performed reverse sputter. The impact of this process step is further evident in the reduced FG layer height and the reduced thickness of the SiO_2 not covered by the FG. Originally, the SiO_2 was 6.6 nm. The HZO is grown conformally around the FG, with an identical thickness throughout the layer of approximately 10.6 nm. Fig. 1(c) shows the gate stack overlapping the Schottky junction. When the Al diffuses into the Si layer, it forms crystalline aluminum (c-Al). The Si to c-Al interface is clearly visible and enhanced in Fig. 1(d). Here, the distinct Si atom columns are identifiable, highlighting the abruptness of the interface.

B. I-V Characteristics

We first analyze reference structures without HZO to understand the inherent charge transport and proceed to analyze the devices with HZO. Through dedicated access to the FG and TG electrodes, the CV performance of MFM stacks and the entire device IV characteristics can be explored with the same structures. Accordingly, first, the reference structure in Fig. 2(a) allows for direct FG contact, characterizing a standard single-top-gated (STG) SBFET without HZO interference. An ambipolar characteristic is observed, as typical for SBFETs with near midgap pinned Schottky barriers. Thus electron/hole injection dominates at $V_{FG} > 0\,\mathrm{V}$ and $V_{FG} < 0\,\mathrm{V}$ accordingly. As previously analyzed for Al-Si SOI SBFETs, transport depends on the interplay between thermionic emission (TE) and field emission (FE) of electrons and holes, which in turn depends on the band bending and thus the barrier height and width at the junctions. The device achieves eight orders of magnitude current modulation with subthreshold slopes (S_{th}) of $80\,\mathrm{mV/dec}$ and $280\,\mathrm{mV/dec}$ for holes and electrons, respectively. Importantly, gate leakage is small compared to the drain currents, highlighting the insulating properties of inter-gate and gate insulators.

Next, focusing on the device with HZO interlayer, capacitance-voltage (CV) measurements of the MFM stack can be performed by accessing both FG and TG. Fig. 2(b) shows a butterfly curve, validating ferroelectric switching. Current peaks at $-1.0\,\mathrm{V}$ and $1.4\,\mathrm{V}$ signify domain switching before the onset of soft dielectric breakdown. Using the HZO thickness of $10.6\,\mathrm{nm}$ and a measured capacitance of $3.3\,\mu\mathrm{F/cm^2}$ at $3\,\mathrm{V}$ ($E = 2.83\,\mathrm{MV/cm}$), ε_r is estimated at 39.

The FG-FeSBFET, featuring an isolated floating gate controlled by the top gate (Fig. 2(c)), exhibits clockwise hysteresis, shifting the baseline SBFET characteristics by approximately $\pm 1.4\,\mathrm{V}$. The device maintains eight orders of magnitude modulation, though the electron-dominated branch is two orders of magnitude lower than the test structure, likely due to enhanced trapping. Despite the significantly thicker gate stack, S_{th} remains stable at $80\,\mathrm{mV/dec}$ (holes) and $240\,\mathrm{mV/dec}$ (electrons).

Alike the explained CV measurement (Fig. 2(b)), the recorded TG IV measurement (red curve) of the FG FeSBFET in Fig. 2(c) features similar current peaks but translated into higher voltages, i.e. at $-3.1\,\mathrm{V}$ and $3.5\,\mathrm{V}$, pointing towards ferroelectric switching within the gate stack. The impact of the two domain-switching peaks can also be seen in the I_D current (black curve).

The observed transfer characteristics in Fig. 2(c) can be explained by the following model involving a combined mechanism of ferroelectric switching and charge injection. We define the net charge of the FG as $Q_{net} = P_{HZO} + Q_{ML}$, where P_{HZO} is the actual polarization charge within the HZO capacitor and Q_{ML} is the charge stored in the FG. This Q_{net} drives the threshold voltage shift via $\Delta V_{th} = Q_{net}/C_{TG}$. The schematic band diagrams of the stack cross-section in Fig. 2 correspond to the marked sweep points in Fig. 2(c). Starting with $V_{TG} = 0\,\mathrm{V}$ (Fig. 2(d)), we assume as an initial condition an upward HZO polarization and a positively-charged FG established by biasing V_{TG} to $-5\,\mathrm{V}$. The present Q_{net} induces a negative V_{th} shift, therefore explaining the observed electron accumulation in the channel.

Next, with a positive V_{TG} sweep, the strong gate coupling (α_{TG}) and remnant polarization in the HZO initially concentrate the voltage drop across the SiO_2 (Fig. 2(e)). This facilitates electron injection into the FG via field emission (FE), thereby displacing the FG potential. Once sufficient charge is injected into the FG, the HZO switches polarization downward (Fig. 2(f)), as supported by the I_{TG} current peaks. Accordingly, the electric field across the HZO increases, whereas the SiO_2 band bending is reduced. This ferroelectrically enhanced switching effectively self-limits further FE injection until higher V_{TG} values again allow FE, reaching the overcharging regime observed in Fig. 2(g).

C. Pulsed Measurements

The device's response to TG voltage pulses was investigated for neuromorphic applications. Fig. 3(a,b) show transfer characteristics after a $-5\,\mathrm{V}$ and $5\,\mathrm{V}$, reset pulse for $10\,\mathrm{ms}$, followed by an increasing number of set pulses (n_{set}) of

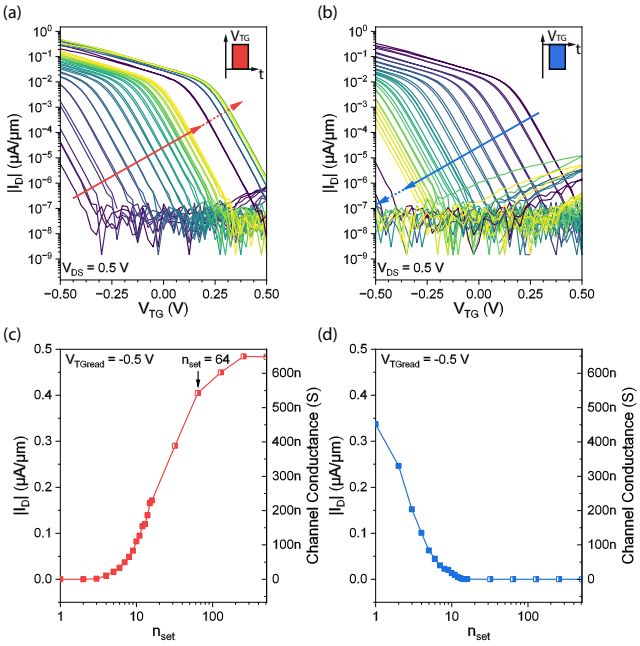

Fig. 3. Pulsed measurement with varying n_{set} pulse number. (a,b) Transfer characteristic in a limited V_{TG} range and marked regions indicating n_{set}. Transfers for positive (a) and negative pulsing direction (b). (c) LTP and (d) LTD graph for $V_{TGread} = -0.5\,\mathrm{V}$ extracted from the transfer characteristics.

$\pm 5\,\mathrm{V}$ with $0.5\,\mathrm{ms}$ duration. Cumulative positive/negative pulse durations up to $256\,\mathrm{ms}$ result in a progressive V_{th} shift towards positive/negative values, respectively. Extracted I_D values at a readout $V_{TGread} = -0.5\,\mathrm{V}$ yield the long-term potentiation (LTP) and depression (LTD) curves in Fig. 3(c,d).

Saturation of $|I_D|$ for the potentiation occurs after $n_{set} = 64$, corresponding to $V_{th,shift} \approx 0.6\,\mathrm{V}$. This represents the state in which sufficient FG charge injection triggers HZO switching (Fig. 2(f)). Further pulsing leads to the overcharging regime (Fig. 2(g)), where injection efficiency diminishes due to reduced SiO_2 band bending, causing the observed saturation in V_{th} shift. Conversely, due to the choice of V_{TGread}, depotentiation is stronger and saturates after 10 pulses.

The proposed model can be used to also explain the V_{th} shift discrepancy between pulsed (+0.6 V) and continous transfer (+1.4 V) measurements. The prolonged measurement time at $V_{TG} = \pm 5\,\mathrm{V}$ during continuous and comparatively slow DC sweeps facilitates sustained injection and deeper overcharging compared to millisecond pulses. This confirms that the device state is a sensitive function of both field magnitude and injection time.

D. Retention and Endurance Measurements

Device reliability was evaluated through endurance cycling and multi-state retention tests. Endurance was tested up to 10^6 cycles using bipolar pulses ($4\,\mathrm{V}/-4.1\,\mathrm{V}$, $10\,\mathrm{ms}$). LTP/LTD characteristics were recorded at each decade using $500\,\mu\mathrm{s}$

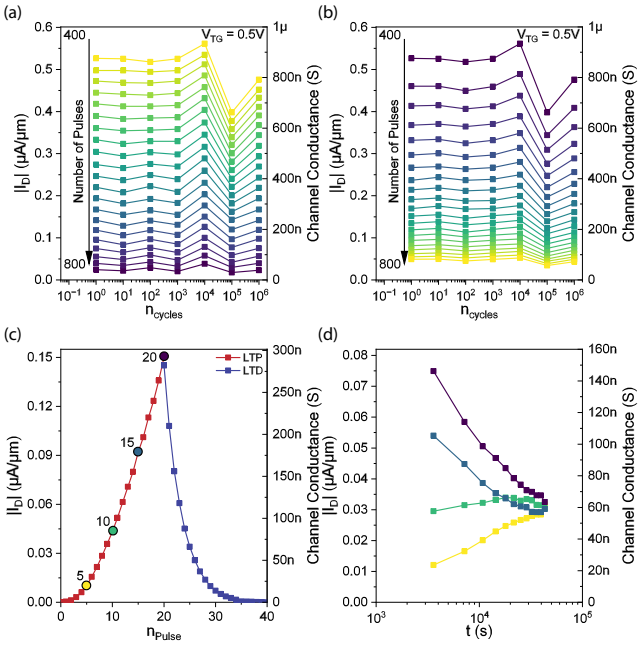

Fig. 4. (a) Endruance measurements up to 10^6 cycles, with LTP-characteristic performed at each decade. (b) LTD-characteristic. (c) Four equidistant conduction states highlighted in LTP/LTD-Characteristic and (b) hourly recorded retention of these states.

pulses (Fig. 4(a,b)). Outstandingly, the device maintains functionality throughout 10^6 cycles, with equidistant conduction states remaining measurable despite minor current fluctuations at 10^5 cycles, likely due to slight variations in the initial reset state. Stability is attributed to the floating gate concept, in which the ferroelectric response of all contributing domains is averaged and influences the FG potential.

Retention was characterized by monitoring four distinct conduction states, set by 5, 10, 15, and 20 pulses, over a 12-hour period (Fig. 4(d)). While the states are initially well-separated across the LTP/LTD range (Fig. 4(c)), the current levels converge after approximately 6 h. This limited retention suggests that while the MFMIS stack successfully decouples interface traps to enable high endurance and multi-state programmability, further optimization of the IL or HZO thickness is required to stabilize the stored FG charge for long-term non-volatile applications. Nevertheless, since the application in mind is not a long-term memory, synaptic weight action should not be hindered.

IV. Conclusions

In this work, we successfully demonstrated the integration of a TiN floating gate into an HZO-based Fe-SBFET architecture. The MFMIS gate stack ensures a homogeneous ferroelectric field acting upon the Schottky junctions and eliminates domain-related variabilities at the junctions as well as the HZO/SiO_2 IL. Our findings demonstrate that sweeping the TG voltage can produce clockwise hysteresis, resulting in a V_{th} shift of ± 1.4 V. In contrast, when pulsing the TG, only a shift of approximately 0.6 V can be attained. The devices we fabricated exhibited stable endurance of up to 10^6 cycles and maintained multiple distinct conductance states, fulfilling the primary requirements for hardware-based synaptic weights in neuromorphic networks. Although retention remains a challenge due to the specific thickness of the oxide interlayer used here, the clear LTP and LTD characteristics validate the FG-FeSBFET as a versatile candidate for non-volatile computing. Our proposed model of the physical mechanism reveals that the device characteristics are defined by the remnant polarization of the HZO and the magnitude of charge injected into the FG. This model indicates that scaling the surface-area ratio between the top gate and the floating gate provides a direct lever to tune the memory window and accelerate switching speeds.

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