A Learning-Enabled Predictive Digital LDO for Fast-Transient Capacitor-less Load Regulation

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***Abstract*—This paper presents an output capacitor-less digital low-dropout regulator (DLDO) incorporating a hardware-accelerated signature-hashing (HASH)-based predictive controller (PC) for recurring dynamic load currents (I_{LOAD}) in heterogeneous SoCs. This learning-assisted HASH-based PC introduces a paradigm shift from the reactive control of existing DLDOs to predictive regulation, achieving significantly reduced voltage droop (V_{DROOP}) and recovery time (T_R) for large ($\geq$124 mA) I_{LOAD} transients. Complementing the HASH-based PC, the proposed DLDO also incorporates sub-range binary search (SRBS) and fine linear control. SRBS performs a localized binary search around the last predicted operating point, enabling fast and stable voltage regulation, while the fine linear control improves steady-state performance in terms of voltage ripple and quiescent current. The proposed capacitor-less DLDO was fabricated in a 65-nm CMOS process and occupies an active area of 0.0404 mm^2. Measurement results demonstrate a T_R of 14 ns and a V_{DROOP} of 50 mV for a I_{LOAD} slew rate of 123 mA/ns at V_{DD} = 1.2 V and V_{OUT} = 1.15 V.**

***Index Terms*—Predictive control, HASH algorithm, fast-transient, sub-range binary search (SRBS), LDO**

I. Introduction

Modern computing platforms, particularly AI accelerators and heterogeneous SoCs, exhibit highly dynamic and repetitive load current (I_{LOAD}) profiles driven by spontaneous workload bursts [1]. These rapid load transients (ΔI_{LOAD}) impose stringent requirements on on-chip voltage regulators, demanding nanosecond (ns) response times (T_R) with minimal voltage droop (V_{DROOP}) and overshoot (V_{OS}) [1]-[3]. Digital low-dropout regulators (DLDOs) have been pivotal due to their scalability, low-voltage operation, and digital design flexibilities. However, conventional DLDOs [2]-[11], primarily based on coarse-fine control loops, governed by synchronous clocking (F_{CLK}) remain inherently reactive and suffer from power-speed trade-offs. To mitigate these trade-offs, designers often resort to large output capacitors (C_{OUT}) [3], [5], [9]-[11] or high-speed oscillators for V_{DROOP} reduction [2], [5] sacrificing area and quiescent current (I_Q). Recent advances such as adaptive-gain scaling [3], [6]-[7] and event-driven loops [8], [11] respond to ΔI_{LOAD} faster than conventional DLDOs, thereby downscaling the C_{OUT} to some extent. However, they share a fundamental limitation: they are purely reactive. For recurring ΔI_{LOAD} steps, as shown in Fig.1(a), these state-of-the-art DLDOs suffer from similar V_{DROOP} and T_R every single time as shown in Fig.1(a). These DLDOs treat each event as a unique disturbance, as no memory or learning mechanism exists to anticipate previously encountered load patterns. This limitation becomes increasingly critical in modern systems where workload-induced current transients are not random but exhibit temporal correlation and repetition. As a result, state-of-the-art DLDOs fail to exploit this predictability, leading to sub-optimal transient performance.

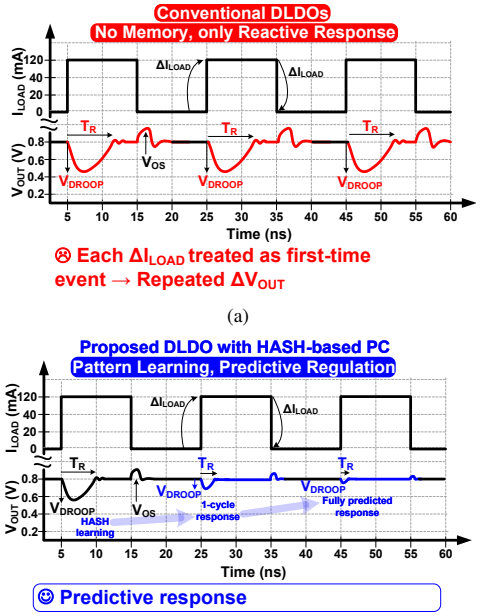

Fig. 1. Comparison of transient response to a repetitive ΔI_{LOAD}: (a) State-of-the-art DLDOs exhibit identical V_{DROOP} and T_R due to lack of memory, and (b) the proposed HASH-based learning-enabled DLDO identifies the ΔI_{LOAD} pattern and enables predictive and proactive response for subsequent ΔI_{LOAD}.

This paper introduces a paradigm shift from reactive control to predictive regulation. We propose the first DLDO regulator that leverages a hardware-accelerated signature-hashing (HASH)-based learning-enabled predictive controller (PC). Unlike coarse-fine [2],[5] or adaptive-gain loops [6]-[7] that merely adjust the gain, our HASH-based PC dynamically monitors regulated voltage (V_{OUT}) fluctuations to infer ΔI_{LOAD} variations and dynamically constructs a hash-based mapping

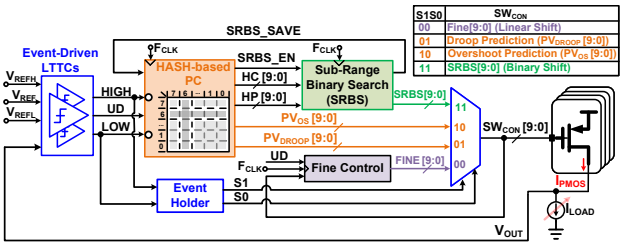

Fig. 2. Overall block diagram of the proposed capacitor-less DLDO.

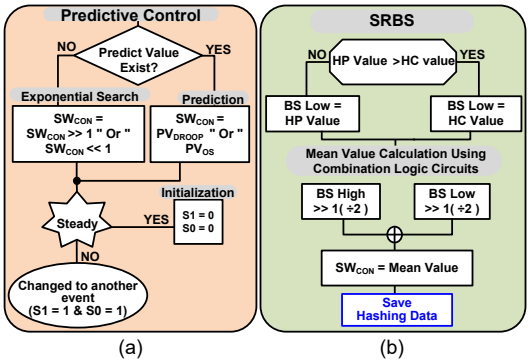

Fig. 3. Flow charts (a) HASH-based PC, and (b) SRBS control.

between transient signatures and optimal control actions. This mapping is stored on a learning table. Upon detecting a previously encountered ΔI_{LOAD}, as shown in Fig.1(b), the HASH-based PC retrieves the corresponding control pattern and proactively applies the required power transistor's drive strength instantly. This learning-enabled operation allows the proposed DLDO to achieve ns T_R with significantly reduced V_{DROOP}, and V_{OS} without using any C_{OUT}, effectively transforming the regulator from a reactive system into a predictive one. The proposed HASH-based PC introduces a new direction for intelligent power management, where on-chip regulators adapt and improve over time based on workload behavior.

II. Proposed Capacitor-less DLDO with HASH-based PC

Fig. 2 shows the overall block diagram of the proposed capacitor-less DLDO. The design comprises event-driven logic-threshold-triggered comparators (LTTCs), a HASH-based predictive coarse controller (HASH-based PC) with sub-range binary search (SRBS) algorithm, and a linear fine controller, driving a 10-bit PMOS power transistor array. The event-driven clock-less LTTCs continuously monitor V_{OUT} using three pre-defined voltage reference levels (V_{REFH}, V_{REF}, and V_{REFL}), and generate three digital signals (*HIGH*, *UD*, and *LOW*) corresponding to the V_{OUT} condition. The *UD* signal indicates whether V_{OUT} is above or below V_{REF}, while the *LOW* and *HIGH* signals flag V_{DROOP} and V_{OS} events, respectively. These event signals are processed by an event holder block, which determines the appropriate control action for the PMOS switch array, as shown in Fig. 2.

The proposed DLDO performs event-driven, memory-based voltage regulation by exploiting temporal conditions in I_{LOAD}

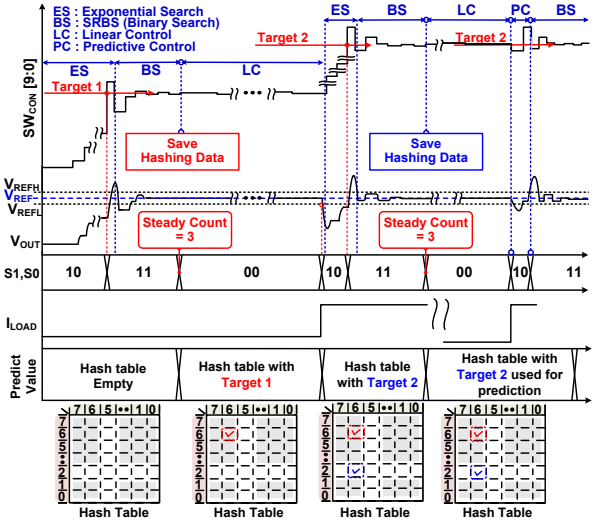

Fig. 4. Overall timing diagram of the proposed capacitor-less DLDO.

transients using: a HASH-based event mapping for predictive coarse control, and the SRBS algorithm for adaptive refinement. The HASH-based PC receives event indicators from the LTTC outputs (*HIGH*, *UD*, and *LOW*) and, in the absence of a stored prediction pattern, it initiates exponential search (ES) by exponentially shifting a single active bit to rapidly explore the required control range. Specifically, the HASH-based PC maintains a lookup table that maps transient events to optimal SW_{CON} codes, producing two 10-bit predicted control vectors (PV_{DROOP}[9:0] & PV_{OS}[9:0]), corresponding to V_{DROOP} and V_{OS}, respectively. These predicted codes are directly forwarded to the multiplexer (MUX) for rapid adjustment of the PMOS transistors in the case of recurring I_{LOAD} transients. The HASH-based PC also provides the current and previously applied switching codes, denoted as *HC*[9:0] and *HP*[9:0], respectively, along with an enable signal (*SRBS_EN*) to the SRBS block. Once the predictive adjustment is made, SRBS starts refining the PMOS control by performing a localized binary search (BS) around the last operating point, generating an updated 10-bit control code (*SRBS*[9:0]). Once the SRBS is done fine-tuning, V_{OUT} becomes approximately equal to V_{REF} and *UD* starts toggling, then SRBS state is saved, and fine control with linear search (LS) is activated to continue with the steady-state for voltage ripples (V_{RIPP}) and I_Q reduction. The control signals applied to the 10-bit segmented PMOS array are selected through a MUX with four inputs, based on the selection signals (S_1S_0) generated by the proposed event holder. This hybrid control strategy enables immediate, single-cycle predictive response through HASH-based PC for recurring events, while maintaining robustness through ES of hash-based PC and SRBS-based adaptation for previously unseen conditions.

Fig. 3 shows the flow charts of the proposed HASH-based PC and SRBS. As shown in Fig. 3(a), upon detection of a voltage transient event, the PC performs a predictive decision by querying the HASH lookup table. If a match is found, the corresponding SW_{CON} value is directly retrieved from the

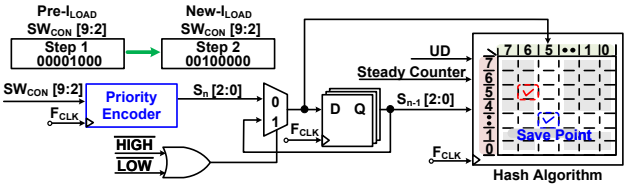

Fig. 5. Block diagram showing the HASH-based PC table update sequence.

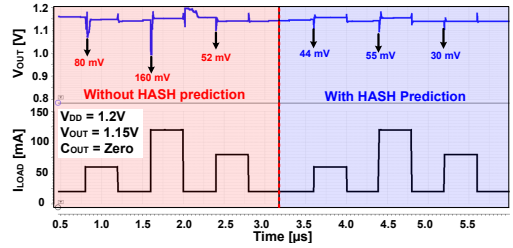

Fig. 6. Simulated load transient response comparison with and without using the proposed HASH prediction.

stored entries (PV_{DROOP} or PV_{OS}) and immediately applied to the PMOS array, enabling single-cycle regulation. In the absence of a match, the controller initiates an adaptive ES to determine the appropriate control action. Following the predictive or ES decision, the system evaluates whether $V_{OUT} \approx V_{REF}$. If the steady-state condition is satisfied, the fine loop maintains stable regulation. Otherwise, SRBS is activated as shown in Fig. 3(b). The SRBS operates using combinational logic to iteratively refine the SW_{CON} by narrowing the search range around the last operating point, enabling fast convergence with minimal latency.

Fig. 4 shows the overall timing diagram of the proposed DLDO, illustrating its transient response and HASH-based PC operation under dynamic I_{LOAD}. During the first load transient (Target 1), I_{LOAD} steps from low to high, causing V_{OUT} to drop below V_{REFL} and trigger the event-driven control sequence. Accordingly, the control state transitions (S_1S_0: 10→11→00) activate the coarse loop, in which the SW_{CON} is progressively updated via search-based regulation until V_{OUT} converges to the target level. Once steady-state is reached (S_1S_0:00), the corresponding optimal control code is stored in the HASH table as a signature associated with this transient event. For a subsequent identical I_{LOAD} (Target 2), the controller exploits the stored HASH entry to retrieve the optimal SW_{CON} directly. This predictive action bypasses the iterative search process and enables immediate application of the required drive strength, resulting in significantly reduced V_{DROOP} and faster settling. The evolution of the HASH table, illustrated in Fig. 4(bottom), highlights the learning process, where entries corresponding to different I_{LOAD} events are progressively stored and reused. This learning-enabled PC allows the DLDO to transition from an initial reactive response to a single-cycle predictive and proactive response for recurring I_{LOAD} conditions, thereby improving both transient performance and regulation efficiency.

Fig. 5 shows the block diagram for the HASH table update process for a new I_{LOAD} event. Upon a load current transition, the controller moves from the previous steady-state operating

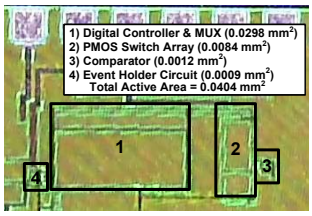

Fig. 7. Chip microphotograph with block-wise area description.

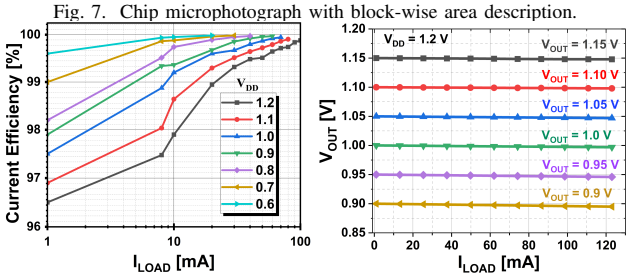

Fig. 8. Measured performance of the proposed DLDO: (a) current efficiency; (b) load regulation.

point (*e.g.*, SW_{CON}[9:2] = 00010000) to a new operating condition (*e.g.*, SW_{CON}[9:2] = 00100000), as shown in Fig. 5. A priority encoder extracts the most significant active bit (MSB-first) from the updated control word to generate a 3-bit address, S_n[2:0], which serves as the indexing key for the HASH table. Concurrently, the complementary event signals ($\overline{HIGH}$ and $\overline{LOW}$) propagate through a DFF-based sequence to determine the appropriate write timing and location within the HASH table. Once steady-state is achieved, the controller stores the corresponding PMOS SW_{CON} pattern at the computed HASH address, forming an event–response pair associated with the observed transient. This stored entry enables direct retrieval of the optimal SW_{CON} during subsequent identical load events, thereby facilitating predictive operation. As a result, the proposed HASH-based PC eliminates repetitive search phases and significantly improves T_R and V_{DROOP} for recurring I_{LOAD} variations.

To evaluate the effectiveness of the HASH-based PC, the transient response of the proposed capacitor-less DLDO was simulated at V_{DD} = 1.2 V, V_{OUT} = 1.15 V, under two operating conditions: with only proposed SRBS-based control (HASH disabled) and with HASH-based PC enabled. As shown in Fig. 6, the SRBS-based control alone achieves fast regulation, but it still exhibits noticeable V_{DROOP} due to its reactive search operation. By incorporating the proposed HASH-based PC, the optimal SW_{CON} is directly applied to recurring load events, effectively bypassing intermediate iterative search stages. As a result, the proposed approach significantly reduces V_{DROOP} as shown in Fig. 6.

III. Measurement Results

The proposed DLDO was designed and fabricated in a 65 nm CMOS process. Its chip micrograph, along with its area distribution are shown in Fig. 7. It includes neither an output nor a compensation capacitor while occupying an active area of 0.0404 mm^2. The proposed DLDO is designed to produce

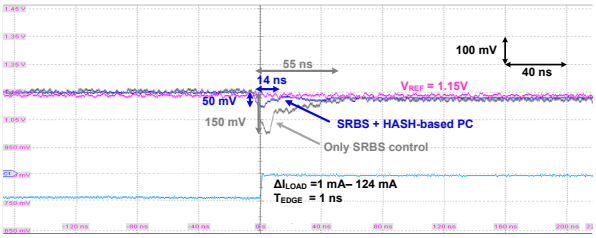

Fig. 9. Measured load transient performance using SRBS control with and without HASH-based prediction enabled to PMOS control.

V_{OUT} in the range of 0.55 V−1.15 V from a V_{DD} of 0.6 V−1.2 V, respectively. It operates at a steady-state F_{CLK} of 10 MHz, which is dynamically boosted to 250 MHz during load transients.

Fig. 8(a) shows measured current efficiency vs I_{LOAD} over the complete range of V_{DD} at F_{CLK} = 10 MHz. As shown, the proposed capacitor-less DLDO achieves the minimum and maximum current efficiencies of 96.5 % and 99.8 %, respectively. Fig. 8(b) shows the measured load regulation of the proposed capacitor-less DLDO at V_{DD} = 1.2 V. While driving the maximum I_{LOAD} of 124 mA, the proposed DLDO achieves 0.04 mV/mA of load regulation at V_{OUT} = 0.9 V.

Fig. 9 shows the measured load transient response of the proposed capacitor-less DLDO at V_{DD} = 1.2 V and V_{OUT} = 1.15 V, comparing two operating conditions: (i) proposed SRBS-based regulation only and (ii) SRBS with HASH-based prediction. As shown, for an I_{LOAD} step from 1 mA to 124 mA with T_{EDGE} = 1 ns, the proposed DLDO using only SRBS control exhibits a V_{DROOP} of 150 mV and a recovery time (T_R) of 55 ns, which is already quite competitive to existing DLDOs. With HASH-based prediction enabled, for the same I_{LOAD} step, the proposed DLDO directly applies the optimal SW_{CON} and reduces V_{DROOP} and T_R to 50 mV and 14 ns, respectively, demonstrating 66.66 % and 74.5 % improvement.

Table I summarizes the performance of the proposed DLDO, and its comparison with state-of-the-art DLDOs. The proposed DLDO outperforms other designs in terms of achieving better load transient performance (small V_{DROOP} & and T_R at large ΔI_{LOAD}) even without using an output capacitor. Furthermore, to fairly compare the overall load transient performance of all DLDOs, we used two figures-of-merit (FoMs), FOM_1 based on the edge-time (T_{EDGE}) of I_{LOAD} variations and a typical FOM_2. Based on these FOMs, the proposed DLDO clearly outperforms the existing DLDOs, achieving the lowest FOMs.

IV. Conclusion

In this work, we presented a capacitor-less DLDO with a HASH-based predictive controller (PC) for fast transient regulation under repetitive dynamic I_{LOAD} conditions. By exploiting temporal correlation in I_{LOAD} events, the HASH-based PC stores optimal PMOS switching patterns, enabling single-cycle predictive response for recurring transients. Combined with a sub-range binary search (SRBS) controller, the proposed DLDO transforms conventional reactive regulation into predictive, learning-enabled control. Measurement results demonstrate 50 mV V_{DROOP} and 14 ns T_R for a 1 mA to 124 mA I_{LOAD} step with 1 ns T_{EDGE}, without an external output capacitor.

TABLE I
Performance Summary and Comparison of the Proposed DLDO with State-of-the-Art Designs

Parameter	This Work	[2]	[3]	[4]	[5]
Process [nm]	**65**	65	65	40	65
Topology	**Digital / Predictive**	TDC	Digital	Digital	VCO-based
V_{DD} [V]	**0.6–1.2**	0.8–1.2	0.65–1.15	0.4–0.9	0.9–1.2
V_{OUT} [V]	**0.55–1.15**	0.7–1.1	0.6–1.1	0.3–0.85	0.5–1.1
$I_{LOAD,MAX}$ [mA]	**124**	105	16.3	250	19
C_{OUT} [nF]	**Free**	0.1	0.25	0.1	0.2
ΔV_{OUT} [mV] @ ΔI_{LOAD} [mA]	**50@123**	102@50	46@5.6	140@8.4	80@3
T_{REC} [ns] @ ΔV_{OUT} [mV]	**14@50**	3500*@50	50*@122	70@140	90@80
I_Q [μA]	**180–300**	80–323	80–1200	90–1340	131
T_{EDGE} [ns]	**1**	1000*	0.1	1	5
F_{CLK} [MHz]	**10–250**	N.A.	16–100	0.1	N.A.
Curr. Eff. [%]	**99.80**	99.88	98.59	99.74	99.3
FOM_1 [ps]	**0.7347**	800.33	30.05	23.21	342.06
FOM_2 [ps]	**0.0029**	0.326	29.34	17.85	233
Area [mm^2]	**0.0394**	0.045	0.0152	0.048	0.059

FOM_1 [ps] $= \frac{C_{\text{OUT}}\Delta V_{\text{OUT}} I_{\text{Q}}}{\Delta I_{\text{LOAD}}^2} + \frac{T_{\text{EDGE}} I_{\text{Q}}}{2\Delta I_{\text{LOAD}}}$,

FOM_2 [ps] $= \left(\frac{C_{\text{OUT}}\Delta V_{\text{OUT}}}{\Delta I_{\text{LOAD}}}\right)\left(\frac{I_{\text{Q}}}{\Delta I_{\text{LOAD}}}\right)$.

*Data is estimated from figures. In this work, $C_{\text{OUT}} = 0$; therefore, the total parasitic capacitance is estimated for FOM calculation ($C_{\text{PAR}} = 5$ pF).

V. Acknowledgment

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