A 224-Gb/s Linear TIA in 28-nm CMOS Co-Packaged with SiPh Photodiode

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***Abstract*—This paper presents a 224-Gb/s linear transimpedance amplifier (TIA) fabricated in a standard 28-nm CMOS process co-packaged with a silicon photonic photodiode. The low-bandwidth 3-stage front-end TIA employs Inverter-Gm for effective gain control. The S2D equalizer exercises single-to-differential conversion, differential phase alignment, and frequency equalization all at once. A voltage-aligned complementary cascade (VACC) is proposed to achieve large bandwidth, high gain, high linearity, and convenient DC coupling. The TIA achieves a transimpedance gain of 52.7-72.8 dBΩ, an O-E bandwidth of 52 GHz, and an input-referred noise density of 21.4 pA/√Hz while consuming 276 mW (1.23 pJ/bit).**

Keywords—CMOS, Trans-impedance Amplifier (TIA), Gain Control, Co-Packaged Optics (CPO), Linear Receiver

I. Introduction

The demand for high bandwidth and high data rates driven by generative artificial intelligence (AI) and large-scale computing clusters is pushing the lane signaling rate to 200 Gb/s+. For high-speed transmission, optical links have become the essential means for scaling the computing fabric in AI factories [1]. This technology imposes demanding requirements on the analog front-end circuits of optical receivers, including wide dynamic range, large bandwidth, low noise, and high linearity, all at low power consumption. In general, transimpedance amplifiers (TIAs) based on the SiGe process have become the mainstream and mature solution in 200-Gb/s links [2-3]. However, their disadvantages in power efficiency, cost, scalability, and the degree of integration with back-end CMOS digital cores are issues that AI factories wish to avoid. As a result, CMOS-based TIAs are becoming indispensable for next-generation high-speed optical receivers.

Most reported CMOS TIAs operate up to 112 Gb/s [4-6]. A CMOS optical receiver capable of operating at 226 Gb/s+ PAM-4 has been reported [7], yet with no circuit design details disclosed. In this work, we present a 224-Gb/s linear TIA implemented in a standard 28-nm CMOS technology, which overcomes the critical challenges associated with bandwidth, noise, and linearity performance without the need for more advanced and costly process. In addition, the TIA is co-designed, and 3D stacked on the silicon photonic (SiPh) photodiode, forming a 224-Gb/s receiver co-packaged optics (CPO).

II. Circuit Design

Fig. 1 illustrates the architecture of the optical receiver proposed in this paper. On the TIA RF path, the front-end (FE) stages are based on CMOS inverter (INV) using SVT

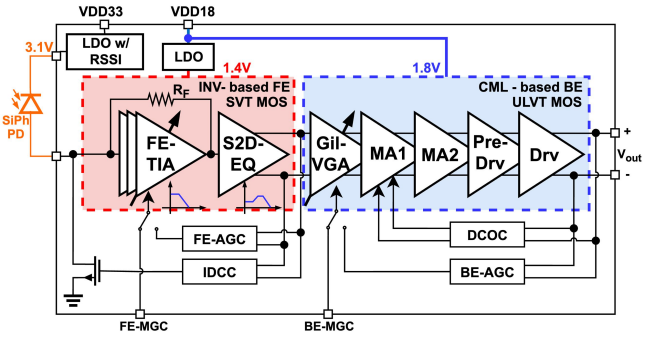

Fig. 1. 224Gb/s CMOS linear TIA architecture.

MOSFET, comprising a variable-gain FE-TIA and a single-ended to differential converter (S2D), biased at a supply voltage of 1.4V to achieve a large f_T [8]. The FE-TIA is designed with a partial bandwidth approach, which is then recovered by following S2D. This bandwidth scheme allows for a low-noise FE [9]. The FE-TIA adopts a 3-stage high-gain amplifier for high transimpedance gain. To meet the performance requirements of the FE over a wide input range, an inverter-G_m-based gain control circuit for FE-TIA is designed to maintain linearity. The S2D stage is designed to incorporate single-to-differential conversion, differential phase alignment, and frequency equalization altogether, forming an S2D equalizer (S2D-EQ). The Voltage-Aligned Complementary Cascode (VACC) is proposed and used to form the backend (BE) circuit, which comprises a Gilbert variable-gain amplifier (Gil-VGA), two main amplifier (MA) gain stages, a pre-output driver (Pre-Drv), and an output driver (Drv). Two independent automatic gain control (AGC) loops are equipped for both the FE and BE, respectively, to realize optimal gain control. The input DC cancellation (IDCC) and DC offset cancellation (DCOC) loops are utilized to draw the

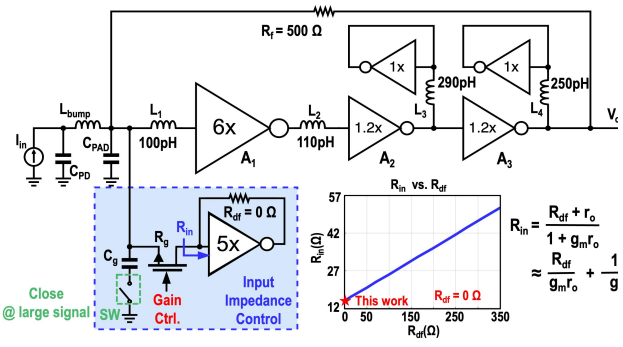

Fig. 2. Proposed three-stage TIA with gain control.

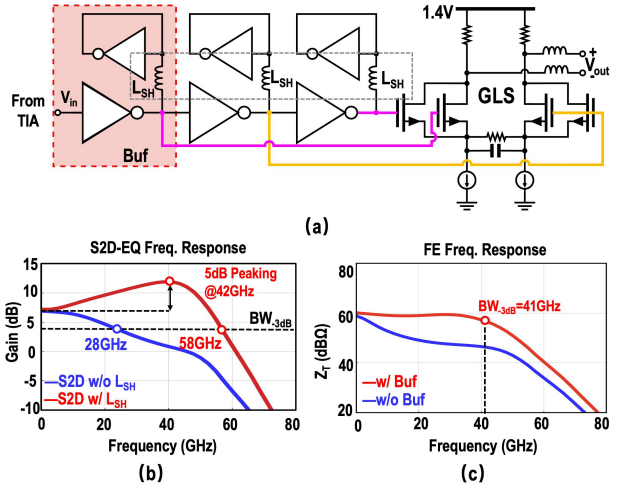

Fig. 3. (a) Architecture of the Proposed S2D-EQ; (b) Equalization capability comparison of the S2D-EQ; (c) Frequency response of S2D-EQ affected by Buf.

DC photocurrent and eliminate the offset, ensuring an aligned DC operating point. An LDO is employed to guard the supply for the single-ended FE. Another LDO featuring an integrated received signal strength indicator (RSSI) provides high-quality bias for the SiPh photodiode.

The variable-gain FE-TIA is shown in Fig. 2. To reach high gain, a three-stage amplifier-based TIA architecture is employed, which allows for the installation of a large feedback resistor (R_F) of 500 Ω. The first stage A_1 adopts a 6×-sized inverter to provide a large G_m for noise reduction as well as high gain. The two serial inductors L_1 and L_2 elevate the main pole at the TIA input and the amplifier main pole at the A_1 output. The subsequent two low-gain stages, A_2 and A_3 extend the bandwidth of the TIA core amplifier with the help of the two shunt inductors L_3 and L_4. For a wide input dynamic range, the gain control circuit in FE-TIA comprises a MOSFET variable resistor R_g and a dedicated inverter G_m unit to form a low-impedance path. At large signal input, the R_g is gradually turned on to steer part of the input signal current from the main TIA path into the inverter-G_m unit. Compared with the dummy TIA loading [4] for gain control, the proposed scheme realizes lower input impedance and enables a wider gain tuning range, evident in Fig. 2. This FE-TIA achieves a 10-dB transimpedance gain tuning range, from 53 dBΩ to 43 dBΩ. In the meantime, as the gain control circuit reduces the input impedance, the FE-TIA bandwidth also boosts undesirably, defying the bandwidth compensation scheme between the FE-TIA and the S2D-EQ. Therefore, a variable trimming capacitor C_g is inserted at the TIA input to compensate for bandwidth variations across different gain settings.

Fig. 3(a) shows the proposed S2D-EQ. We draw on the signal interpolation architecture proposed in [6] and present a G_m-linearized summer (GLS), which ensures consistent gain and bandwidth across both ends of the differential output while improving linearity. To realize the equalization in S2D, we introduce a three-stage shunt peaking based on a high-bandwidth G_m-G_m cell, and the S2D achieves 5 dB of peaking at 42 GHz, as shown in Fig. 3(b). Meanwhile, to reduce the loading from S2D seen by the TIA, an extra G_m-G_m stage is placed at the input of the S2D, which serves as the output

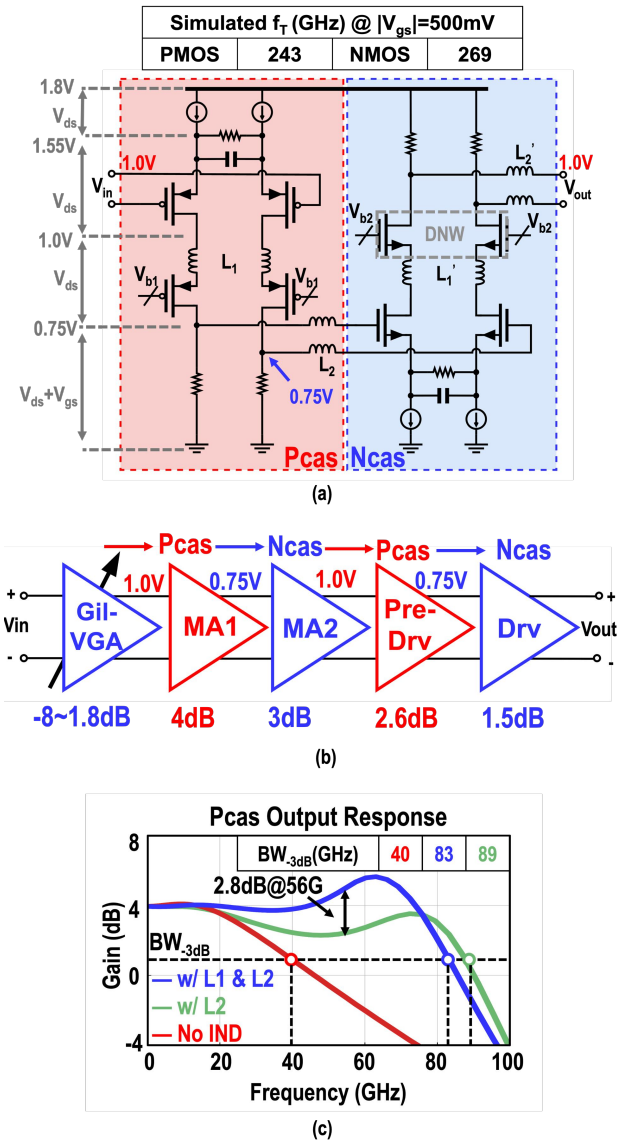

Fig. 4. (a) Proposed Voltage-Aligned Complementary Cascode (VACC) architecture; (b) Architecture of the BE; (c) Pcas frequency response.

buffer of the FE-TIA and extends the overall 3-dB bandwidth of the FE to 41 GHz, evident in Fig. 3(c).

The CML-based BE is employed to improve signal integrity and reject common-mode noise. However, conventional CML stages suffer from Miller capacitance, making it difficult to reach high bandwidth. In addition, the low supply voltage doesn't allow sufficient bias voltage to attain high transistor f_T. In light of this, we propose the Voltage-Aligned Complementary Cascode (VACC) to realize high gain, high bandwidth, as well as high linearity. Equally important, its aligned input-output common-mode voltage allows for easy multi-stage DC coupling. As shown in Fig. 4(a), the VACC comprises a Pcas stage and an Ncas stage, both with cascade transistors to shield the Miller capacitance for high bandwidth. Simulation confirms very close f_T between NMOS and PMOS transistors at 28 nm CMOS, which mitigates speed-related concerns. The Pcas shifts the voltage up while the Ncas shifts the voltage down, forming aligned DC voltages. The supply voltage is also elevated to

1.8 V to accommodate both the cascode transistor, sufficiently biased G_m transistors, as well as ample IR drop on the load for high gain.

To reach the high bandwidth, the peaking elements in VACC also need to work cohesively. As shown in Fig. 4(c), the RC degeneration network linearizes the G_m transistor, reduces its input capacitance, and compensates for the mid-band loss. The cascode transistor further reduces the input capacitance of the G_m transistor, which allows for high-frequency (70 GHz+) and high-Q peaking when resonates with serial inductor L_2/L_2'. Finally, the addition of another serial inductor L_1/L_1' resonates with the input capacitance of the cascode transistor and forms a mid-high frequency band peaking at 60 GHz+. Together, the Pcas achieves a bandwidth of more than 80 GHz and a gain of 4 dB.

The linearized Gil-VGA exercises gain control, providing another 10-dB dynamic range. The BE achieves a high gain of 14 dB and a total bandwidth as high as 70 GHz, with a peaking at 60 GHz. Combined with the FE's bandwidth of 41 GHz, the overall bandwidth of the entire chip is extended to more than 52 GHz.

III. Measurement Results

Fig. 5(a) presents micrographs of the fabricated TIA chip, which occupies a core area of 1.77×0.41 mm² and features a total of 29 compactly arranged inductors in the layout. The chip is powered by a 1.8 V supply with a measured operating current of 153 mA; the total power consumption, including LDO, is 276 mW. A 3D packaging scheme is adopted in this work: the electrical IC (EIC) is 3D flip-chip bonded to a photonic integrated circuit (PIC) that integrates a photodiode and RF output pads, and an optical fiber is edge coupled to the photodiode via a V-groove, forming the optical receiver front-end module.

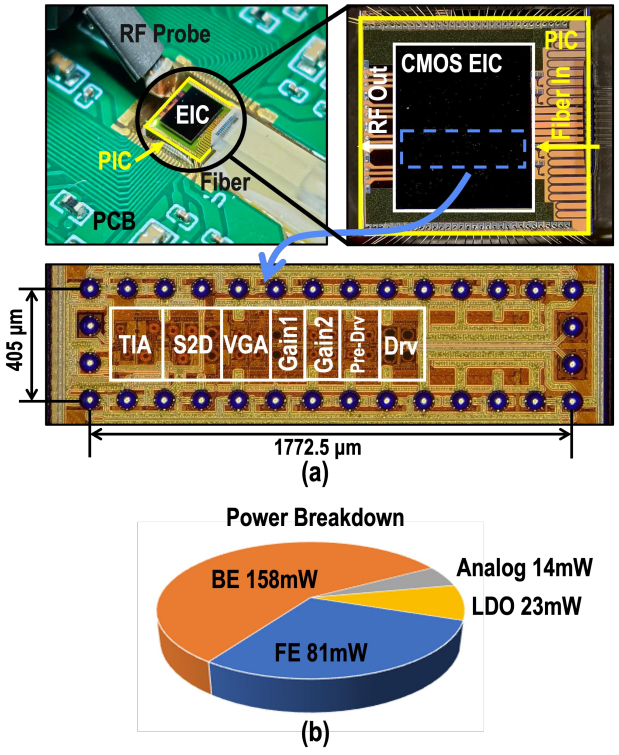

Fig. 5. (a) CPO and Die photo; (b) Power breakdown.

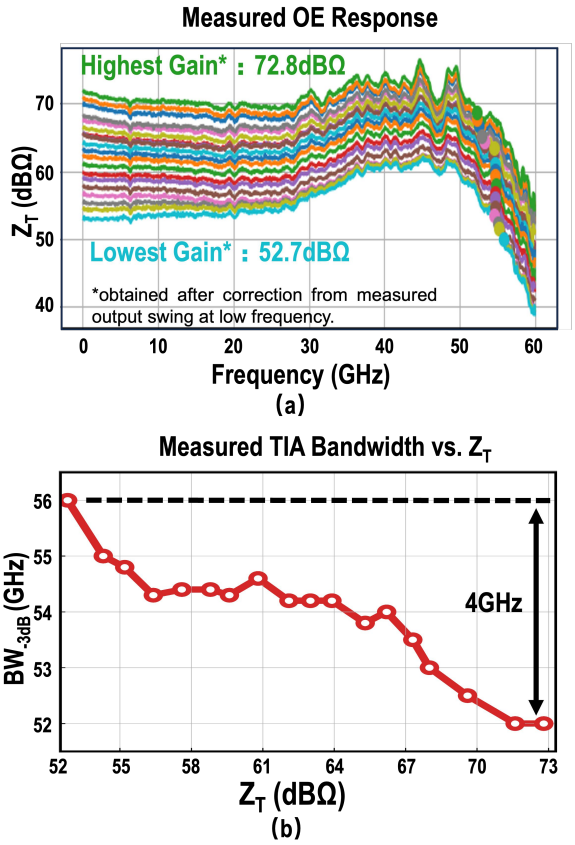

Fig. 6. (a) Measured OE response; (b) Measured TIA bandwidth vs. Z_T.

Fig. 6(a) presents the measured optoelectronic (OE) frequency response, showing a maximum transimpedance gain of 72.8 dBΩ and a minimum gain of 52.7 dB dBΩ, with bandwidth beyond 50 GHz. Fig. 6(b) summarizes the gain bandwidth relation under the gain control range, showing a bandwidth variation of only 4 GHz.

Fig. 7 illustrates the optoelectronic measurement setup based on a Keysight M8199B arbitrary waveform generator (AWG) and an N1046A sampling oscilloscope. The calibration reference planes have been extended to the tips of the optical probe and the RF GSSG probe, respectively. A 67-GHz Mach-Zehnder modulator (MZM) is used to generate the modulated laser. Fig. 8 presents the measured optical eye

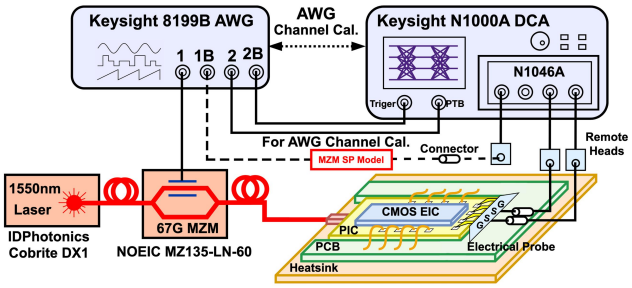

Fig. 7. Measurement setup

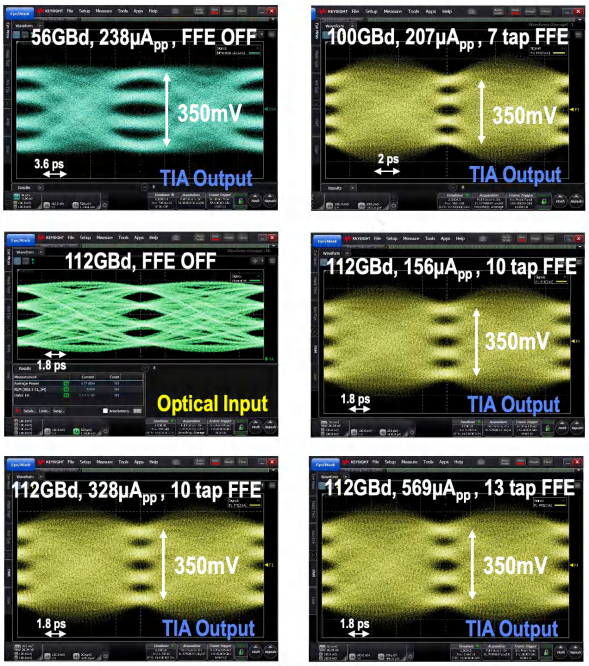

Fig. 8. Measured output eye diagrams.

diagrams. With feed-forward equalization (FFE) enabled, clear 112-GBaud PAM-4 eye diagrams are obtained for various input conditions.

Fig. 9 shows the measured total harmonic distortion (THD) with various input currents using R&S FSV3000 signal and spectrum analyzer and Arbitrary Waveform Generator (AWG) at 2 GHz, showing THD less than 3% at 1 mA_{pp}. The noise performance was characterized using a Keysight N1046A sampling oscilloscope. With the ambient noise subtracted, the measured output voltage noise amplitude is 21.3 mV, which translates to an input-referred noise density (IRND) of 21.4 pA/√Hz.

Table I comprehensively compares this work with recently reported high-speed transimpedance amplifiers for Intensity Modulation with Direct Detection (IMDD). The results show that this work doubles the data rate compared to similar CMOS-based TIAs, yet with less power consumption than SiGe implementations. Overall, this study successfully realizes a full-blown implementation targeting actual application and verifies the engineering feasibility of realizing

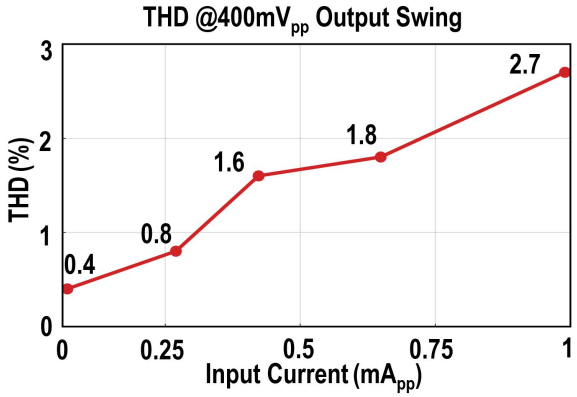

Fig. 9. Measured THD performance.

TABLE I. COMPARISON OF STATE-OF-THE-ART TIAS

	2025 JLT [2]	2024 CICC [4]	2023 JSSC [5]	2025 ISSCC [6]	This work
Technology	55 nm SiGe	22nm FDSOI	16nm FinFET	28nm CMOS	28nm CMOS
Supply (V)	2.5	1.8	0.9	1/1.2	1.4
Data rate (Gb/s)	256	112	112	112	224
BW (GHz)	62	28	32	29.5	52
Max Zt (dBΩ)	76.8	74	63	62	72.8
Min Zt (dBΩ)	N/A	47	54	<52	52.7
THD (%)	N/A	<4@Ipp= 2.5mApp	<8@Ipp= 670μApp	<5@Ipp= 450μApp	<3@Ipp =1mApp
Power (mW)	500	155	77	68.2	276
IRDN (pA/√Hz)	N/A	11	16.9	16	21.4
Power Efficiency (pJ/bit)	1.95	1.38	0.69	0.61	1.23

a 224-Gb/s linear TIA in planar CMOS technology, with a balanced trade-off among bandwidth, gain, noise, and linearity with reasonable energy efficiency.

IV. CONCLUSION

This paper successfully demonstrates a 224-Gb/s variable-gain, linear transimpedance amplifier (TIA) fabricated in a standard 28-nm planar CMOS process, with an input-referred noise density (IRND) of 21.4 pA/√Hz, and its energy efficiency is 1.23pJ/bit. Realized in a CPO chiplet, its balanced overall performance demonstrates the promising application potential in high-speed optical interconnects for future AI factories.

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