A 5–20 V Input Reconfigurable Series-Parallel Charger for Dual Batteries of Arbitrary Capacity

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***Abstract*—This paper presents a high-efficiency 5-20V input charger for dual-battery systems in foldable smartphones. The design adopts a passive-stacked third-order buck topology that leverages cable inductance to reduce the primary inductor current while maintaining a full 0–1 voltage conversion ratio (VCR). A reconfigurable series-parallel operating mode is proposed to simultaneously enhance charging efficiency and achieve passive voltage balancing between two batteries with arbitrary capacity ratios, requiring minimal additional loss. Fabricated in a 0.18 µm BCD process, the charger achieves a peak efficiency of 95.3% when charging two identical batteries and maintains 93.8% efficiency even under a 3:2 charge allocation ratio, supporting up to 20W output power.**

***Keywords*—Battery charger, dual-battery charging, fast charging, passive-stacked third-order buck, series-parallel reconfiguration, cable inductance, voltage balancing**

I. Introduction

In recent years, the rapid advancement of foldable smartphones has led to the widespread adoption of dual-battery configurations. However, due to space constraints and component interference, the two batteries often exhibit mismatched capacities. Furthermore, the Universal Serial Bus Power Delivery (USBPD) standards support higher input voltage and charging current. As shown in Fig.1, the primary inductor (L_P) in conventional buck chargers carries the full charging current (I_{CH}), requiring a bulky inductor with high current capability. The large input capacitor (C_{IN}) is also required to handle discontinuous input current (I_{IN}).

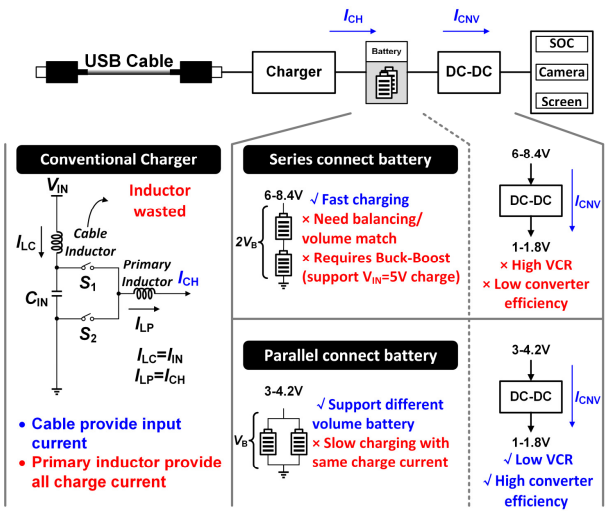

Fig. 1. Issues in conventional chargers.

While some prior works have sought to reduce C_{IN} and L_P by leveraging the cable inductance (L_C), the proposed topologies severely constrain the achievable VCR [1-3]. It prevents them from supporting both the commonly used 5V USB input voltage (V_{IN}) and the higher V_{IN} required for fast charging.

For dual-battery applications, a series connection halves the charger output current (I_{CH}) for the same charging power, thereby enhancing charging efficiency by reducing conduction losses, as illustrated in Fig. 1. However, this approach introduces significant design trade-offs. Firstly, the elevated stack voltage reduces the efficiency of the downstream DC-DC converter powering the system loads (e.g., processors) [1]. Secondly, it necessitates either stringent battery capacity matching or complex active-balancing circuitry [1-4]. Finally, because the total stack voltage often exceeds the standard 5V USB input, a buck-boost capability is required for the charger [2]. Conversely, a parallel connection avoids these issues but imposes a high VCR on the charger when operating from high V_{IN}, thereby compromising efficiency.

II. Proposed Charger

The proposed charger, as illustrated in Fig. 2 (a), employs a passive-stacked third-order buck topology [5] to regulate V_{B2P}. It utilizes the cable inductor (L_C) without adding extra passive components. Fig. 2 (b) demonstrates that this design maintains the full 0-1 VCR while reducing the primary inductor current (I_{LP}) to $I_{CH} - I_{LC}$, achieving a 30-90% reduction in the operating range and thus significantly shrinking the inductor's volume. Concurrently, the cable current (I_{LC}) remains equal to the input current (I_{IN}), eliminating the need for an input capacitor (C_{IN}).

As shown in Fig. 2 (c), a reconfigurable series-parallel charging mode is proposed to leverage the advantages of both configurations when the input voltage (V_{IN}) exceeds 9V. Under these circumstances, the batteries are connected in series for charging to narrow the V_{IN} to V_{B2P} gap, while a single battery is used to power the downstream converters, preserving high converter efficiency. When a voltage imbalance occurs due to unequal battery capacities, the charger switches to a parallel connection, enabling passive cell equalization through the internal battery resistance. Because these series-parallel transitions occur at a much lower frequency than the main switching frequency (F_{SW}), the associated switching losses are negligible. Furthermore, as shown in Fig. 2(d), the charge-sharing loss (P_{CS}) decreases as the voltage difference between the batteries diminishes. Unlike the single-shot balancing after charge completion [4],

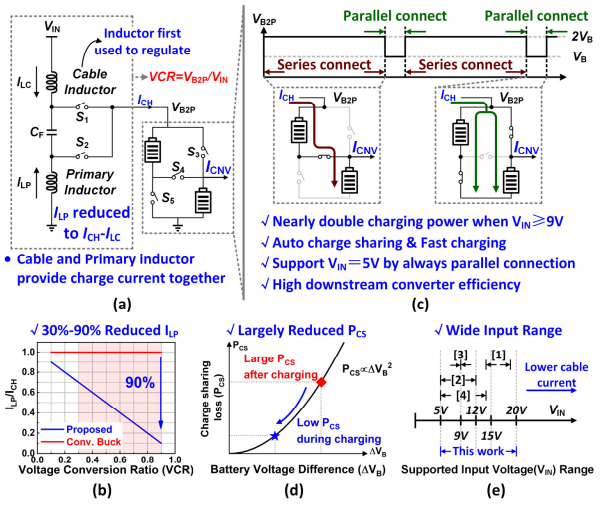

Fig. 2. (a) The proposed charger, (b) I_{LP} / I_{CH} reduction comparison. (c) series-parallel operating mode. (d) Charge sharing loss vs ΔV_B. (e) V_{IN} range comparison.

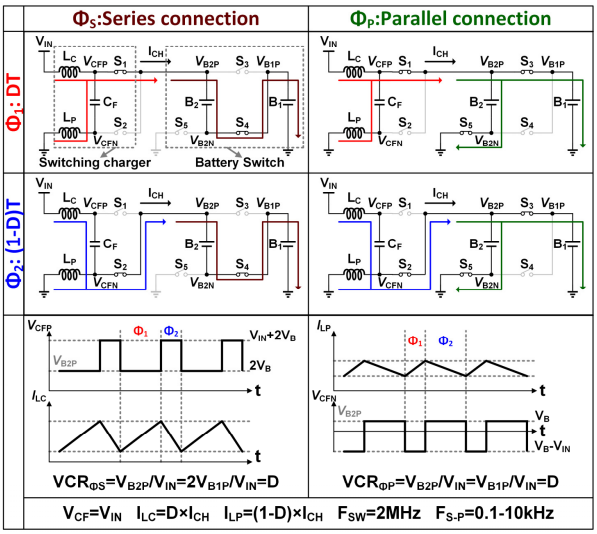

Fig. 3. Operating principle of the proposed charger.

this approach offers progressive balancing with minimal voltage difference. Finally, the parallel mode supports direct 5V input charging, enabling the proposed design to cover a wide V_{IN} range from 5V to 20V. As compared in Fig. 2(e), this work achieves the widest V_{IN} support among state-of-the-art designs, making it efficient for both low- and high-voltage scenarios.

A. Operational Principles

Fig. 3 illustrates the operating principle of the proposed charger. In phase 1 (Φ_1), the positive terminal of the flying capacitor C_F (V_{CFP}) connects to V_{B2P} via switch S_1, energizing L_C and L_P while C_F is discharged to the V_{B2P} by I_{LP}. In phase 2 (Φ_2), V_{B2P} connects to the negative terminal of C_F (V_{CFN}) via switch S_2, de-energizing L_C and L_P as C_F is charged by I_{LC}. The duty cycle of Φ_1 is D. During Φ_1, the voltage across L_C is $V_{LC} = V_{IN} - V_{B2P}$, and during Φ_2, $V_{LC} = -V_{B2P}$. By applying the volt-second balance, VCR = V_{B2P}/V_{IN} = D. Since C_F is connected in parallel with V_{IN} through L_C and L_P constantly, the average V_{CF} equals V_{IN}. Φ_1 and Φ_2 alternate at F_{SW} of 2 MHz. Because I_{LC} provides a direct path to V_{B2P}, the I_{LP} is reduced from I_{CH} to (1-D) I_{CH}. Regarding the battery configuration, during Φ_S, V_{B2P} is twice the battery voltage ($2V_B$), with equal charging currents $I_{B1} = I_{B2}$. In Φ_P, V_{B2P} voltage is V_B, two batteries share charge through S_3 S_5, and the series-parallel switching frequency ($F_{S\text{-}P}$) is in the order of several kHz.

B. System Architecture

Fig. 4 shows the overall system architecture. Switches S_1 and S_2 are implemented with 24V MOSFETs to withstand a maximum V_{IN} of 20V, while switches S_3, S_4, and S_5, which control the series-parallel connection of the two batteries, utilize 5V MOSFETs. The system adopts peak current-mode control by sensing I_{LP}, featuring a proposed adaptive slope control by sensing I_{LP}. To accommodate the different D in Φ_S and Φ_P, the circuit dynamically tunes the compensation slope to maintain consistent I_{LP} peak values across both phases. and prevent subharmonic oscillations. The system utilizes a constant-current constant-voltage (CC-CV) charging method to regulate V_{B1P}. A series-parallel controller monitors the

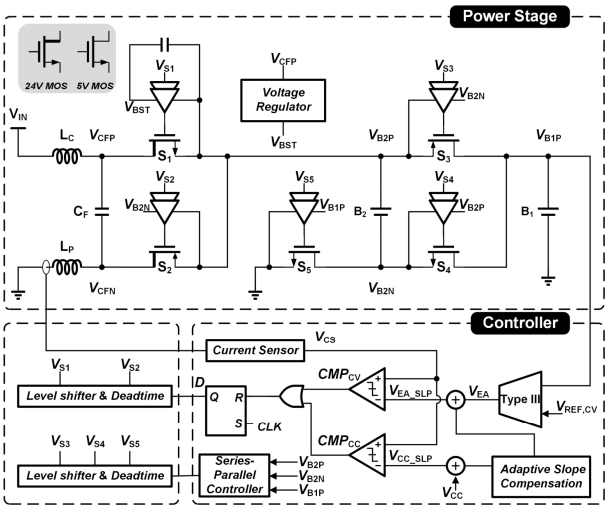

Fig. 4. System block diagram of the proposed charger.

battery voltage difference (ΔV_B) to manage battery connection states. By closed-loop adjusting the Φ_S and Φ_P switch frequency, the system ensures batteries are predominantly charged in series for high efficiency, while avoiding excessive ΔV_B to minimize charge-sharing losses.

C. Two–Battery Series–Parallel Controller

Fig. 5 presents the series-parallel controller and the two-battery charging process. V_{B1} and V_{B2} refer to the voltage of the two batteries. The battery differentiator senses ΔV_B via a resistor array [6] to set I_{GM}, controlling the time for V_{BDA} to reach V_{TH} and thus adjusting the Φ_P entry frequency. Two battery differentiators are adopted to indicate the absolute value of $|V_{B2} - V_{B1}|$, regardless of which V_B is higher. The Parallel Timer enforces a fixed parallel duration for charge balancing. A large ΔV_B increases I_{GM} to shorten the series duration and induces a higher hard-charge current to progressively reduce ΔV_B toward V_{DF}.

D. Circuit Implementation and Waveform of the Controller

As shown in Fig. 6 (a), the current sensor employs DCR to detect I_{LP}, level-shifts it from a negative voltage V_{CX} to near V_L, and amplifies the voltage via DDA feedback resistor. The slope compensation circuit, shown in Fig. 6 (b),

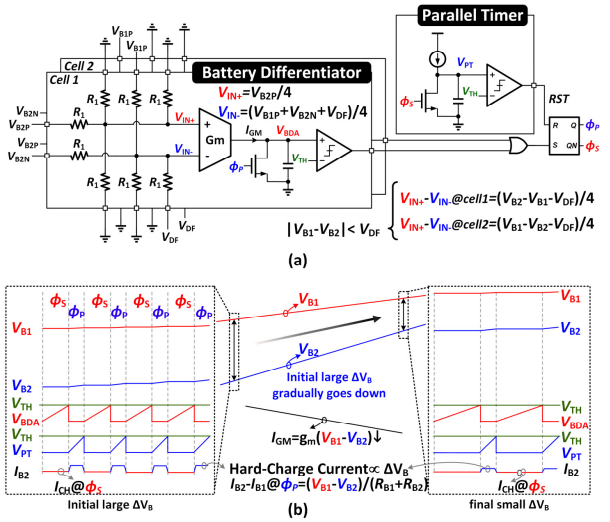

Fig. 5. (a) Two batteries Series–Parallel controller and (b) waveform of the two batteries charging process.

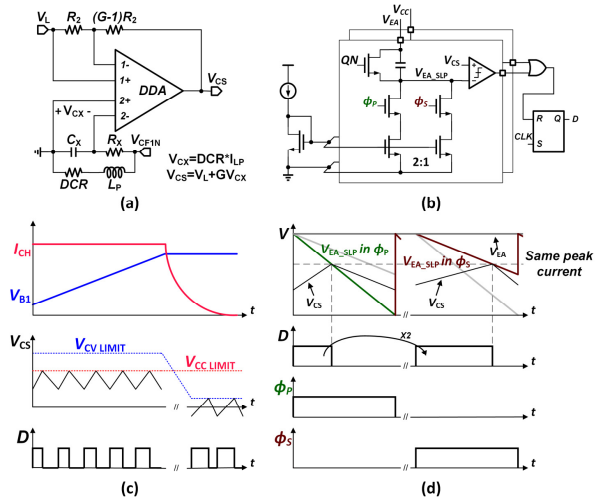

Fig. 6. (a) Schematic of current sensor, (b) schematic of slope compensation, (c) waveform of CC-CV mode transition, (d) Comparison of slope compensation between Φ_P and Φ_S.

generates the compensated signal V_{EA_SLP} by drawing a current from V_{EA}. In Φ_P, the discharge current is set to twice that of Φ_S. This ensures that when D doubles from Φ_P to Φ_S, V_{EA_SLP} and V_{CS} intersect at the same voltage level, thereby maintaining the same peak current limit, as illustrated in Fig. 6 (d). Additionally, Fig. 6 (c) demonstrates the CC-CV transition, where the system shifts from CC to CV operation via the lower current limit between V_{CV} and V_{CC}.

III. Measurement Results

The proposed charger was fabricated in a 0.18μm BCD process. Fig. 7 shows the photos of the chip and the PCB. The flying capacitors (22μF×2, 0805 package) and the primary inductor (4.7μH, 89-mΩ DCR, 1210 package) were selected to reduce the charging current ripple. An on-board cable inductor (1μH, 22-mΩ DCR, 1210 package) with an inductance value similar to that of a 2-meter USB cable was used for testing.

Fig. 8 (a) presents the measured steady-state waveforms with a discrete inductor at 5V V_{IN} parallel connection, while V_B is 3.3V, I_{LP} is reduced by 66% compared to conventional

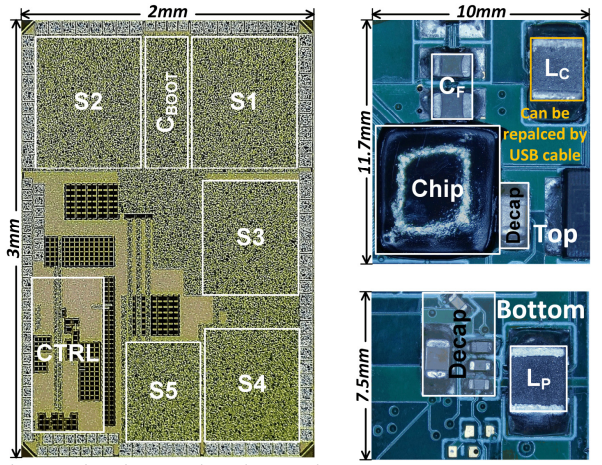

Fig. 7. Die micrograph and PCB photo.

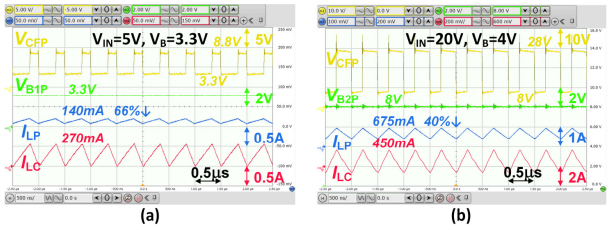

Fig. 8. Measured steady-state waveforms in (a) parallel connection using a discrete inductor; (b) series connection using a 2m USB cable replacing L_C.

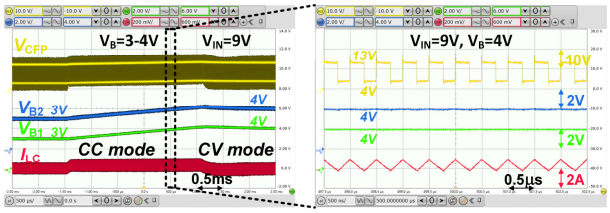

Fig. 9. Measured the transition from CC to CV mode under force parallel charging.

chargers. Fig. 8 (b) shows the steady-state waveforms with a 2-meter USB cable at 20V V_{IN} in series connection, where I_{LP} is also reduced by 40%.

Fig. 9 demonstrates the CC to CV mode transition waveform in parallel connection. Fig. 10 illustrates the battery charging and voltage balancing process. A 3:4 capacity ratio was used to emulate two batteries of different capacities. During the CC mode, a higher I_{CH} was supplied. The charger switches to parallel charging mode more frequently to balance the voltages of the two batteries. In the CV mode, the lower I_{CH} reduced the rate of the increase of ΔV_B, and the $F_{S\text{-}P}$ decreased. Fig. 10 (c) shows the voltage profiles of both batteries during CC mode. The two batteries are gradually charged up while maintaining a small ΔV_B to prevent large P_{CS}.

Fig. 11 and Fig. 12 present the measured efficiency for 3:2 and 1:1 battery volume ratios, respectively. For the 3:2 mismatched scenario, the peak efficiency is 93.8% excluding the L_C loss, as shown in Fig.11(b). Fig.12(b) depicts a higher peak efficiency of 95.3% for the 1:1 case without L_C loss. Table I summarizes the performance. This work features the widest V_{IN} range (5–20V), utilizes the cable inductor, enables voltage balancing during series charging, supports arbitrary battery capacity ratios, and achieves up to 20W output power.

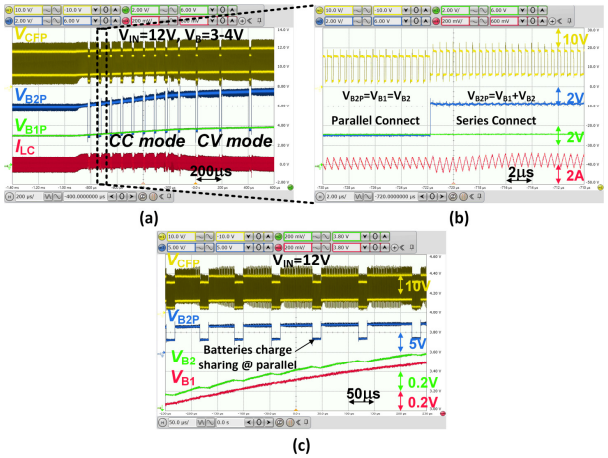

Fig. 10. Measured waveforms for two batteries with a 3:4 capacity ratio: (a) overall charging and balancing process, (b) detailed view of Φ_P to Φ_S transition, and (c) Voltage profiles of individual battery voltages during the process

TABLE I. Comparison with prior arts

Work	ISSCC'19 [3]	ISSCC'22 [4]	VLSI'23 [2]	ASSCC'24 [1]	This Work
Process	130nm BCD	130nm BCD	180nm BCD	180nm BCD	**180nm BCD**
Battery connection	Series	Series-Parallel	Series	Series	**Series-Parallel**
Topology	Hybrid step-down	Buck/Direct	Hybrid step-up/down	Switch capacitor	**Hybrid step-down**
V_{IN}	9 V	5-13.7 V	5-12 V	14-18.5 V	**5-20 V**
F_{SW}	2.3 MHz	1.6 MHz / -	0.5-0.8 MHz	0.66 MHz	**2 MHz**
Peak P_{OUT}	27.4 W	87 W *	29.6 W	29.5W	**20 W**
Chip Area	7.37 mm^2	32.33 mm^2	6.76 mm^2	5.2 mm^2	**6 mm^2**
Peak Efficiency	97%	99.2% *	97.23%	97.5%	**95.3% / 93.8% ****
Battery to Downstream Converter Voltage	6-8.4 V ***	3-4.2 V	6-8.6 V ***	6-8.6 V	**3-4.2 V**
Utilize the cable Inductor?	Yes	No	Yes	No	**Yes**
Voltage balance during charging process?	No	Yes (Unidirectional)	No	No	**Yes**
Support arbitrary battery capacity ratio?	No	No	No	No	**Yes**

* USB programmable power supply (PPS) in direct charging mode
** Q_{B1}:Q_{B2} = 3:2
*** Compared with dual batteries configuration

IV. Conclusion

The proposed charger combines a passive-stacked third-order buck topology with a battery series-parallel structure, supports a wide 5-20V V_{IN} range charging dual batteries with arbitrary capacity ratios. By narrowing the V_{IN} to V_{B2P} gap through series connection, the charger significantly enhances efficiency when the V_{IN} exceeds $2V_B$. Simultaneously, it ensures voltage balancing between the two batteries during charging, reducing charge-sharing losses caused by post-charging voltage balancing. Moreover, the primary inductor current is reduced by utilizing cable inductance. The prototype chip achieves a peak efficiency of 95.3% for identical batteries, and 93.8% for a 3:2 capacity ratio. delivering up to 20W output power.

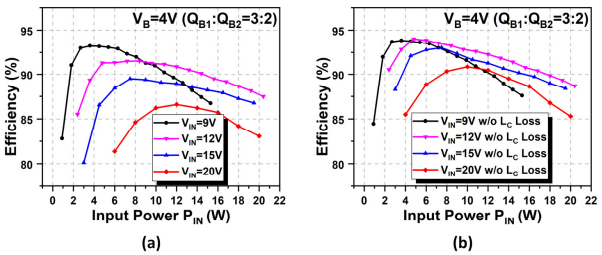

Fig. 11. Measured efficiency of the proposed charger when charging two batteries of a 3:2 volume ratio (a) with the L_C Loss (b) without the L_C Loss.

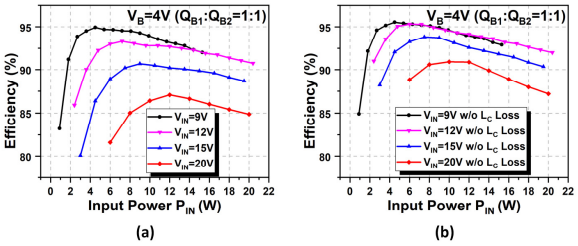

Fig. 12. Measured efficiency of the proposed charger when charging two batteries of the same volume (a) with the L_C Loss (b) without the L_C Loss.

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