An Autonomous Computational Current-Booster Chiplet for Fast Droop Mitigation and Universal Compatibility in 3D-IC Vertical Power Delivery

Renwei Chen[1], Xuchen Men[1], Zhoutong Liu[1], Yunxin Wang[1], Xuliang Wang[1], Junxiang Xu[1], Jingshu Yu[2], Rongmei Chen[3], Jin Wei[3], Jianshi Tang[1], Yan Wang[1] and Xiaosen Liu[1]
[1]Tsinghua University, BNRist, Beijing, China, [2]Intel Corporation, Hillsboro, Oregon, [3]Peking University, Beijing, China

***Abstract*—This paper presents an autonomous computational current-booster (ACCB) integrated with an on-package voltage regulator (OPVR) for ultrafast transient regulation in 2.5D/3D-IC vertical power delivery (VPD) platforms. The proposed in-situ ACCB dynamically reconfigures flying capacitors to generate voltage headroom and provide bidirectional transient current injection and absorption, and is validated in a system integrated with an on-package switched-capacitor voltage regulator. By locally quantizing PDN dynamics and computing actuation strength for current mismatch supplement, the booster demonstrates flexibility for cooperation in power delivery with arbitrary OPVRs. The prototype achieves a 79.6% droop reduction under a 0–20 A with 40-ns load step, with the best reported transient FoMs of 1.53 nF/A and 0.076 nF/A².**

***Keywords*—ACCB, droop suppression, current tracking, universal compatibility, vertical power delivery.**

I. Introduction

Large-scale HPC processors such as System-on-Wafer eXtreme (SoW-X) platforms and backside power delivery network (BSPDN) technologies impose unprecedented challenges as thermal design power (TDP) exceeds 10 kW and aggregate load current slew rates reach the kA/µs scale [1], [2], making fast transient response a critical bottleneck for system efficiency and performance. Conventional on-board VRMs offer high efficiency but suffer from limited bandwidth due to bulky inductors and their physical distance from XPU cores, even with transient speed-up techniques [3]. Fully integrated voltage regulators (FIVRs) improve locality through advanced packaging, yet their operating frequency and efficiency remain constrained by current-sensing bandwidth and inductor slew rate [4]. Digital linear voltage regulators (DLVRs) provide nanosecond transient response as a critical path in on-package voltage regulators (OPVRs), at the cost of an additional high-voltage supply, bump overhead, parasitic inductance, and stability constraints. Nevertheless, DLVR-dominated designs degrade steady-state efficiency due to their inherently linear operation [5]–[8].

To address these issues, this paper presents an autonomous computational current-booster (ACCB) chiplet that augments a multistage modular switched-capacitor voltage regulator cascaded with a continuously scalable conversion-ratio regulator (MMCSCR) chiplet, forming a monolithic VPD system (Fig. 1) for HPC processors. Two key innovations are highlighted. First, the ACCB droop-mitigation scheme asynchronously reconfigures flying capacitors to bidirectionally boost or sink transient current, leveraging elevated voltage headroom and established sink path to discriminate di/dt severity. Second, the ACCB introduces a new transient-regulation paradigm for versatile OPVR architectures by proactively quantizing complex PDN impedance and computing the optimal supplemental current

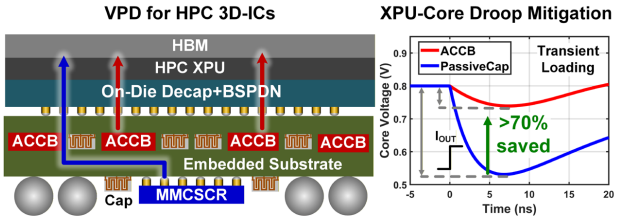

Fig. 1. ACCB–MMCSCR system enabling VPD, with transient droop mitigation enabled by ACCB for 3D HPC processors.

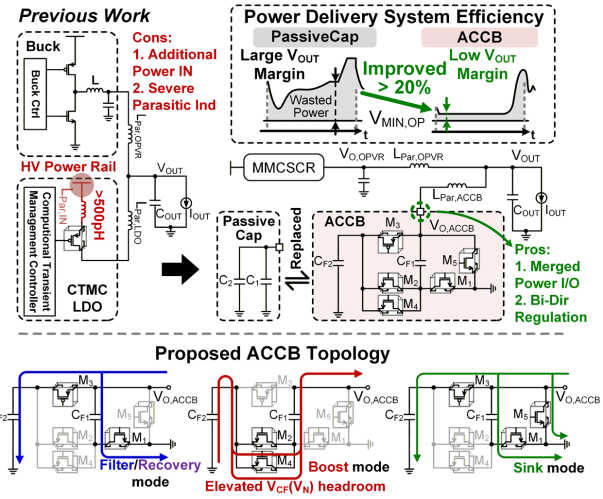

Fig. 2. Comparison of prior hybrid architectures with the proposed ACCB–MMCSCR system, highlighting ACCB system-level efficiency gains and its operating principle featuring elevated headroom V_N.

for arbitrary workload profiles with minimal ripple. Compared with the PassiveCap baseline, the proposed ACCB achieves a 79.6% droop reduction from 232 mV to 49 mV under a 0–20 A load step within 40 ns, and attains the best reported transient figures-of-merit (FoMs) of 1.53 nF/A and 0.076 nF/A².

II. ACCB Topology for Transient Droop Suppression

The proposed ACCB-MMCSCR system eliminates bulky inductors and enables VPD for HPC platforms, as shown in Fig. 1. The compact ACCB is integrated to provide transient enhancement using reconfigurable on-package capacitors, forming a short vertical path to the cores, while the MMCSCR serves as a high-efficiency, fine-grained OPVR mounted on the substrate top side. Compared with a baseline where the MMCSCR employs an equal package area of passive decoupling capacitors (PassiveCap), this scheme delivers >70% droop reduction at the cores under transient loading. By exclusively leveraging capacitive energy storage, the system transcends the transient limitations of inductor-based architectures, enabling fundamentally faster load response.

Fig. 2 shows the prior hybrid buck–LDO design where the LDO clamping relies on an additional high-power rail with

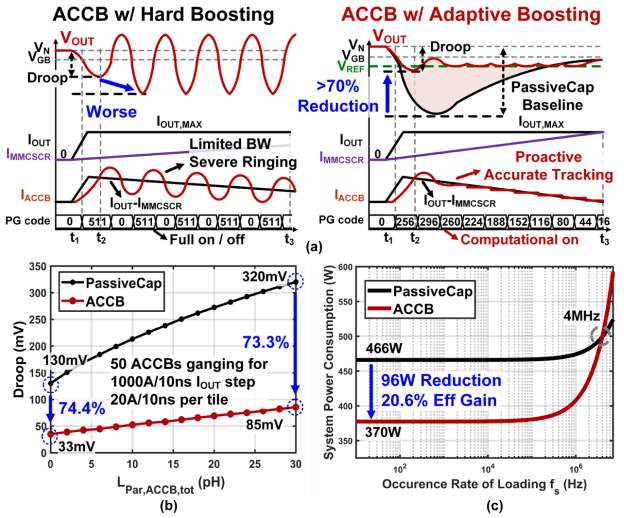

Fig. 3. (a) Droop comparison between PassiveCap baseline, ACCB with hard and adaptive boosting. (b) Droop reduction under 1000-A loading vs. the total output parasitic inductance $L_{Par,ACCB,tot}$. (c) System power reduction vs. occurrence rate of 1000-A load-transient event f_s.

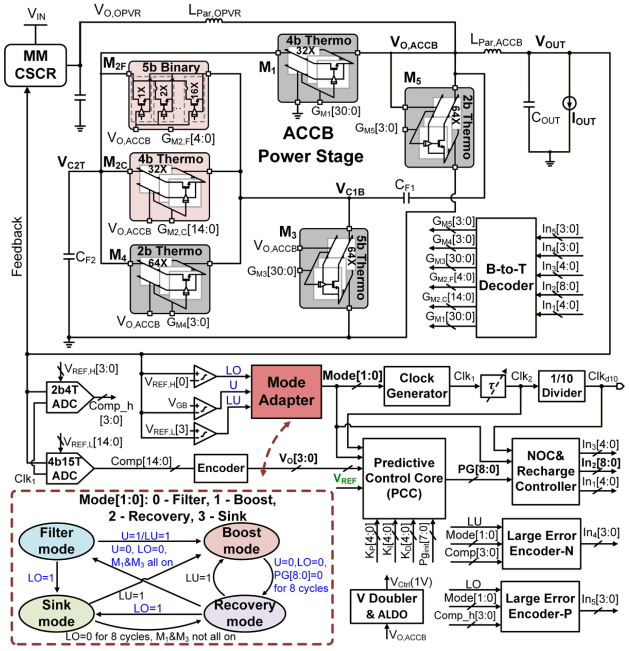

Fig. 4. Overall architecture of the proposed event-driven ACCB.

large (>500 pH) parasitic inductance. In contrast, the ACCB merges power input and output (I/O) via reconfigurable switched-capacitor paths to enable bidirectional current boosting and sinking with reduced parasitic inductance, allowing integration in the substrate/RDL close to the XPU cores. Replacing PassiveCap with ACCB lowers the required voltage margin above the output-stage minimum operating voltage $V_{MIN,OP}$, reduces the steady-state load operating voltage and improves system-level efficiency by over 20%.

The ACCB operates in four modes with segmented power gates $M_{1\text{-}5}$ for current drive strength tuning. In Filter and Recovery modes, M_1 and M_3 are fully and partially turned on, respectively, to connect the C_{F1} and C_{F2} in parallel for passive decoupling and supply noise suppression. In Boost mode, the C_{FS} are reconfigured in series with the main power gate M_2 turned on, elevating their effective voltage from the normal operating voltage V_N to $2V_N$ at $V_{O,ACCB}$ node, providing an

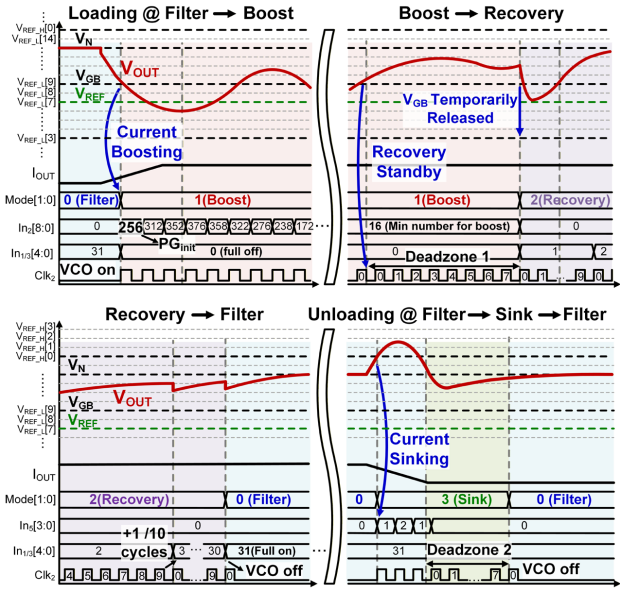

Fig. 5. Event-driven adaptive mode transitions during a complete load transition event for computational boost/sink current regulation.

additional headroom of V_N for rapid current injection to arrest droop. M_4 is conditionally turned on to provide an additional charge injection path for suppressing severe droop. In Sink mode, M_1, M_3 and M_5 are turned on, configuring the C_{FS} in parallel while M_5 forms a discharge path to absorb excess charge to ground, suppressing severe voltage overshoot.

Fig. 3 shows that the ACCB supplies supplementary current when V_{OUT} drops below the guardband level V_{GB}, leveraging elevated voltage headroom V_N, proactively suppressing the dominant droop by over 70% relative to PassiveCap across a wide range of total output parasitic inductance in a ganged system with 50 ACCBs under a 1000-A, 10-ns load step, where each ACCB handles a 20-A, 10-ns loading. During the droop-mitigation process, hard boosting induces ringing due to parasitic-limited bandwidth, whereas computational adaptive boosting modulates the active power tails of M_2 by quantizing the voltage error between V_{OUT} and V_{REF} and its temporal evolution using accumulated state history and predicted error trends. This enables precise tracking of the mismatch between I_{OUT} and I_{MMCSCR}, stabilizing V_{OUT} at a reference V_{REF} below V_{GB} and preserving voltage headroom for I_{MMCSCR} ramping. Under a maximum 1000-A transient load, the ACCB-enabled system exhibits a power crossover point with the PassiveCap baseline at a loading event rate of 4 MHz. Below this rate, it significantly reduces system power by 96 W from 466 W to 370 W at low event rates through V_{GB} reduction and achieves up to 20.6% efficiency improvement for practical HPC processor specifications.

III. System Implementation and Design Details

Fig. 4 presents the ACCB's architecture with a segmented power stage and hybrid control scheme. M_2 is partitioned into coarse ($15\times M_{2C}$) and fine ($31\times M_{2F}$) tiles for glitch-free, programmable current control, while M_1/M_3 employ 32-tile thermometer-coded segmentation for fine-grained filtering strength tuning. Large-sized M_4/M_5 tiles introduce nonlinear boost/sink paths to handle severe undershoot and overshoot. An event-driven controller asynchronously detects voltage excursions and synchronously computes control actions, enabling adaptive switching among four modes. V_{OUT} is

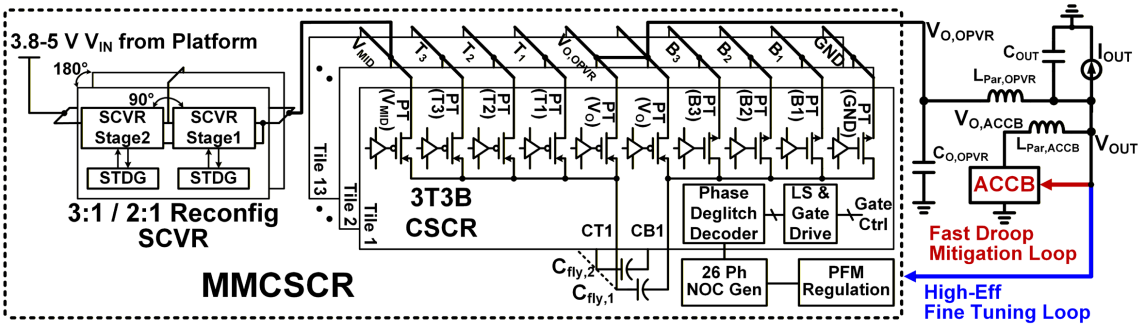

Fig. 6. Overall architecture of the ACCB-MMCSCR power delivery system with dual-loop synergetic regulation.

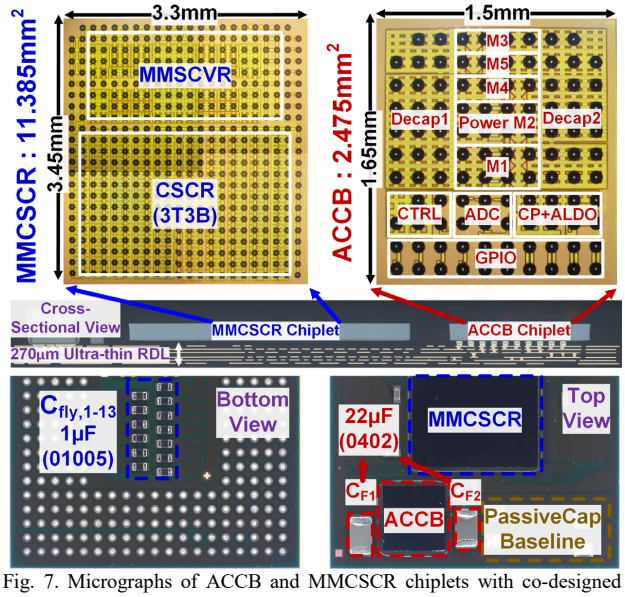

Fig. 7. Micrographs of ACCB and MMCSCR chiplets with co-designed substrate and 2.5D/3D optimization.

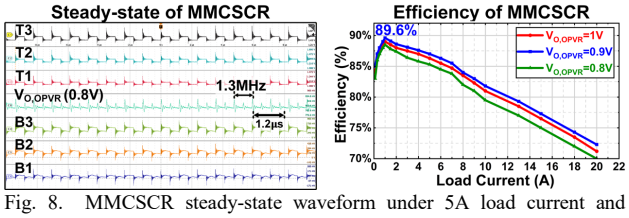

Fig. 8. MMCSCR steady-state waveform under 5A load current and measured power conversion efficiency with 5V input.

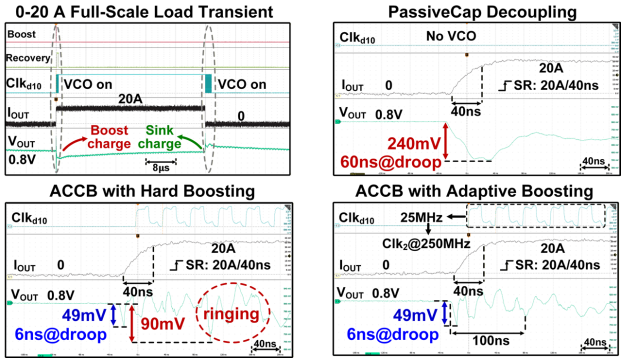

Fig. 9. Measured load-transient responses under passive decoupling and ACCB regulation with hard boosting and adaptive boosting.

quantized by a dual-rail ADC, and a predictive control core (PCC) dynamically determines the required M_2 tail activation based on sampled voltage error. The large error encoders N/P compare V_{OUT} with multiple low-level references $V_{REF,L}[3:0]$ and high-level references $V_{REF,H}[3:0]$ to selectively enable M_4 and M_5 tiles, providing large-signal charge injection and absorption to suppress severe undershoot and overshoot, respectively. An on-chip voltage doubler and DLDO generate V_{Ctrl} for controller power supply, eliminating the need for external bias supplies.

Fig. 5 shows the event-driven mode transitions during a complete load transient event. From Filter mode, undershoot asynchronously triggers the VCO, enabling synchronous Boost operation where M_2 injects current until V_{OUT} recovers toward V_{REF}. When V_{OUT} exceeds V_{GB} and $In_2[8:0]$ falls below the preset minimum threshold of 16 for eight consecutive cycles, the system enters Recovery mode to gradually recharge the capacitors with a temporarily released guardband to avoid false re-triggering. After recharging, it returns to Filter mode and disables the VCO. During load release, overshoot triggers Sink mode to discharge excess charge, and the system returns to Filter conditioned on sustained in-range V_{OUT} to prevent mode chatter.

Fig. 6 shows the complete MMCSCR employing a two-stage architecture, consisting of a 2:1/3:1 SCVR for initial step-down from 3.8–5 V to 1.6–1.9 V, followed by a 3T3B CSCR for low-voltage, high-current regulation. The MMCSCR provides high-efficiency, fine-grained $V_{O,OPVR}$ regulation, with transient droop suppression further assisted by the ACCB's fast tuning at the core stage.

IV. Fabrication & Measurement Results

The proposed ACCB and MMCSCR chiplets were fabricated in 65-nm CMOS, occupying 2.475 mm² and 11.385 mm², respectively (Fig. 7). The MMCSCR employs thirteen 1-µF flying capacitors, while the ACCB integrates two 22-µF flying capacitors on the 270 µm ultra-thin interposer with 3060 A/cm³ volumetric current density. Capacitors with equal area are used as PassiveCap references for fair comparison. A 20-A load transient is implemented with a single ACCB to emulate the behavior of 1000-A processor workloads using an on-board OptiMOS. Fig. 8 shows the steady-state waveforms of the MMCSCR nodes $V_{O,OPVR}$, T_1–T_3, and B_1–B_3 at a switching frequency of 1.3 MHz with I_{OUT} = 5 A. The measured conversion efficiency versus load current exhibits a peak efficiency of 89.6%.

Fig. 9 shows the full-scale waveform of a 0–20 A load transient in the proposed ACCB–MMCSCR system. The ACCB is asynchronously activated for boost and sink during loading and unloading events, with predefined mode transitions ensuring fast and stable operation. Under a 0–20 A full-scale load step, the ACCB reduces the first droop from 240 mV to 49 mV, achieving 79.6% suppression. While hard boosting and adaptive boosting provide the same first-droop

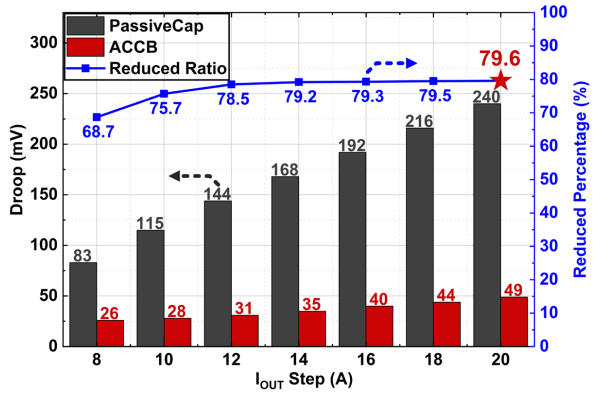

Fig. 10. Comparison of voltage droop for ACCB and PassiveCap versus transient load current step.

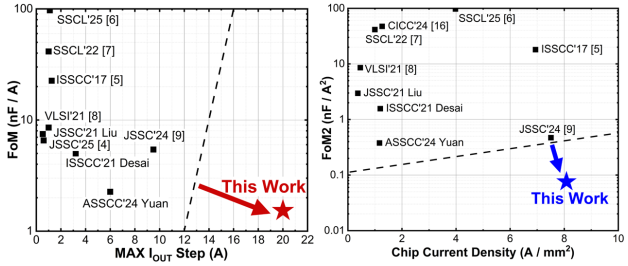

Fig. 11. FoM, FoM2, maximum load and Si die current density comparison.

reduction, adaptive boosting further mitigates the following ringing and enables stable settling within 100 ns.

Fig. 10 compares output-voltage droop under different load steps. While droop increases with load amplitude in both cases, ACCB consistently achieves superior suppression, with higher absolute and relative reduction at heavy loads—from 68.7% (57 mV) at 8 A to maximum 79.6% (191 mV) at 20 A, enabling a nearly 200-mV reduction in voltage guardband.

Fig. 11 and Table I summarizes the proposed ACCB achieves the best transient FoM, exhibiting a 5-63× reduction compared with the prior state-of-the-arts [5]-[8], while simultaneously supporting the largest load current step of 20 A, which is at least 10 A larger than previously reported values. The design also achieves the highest chip current density of 8.08 A/mm². In addition, the ACCB demonstrates at least 10× improvement in transient FoM2, further highlighting its superior efficiency in high-current transient droop suppression. These results collectively establish the proposed ACCB as delivering the highest transient droop mitigation capability among reported approaches.

V. Conclusions

This work presents an ACCB chiplet that augments a MMCSCR chiplet and proactively reconfigures flying capacitors and employs predictive power-gate control to boost current during transients for droop mitigation. The proposed ACCB reduces undershoot from 240 mV to 49 mV under 20-A load step, achieving 79.6% reduction. It attains leading FoMs of 1.53 nF/A and 0.076 nF/A² with 8.08 A/mm² current density, demonstrating a compatible and efficient solution for future fully integrated HPC systems.

Acknowledgement

This work was supported by the National Key R&D Program of China 2024YFF1400200 and Grant BNR2026RC01013. *Corresponding Author: Xiaosen Liu.*

TABLE I. Performance Comparison Table

		ISSCC'17 [5]	SSCL'25 [6]	SSCL'22 [7]	VLSI'21 [8]	This work
Process		130 nm	28 nm	180 nm	22nm	**65nm**
Voltage Regulator	**Architecture**	Buck	Buck	Buck	Buck	**MMCSCR**
	V_{IN} (V)	3.3	2.7 - 4.3	1.8	1.5 - 2.2	**3.8 - 5**
	V_{OUT} (V)	1.8	1.2	0.5 - 1.5	0.5 - 1.15	**0.8**
	Si Die Density (A/mm²)	1.22*	4.17*	0.922*	0.25*	**1.76**
Droop Suppression Scheme	**Architecture**	DLDO	DLDO	ITSC	DLDO	**ACCB**
	V_{IN} (V)	3.3	2.7 - 4.3	1.8	1.2	**0.8**
	Power I/O Combined	No	No	No	No	**Yes**
	F_{SW} Assisted	\	1 GHz	1 - 2 MHz	\	**250 MHz**
	Output Capacitor	940 nF	1 µF	200 nF	36 nF	**470 nF**
	Si Die Density (A/mm²)	6.94	6.87	0.461	1.0	**8.08**
Load Transient	**Load Step / Edge Time**	1.25A/2ns	1A/0.8ns	1A/100ns	1A/0.4ns	**20A/40ns**
	Undershoot (mV)	36	68	207	190	**49**
	Settling Time (ns)	125	112	186	13	**100**
	FoM (nF/A)	22.56	97.14	41.4	8.49	**1.53**
	FoM2 (nF/A²)	18.05	97.14	41.4	8.49	**0.076**

*Calculated using estimated part area due to layout constraints.

$$\textbf{FoM}\ [\mathbf{nF/A}] = \frac{V_{Droop,MAX}}{\Delta I_{OUT,MAX} V_{OUT}} \times C_{OUT},\quad \textbf{FoM2}\ [\mathbf{nF/A^2}] = \frac{V_{Droop,MAX}}{\Delta I_{OUT,MAX}^2 V_{OUT}} \times C_{OUT}$$

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