A 140-GHz 27-mW Fractional-N Synthesizer with 234-fs Jitter

Chandrakanth Choppa
Electrical and Computer Engineering
University of California, Los Angeles
Los Angeles, USA
chandrakanthc@ucla.edu

Long Kong
Fudan University
Shanghai, China
longkong@fudan.edu.cn

Behzad Razavi
Electrical and Computer Engineering
University of California, Los Angeles
Los Angeles, USA
razavi@ee.ucla.edu

***Abstract*—A cascaded architecture with a wideband fractional-N loop is introduced that greatly suppresses the delta-sigma modulator noise. Employing several novel concepts, the synthesizer achieves a 2.8X reduction in jitter and a 2X reduction in power, compared to the state of the art. Fabricated in 28-nm CMOS technology, the PLL exhibits an rms jitter of 234 fs, and consumes 27 mW while occupying an area of 0.248 mm^2, thus making it attractive for beamforming systems with one dedicated synthesizer per element.**

Keywords—140 GHz, 6G, clock generation, cascaded PLL, delta-sigma modulator, fractional-N PLL, phase frequency detector.

I. Introduction

The 140-GHz band presents an attractive medium for high-throughput wireless communications. A great deal of work has been expended on 6G radios for this band [1-3], but no fractional-N synthesizer operating at these frequencies has been reported. This paper addresses this need.

Our work introduces four concepts that improve performance: (1) a cascaded-PLL architecture using a wideband fractional-N loop, (2) a high-speed multimodulus divider (MMD), (3) a high-speed pipelined ΔΣ modulator, and (4) a highly-linear phase/frequency detector (PFD). As a result, the jitter is reduced by a factor of 2.8 and the power by a factor of 2 with respect to the state of the art.

II. General Considerations

A single-loop synthesizer architecture faces rigid trade-offs among reference phase noise (PN), VCO PN and the ΔΣ quantization noise (Q-noise) making cascaded PLLs more desirable. As illustrated in Fig. 1(a), increasing the ΔΣ clock frequency from f_{CK1} to f_{CK2} can significantly lower its in-band noise contribution. For a MASH 1-1-1, each doubling of f_{CK} lowers the rms jitter by about a factor of 2.5 to 3, encouraging us to maximize the fractional-N loop reference frequency.

Now, consider the permutations depicted in Fig. 1(b), (c). With a crystal frequency of a few hundred megahertz, the arrangement of Fig. 1(b) suffers from high ΔΣ noise unless its BW is drastically reduced. For example, cascaded PLL in [4] selects a BW of 120 kHz for its first PLL, leading to their first VCO to dominate phase noise at output leading to 650 fs jitter at f_{OUT} = 100 GHz with P = 54 mW. In Fig. 1(c), on the other hand, the ΔΣ noise can be minimized if f_1 is sufficiently high for a given bandwidth f_0, e.g., around 5 GHz. Moreover, the wide loop BW available in this scenario allows heavy suppression of the 140-GHz VCO in the second loop. This is one of key distinctions between our approach and the prior art. Our second PLL with a reference frequency of 4.75 GHz allows a bandwidth of ~60 MHz while suppressing the MASH 1-1-1 Q-noise running at a high frequency while consuming minimal power. Such an endeavor faces several challenges that will be described in sections below, along with novel concepts addressing them. Of course, the digital ΔΣM in this PLL must also be able to operate at a high frequency consuming minimal power.

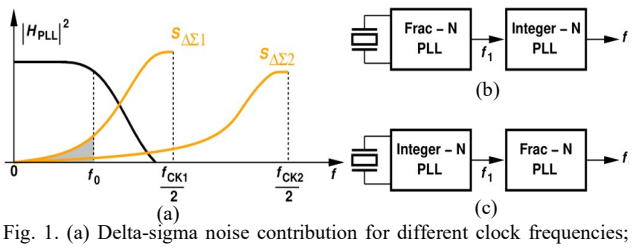

Fig. 1. (a) Delta-sigma noise contribution for different clock frequencies; (b), (c) Cascaded PLL permutations.

III. Proposed Synthesizer Architecture

Shown in Fig. 2, the proposed synthesizer consists of an integer-N loop that generates an output at 4.75 GHz and a fractional-N loop that receives this reference and produces a Q-noise profile having a peak at 2.375 GHz. The second PLL can thus benefit from a loop bandwidth as wide as ~60 MHz to suppress the PN of the 140 GHz VCO, and yet minimize the ΔΣ Q-noise. Our 140 GHz oscillator has a Q of 5, with a PN of -106.59 dBc/Hz at 10 MHz offset. Such a high phase noise requires a wide loop BW, greatly exacerbating the ΔΣ modulator noise problem – unless the modulator runs at a very high clock frequency. Each loop incorporates an LC VCO, a ÷4 stage, and a multimodulus divider.

The architecture of Fig. 2 merits several remarks. First, rather than generate 4.75 GHz directly, PLL_1 runs its VCO at 19 GHz and divides the result by 4. This is for two reasons:

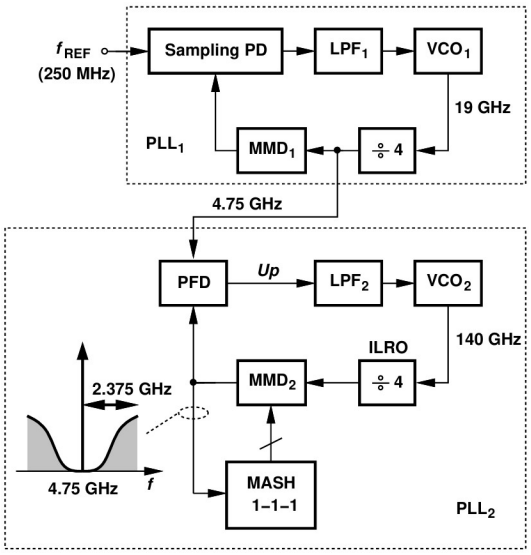

Fig. 2. Proposed synthesizer architecture.

(a) the inductor Q at 19 GHz is 50% higher, and (b) spurs generated at the output of VCO_2 due to coupling from VCO_1 are at least 12 dB lower. Second, for the MMD in PLL_2 to operate robustly in 28-nm technology, its input frequency must remain below approximately 40 GHz, hence the need for the ÷4 stage following VCO_2. Third, the MASH 1-1-1 ΔΣ modulator accommodates a 16-bit input, providing a frequency resolution of 290 kHz at 140 GHz. This resolution of 290 kHz at 140 GHz translates to an error of 2 ppm, which is much lower than typical crystal frequency errors of 10-100 ppm. In other words, there is no need to target finer resolutions. Fourth, while PLL_1 utilizes a sampling PD, PLL_2 opts for a new PFD structure and no charge pump so as to avoid folding of the ΔΣ Q-noise (Section Ⅳ, C).

Another remarkable property of the proposed architecture relates to its low fractional spur levels. To appreciate this point, we first note that a single loop operating with a reference of a few hundred megahertz must select a very small fractional control word (FCW), suffering from large in-band spurs. For example, the prototype in [4] exhibits spurs at -34.2 dBc. In our approach, on the other hand, the second loop's high reference frequency and FCWs in the range of 0.368 – 0.789 place the spurs far outside the loop BW (offset frequency of 0.75 GHz to 3.75 GHz over the 136 – 148 GHz locking range), (Section Ⅴ). In other words, by design, we avoid spurs below 750-MHz offset.

The architecture of Fig. 2 also faces a number of challenges. First, the MMD must operate robustly at 35 GHz in 28-nm technology. Second, the speed and power of the ΔΣM can prove prohibitive. Third, the high-speed phase detector in PLL_2 must exhibit a very high linearity so as to minimize folding of the ΔΣM's high-frequency noise. We address these challenges below.

The choice of the divide ratio following VCO_2 entails a trade-off between the ΔΣ Q-noise and the power consumption of MMD_2. If we instead select a ÷8 stage, the MMD output phase steps doubles, raising the Q-noise power by 6 dB, requires a more linear PD but the MMD power can be reduced from 1.67 mW to 0.8 mW. The relatively small change in power encourages the use of a ÷4 circuit implemented as an injection-locked ring oscillator (ILRO).

IV. BUILDING BLOCKS

A. Multimodulus Divider

The proposed MMD is implemented with a cascade of three ÷2/3 stages. Shown in Fig. 3(a) is the conventional structure of one ÷2/3 stage [6], where L_j denotes a latch. This circuit fails beyond 30 GHz due to excessive delays in paths from Q to X, Q to Z and Y to Z. We thus propose the topology depicted in Fig. 3(c), where latches L_1 and L_3 are eliminated. The structure still divides by 2 for $B = 0$ and by 3 for $B = 1$, while offering three advantages: (a) it can run at speeds as high as 48 GHz as shown in Fig. 3(d), (b) it consumes less power, and (3) it presents less capacitance to its input clock, hence allowing a rail-to-rail clock swing to enhance the speed. As a result, MMD_2 draws only 1.67 mW at 35 GHz. The omission of L_1 and L_3 does pose a lower bound of 27 GHz on the clock frequency, a manageable issue across PVT corners.

The proposed ÷2/3 circuit operates as follows. Suppose $B = 0$, the outer loop containing L_4 is disabled with Y set to 0.

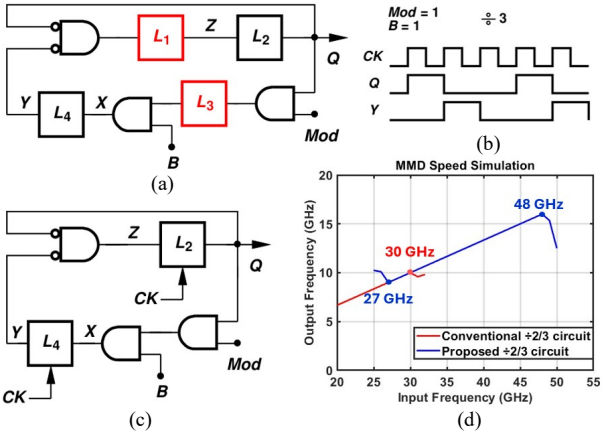

Fig. 3. (a) Conventional ÷2/3 circuit; (b) ÷3 waveforms; (c) proposed ÷2/3 circuit; (d) conventional vs proposed ÷2/3 circuit speed simulation for ÷3 mode.

L_2 returns its output Q to Z with an inversion, thus dividing CK by 2. The divide by 3 operation is shown in Fig. 3(b). Since we now set $B = 1$, Y is simply a clock cycle delayed version of output Q. At the first and second rising edge of CK, output Q toggles (like the ÷2 operation) as Y is still 0. On the third rising edge, since Y is now 1, the signal Z is made 0 which is latched onto Q. This leads to a missed transition on Q. At the 4th rising edge, Y is at 0, and thus the output Q toggles leading to the ÷3 operation.

B. ΔΣ Modulator

Processing a 16-bit input, the accumulators can exhibit a high capacitance in their clock path. The differential clock inputs (provided by MMD_2) see 200 fF load each, and draw 1.9 mW. The 16-bit adders must incur a total delay less than 86 ps, which is achieved by a hybrid carry-look-ahead and carry-select architecture. Despite this technique, the tight timing budget for transferring the output of the first accumulator to the second proves problematic, especially in view of the long interconnects between the two. To resolve this issue, we propose the pipelined MASH architecture illustrated in Fig. 4 where the z^{-1} stages shown in blue improve this budget by 10 to 15 ps. The eight output values after adding with the integer component (of value 7) drive MMD_2, yielding a maximum phase step of ±16 T_{VCO} at its output.

The 200-fF input capacitance of the MASH must be driven by MMD_2, introducing considerable delay. As shown in Fig. 5(a) the delay through the clock buffer (will need to

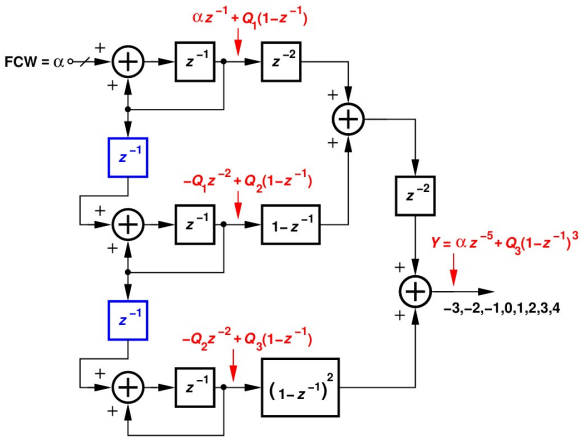

Fig. 4. Proposed MASH 1-1-1.

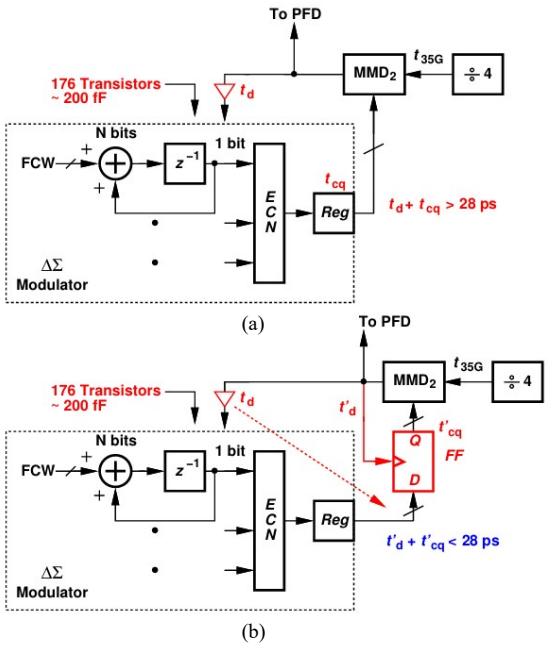

Fig. 5. (a) Problem of MASH-MMD interface timing; (b) proposed pipelining to resolve MASH-MMD interface timing.

be multistage) and MMD$_2$ input must remain less than about 28 ps ($t_d + t_{cq} \leq 28$ ps), a daunting challenge we faced when closing the loop. In Fig. 5(b), we propose the pipelining technique provided by *FF* to confer another 20 ps to this loop. Now t'_d is much smaller than t_d since the added 4 bit *FF* provides much smaller loading than the MASH's 200 fF, thus able to meet 28 ps ($t'_d + t'_{cq} \leq 28$ ps). This is essentially pipelining performed in the clock path resolving the MASH input clock buffer delay.

C. Linear PFD

PDs such as the two-stage passive sampling circuit or the TSPC PFD [7] can operate at 4.75 GHz but do not maintain linearity for phase excursions as large as ±16 T_{VCO}. As an example, Fig. 6(a) plots the simulated gain of a TSPC PFD, revealing a sharp change between 150º and 180º. If used in our architecture, this structure yields the PN behavior shown in Fig. 6(b), causing about 20 dB of rise in the in-band noise.

We propose the PFD shown in Fig. 7, where *REF* is the reference clock from PLL$_1$. The pulse gen. circuit generates a pulsewidth of $\Delta T \approx 24$ ps from the output of MMD$_2$ (on every rising edge on V_{DIV}) and operates as follows. When *REF* is low, *P* is high while *B* is high and *Up* is low. If *REF* rises, the first loop retains the logical ONE at *P*, and the second loop carries this level to *Up*. When the rising edge on V_{DIV} arrives after a lag ΔT_E, *B* then falls, *Up* is reset to zero, exhibiting a pulsewidth equal to the phase difference between *REF* and V_{DIV}. The key property of this topology is

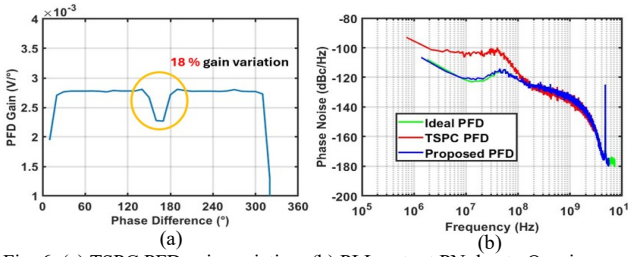

Fig. 6. (a) TSPC PFD gain variation; (b) PLL output PN due to Q-noise.

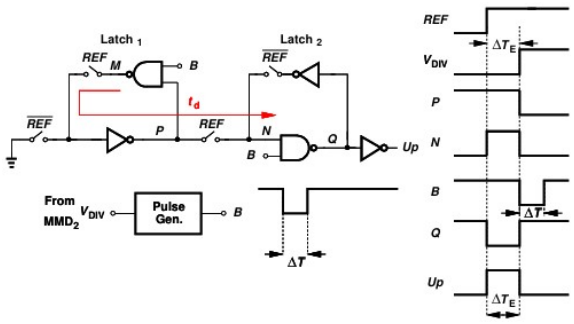

Fig. 7. Proposed PFD.

that it achieves high linearity because the transition time to reset *Up* is independent of the instantaneous phase error. This point stands in contrast to, for example, the TSPC PFD which suffers from charge sharing and hence an input-dependent delay. We remark that ΔT must be greater than the delay from *M* to *N* (t_d) for correct operation. Note that the logic for the down pulse is omitted to save power. The two-stage LPF$_2$ in Fig. 2 simply extracts the dc content of the *Up* pulse while suppressing its harmonics. Since the residual ripple on the control of VCO$_2$ is at 4.75 GHz, it leads to small spurs at the output.

Fig. 6(b) plots the PN of our fractional-N loop with the proposed PFD, indicating negligible folding.

V. EXPERIMENTAL RESULTS

The cascaded synthesizer has been fabricated in TSMC's 28-nm technology. Fig. 8(b) shows the die, whose active area measures 611 µm x 406 µm. PLL$_1$ draws 5.1 mW and PLL$_2$ 21.5 mW (5.1 mW in VCO$_2$, 4.3 mW in MASH, 1.67 mW in MMD$_2$, 2.4 mW in ILRO, 2.13 mW in ILRO output buffer, 2.85 mW in PFD and 3 mW in MASH clock buffer). The compact, low-power design makes it attractive for beamforming systems with one dedicated synthesizer per element. To simplify measurements, an on-chip mixer (Fig. 8(a)) downconverts the output of PLL$_2$ with the aid of an external 136 GHz signal. Fig. 9 shows the downconverted spectrum when the PLL cascade is locked at 140 GHz. Fig. 10 displays the output phase noise of PLL$_1$ (directly measured from its 4.75 GHz output), suggesting an rms jitter of 212 fs. Fig. 11 plots the PN of the overall cascade in the fractional-N mode (after downconversion to 4 GHz). Integrated from 10 kHz to 300 MHz, the total rms jitter amounts to 234 fs, suggesting that PLL$_2$ contributes only about 100 fs. The integer portion of the division ratio into the MMD$_2$ is set to 7. Fig. 12 presents the measured fractional spur levels when the PLL output frequency is locked from 136 GHz to 148 GHz (in steps of 1 GHz) by sweeping the FCW from 0.368 to 0.789. As explained in section III the proposed synthesizer is free from spurs below 750 MHz. The

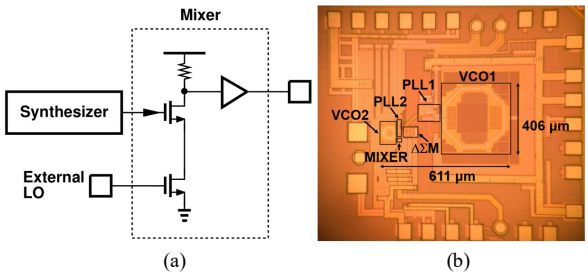

Fig. 8. (a) On-chip mixer; (b) die micrograph.

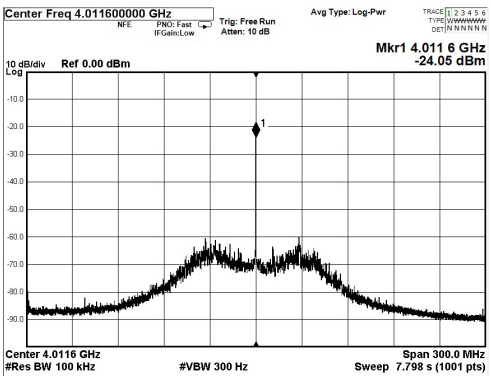

Fig. 9. Output spectrum produced by the on-chip mixer.

highest is around -67.27 dBc.

Table 1 compares our work to the state of the art in the range of 100–140 GHz. Papers [5] and [1] use integer-N architectures. In general, integer-N synthesizers achieve better jitter performance because they do not rely on ΔΣ modulators, enabling a wider loop bandwidth and more effective suppression of phase noise from low-Q VCOs at high frequencies. We note that [1] uses a reference frequency of ~5.8 GHz. Generating such a clean source is often quite power hungry and is not included in their reported 79.2 mW power consumption. Comparing with the only fractional-N design [4] in this frequency range, we achieve a 2.8X reduction in jitter, a 2X reduction in power and 33 dB lower fractional spurs.

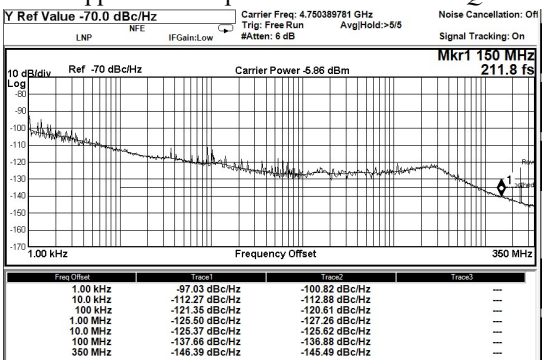

Fig. 10. Measured phase noise of PLL_1.

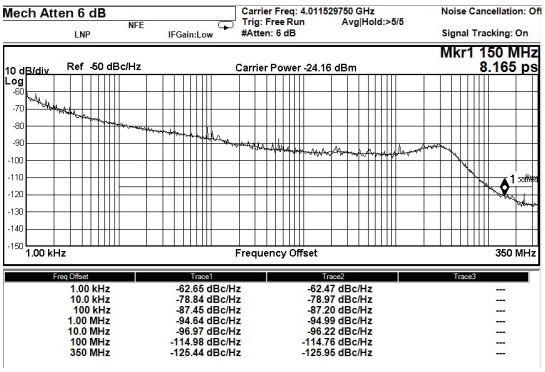

Fig. 11. Measured phase noise of the PLL cascade. Mixer output jitter of 8.165 ps must be divided by 34.9 (140.011/4.011) to refer to the VCO_2 frequency of 140.011 GHz, yielding 234 fs.

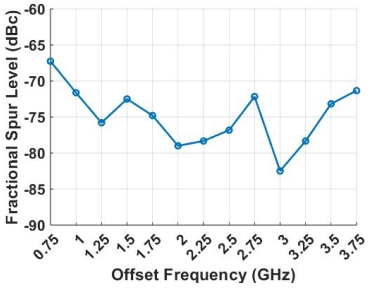

Fig. 12. Measured fractional spur levels.

VI. CONCLUSION

We have demonstrated a novel cascaded PLL where the ΔΣ modulator is clocked at 4.75 GHz. Several new circuit and architecture techniques were introduced to enable the proposed synthesizer and achieve 2X reduction in power and ~2.8X reduction in jitter compared to the state of the art.

TABLE 1. Performance summary

Reference	This Work	[4]	[5]	[1]
Frequency (GHz)	136-148	93.4 – 104.8	99.5 – 102.5	140
Technology	28nm CMOS	65nm CMOS	65nm CMOS	22nm FinFET
Type	Frac.-N	Frac.-N*	Int.-N	Int.-N*
Resolution (kHz)	290	3.6	NA	NA
Power (mW)	27	57	22.5	79.2
RMS Jitter (fs)	234	650	82	31.7
Integ. Range (MHz)	0.01 - 300	0.01 - 300	0.001 - 300	0.1 - 1000
P.N. @1MHz (dBc/Hz)	-94.6	-85.53	-104.3	-112.7
Ref. Freq (MHz)	250	100	500	5800
Ref. Spur (dBc)	-55.6	-43.83	-42	-
Max Frac. Spur (dBc)	-67.27	-34.23	NA	NA
FoM (dB)	-238.3	-226.2	-248.2	-251
Area (mm^2)	0.248	0.8755	0.16	-

$\text{FoM} = 10\log_{10}\left[\left(\frac{\text{Jitter}}{1\text{s}}\right)^2\left(\frac{\text{Power}}{1\text{mW}}\right)\right]$ *Quadrature output

REFERENCES

[1] S. Callender et al., "A fully integrated 160Gb/s D-and transmitter with 1.1 pJ/b efficiency in 22nm FinFET technology," ISSCC, pp. 78-80, Feb. 2022.

[2] S. Dong et al., "A 140GHz RF beamforming phased-array receiver supporting >20dB IRR with 8GHz channel bandwidth at low IF in 22nm FDSOI CMOS," RFIC, pp. 293-296, June 2023.

[3] A. Ahmed et al., "140-GHz 2-D scalable on-grid 8✕ 8-element transmit–receive phased arrays with up/down converters demonstrating a 5.2-m link at 16 Gbps," TMTT, vol. 72, pp. 2852-2868, May 2024.

[4] X. Yi et al., "A 93.4–104.8-GHz 57-mW fractional- ${N}$ cascaded PLL with true in-phase injection-coupled QVCO in 65-nm CMOS technology," TMTT, vol. 67, pp. 2370-2381, June 2019.

[5] S. Park, S. Choi, S. Yoo, Y. Cho and J. Choi, "An ultra-low jitter, low-power, 102-GHz PLL using a power-gating injection-locked frequency multiplier-based phase detector," JSSC, vol. 57, pp. 2829-2840, Sept. 2022.

[6] C. S. Vaucher, et al., "A family of low-power truly modular programmable dividers in standard 0.35-/spl mu/m CMOS technology," JSSC, vol. 35, pp. 1039-1045, July 2000.

[7] Won-Hyo Lee, Jun-Dong Cho and Sung-Dae Lee, "A high speed and low power phase-frequency detector and charge-pump," Proceedings of the ASP-DAC '99 Asia and South Pacific Design Automation Conference, pp. 269-272, Jan. 19.