A Chopper-Stabilized Class-AB Operational Amplifier in Monolithic GaN Technology

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***Abstract*—This paper presents a monolithic GaN operational amplifier with a class-AB output stage and demonstrates the first chopper-stabilized op-amp in this technology. Chopping is used to reduce the large DC offset and low-frequency noise inherent to GaN devices, lowering the measured offset from 90 mV to 8 mV under DC conditions and to 12 mV for a 500 Hz sinusoidal input with a 500 kHz chopping frequency. The amplifier operates from a 7 V supply and can drive capacitive loads up to 100 pF. Measurements show an open-loop gain of at least 87 dB at 20 Hz, a source/sink current capability of -30 mA and +40 mA, and slew rates of +1.5 V/μs and -0.8 V/μs. The PSRR is 89 dB at 10 kHz and 65 dB at 1 MHz, demonstrating the feasibility of precision analog design in monolithic GaN technology.**

***Index Terms*—op-amp, Gallium Nitride, class AB, chopper stabilization, offset reduction.**

I. Introduction and State of the Art

Gallium Nitride (GaN) has emerged as a promising material for high-efficiency, high-frequency power amplification, owing to its wide bandgap, high electron mobility, and superior breakdown voltage compared to conventional silicon [1]. These intrinsic advantages enable GaN devices to achieve higher power density and faster switching speeds, making them ideal for RF, mixed-signal, and power-management applications [2], [3].

Despite GaN technology's advantages, integrated circuits for mixed-signal and analog blocks, such as operational amplifiers (op-amps), remain challenging. This is mainly due to the absence of complementary p-channel devices; GaN processes currently support only n-channel depletion-mode (D-HEMTs) and enhancement-mode (E-HEMTs) transistors and passive components. However, monolithic GaN technology is appealing for high-frequency and high-temperature operation in a compact, efficient form [4].

In this emerging GaN technology, device trapping and process variability cause significant low-frequency flicker noise and DC offset, limiting precision. Chopper stabilization mitigates these by modulating non-idealities out of the signal band and shifting them to higher frequencies, where filtering attenuates them. This enhances accuracy and stability, allowing GaN op-amps to achieve low-noise, high-precision performance while retaining wide-bandgap advantages. GaN MMIC-based (Monolithic Microwave Integrated Circuit) op-amps have been demonstrated in prior works. [5], [6]. In [7], the op-amp was used in a fully integrated GaN gate driver implemented using a 0.5-μm GaN-on-Si process. A two-stage amplifier for current sensing with E-HEMT and D-HEMT devices and a source follower appears in [8]. A three-stage op-amp using only E-HEMTs was reported in [9]. Differential E-HEMT pairs are used in current-sensing circuits [10]. In [11], a two-stage amplifier using both E-HEMT and D-HEMT devices with optimized chip area was presented.

This work presents a class-AB op-amp in monolithic GaN technology with chopper stabilization, reducing DC offset from 90 mV to 8 mV (DC) and 12 mV for a 500-Hz sine input at 500 kHz f_{chop}. The op-amp operates at 7 V, drives up to 100 pF, and is validated in STpGaN monolithic technology. It achieves a 87 dB DC open-loop gain, a source/sink current capability of -30 mA and $+40$ mA, slew rates of +1.5 V/μs and -0.8 V/μs, and a PSRR of 89 dB at 10 kHz and 65 dB at 1 MHz.

II. Proposed Chopper-Stabilized Amplifier with Class AB Output Stage

A. Circuit Description

The current generator block in Fig. 1 (top-right) operates as an active load or bias current source, depending on output connection. Although depicted with its output connected to V_{DD}, it can also be connected to other nodes while maintaining current-source behavior with sufficient voltage headroom. These blocks replace p-channel transistors as active loads and current sources [12]. It consists of a D-HEMT M_{DA} and a resistor R. A cascode D-HEMT M_{DB} is added to increase the output impedance. To ensure a minimum current ($\sim 10\,\mu A$) through the transistor, a resistor of approximately $20\,k\Omega$ is connected to the source node of M_{DA}. The output impedance of the current generator block can be expressed as

$$R_{out} \approx g_{mDB} g_{mDA} r_{oDB} r_{oDA} \cdot R, \tag{1}$$

where g_{mDA}, g_{mDB} are the transconductance of M_{DA} and M_{DB} respectively, r_{oDA}, r_{oDB} are the drain-to-source resistance of M_{DA} and M_{DB} respectively and R is the resistance connected at the source of M_{DA}. The D-HEMT pair, M_{D1} and M_{D2}, forms the differential input stage of the amplifier shown in Fig. 1. The current generator blocks I_{D1} and I_{D2} serve as active loads, while I_{D3} functions as the tail current source. I_{D3} is realized using the same self-biased current generator block described above, with its output node connected to the

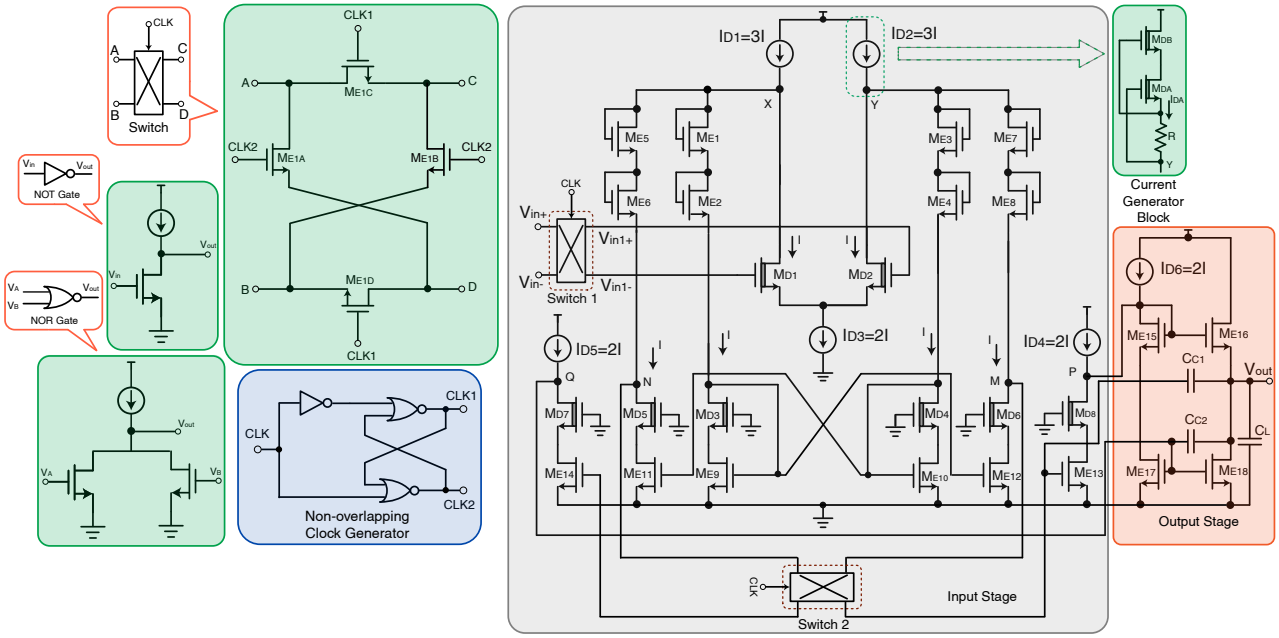


Fig. 1: Schematic diagram of the proposed Class AB operational amplifier.

tail of the differential pair. D-HEMT devices are employed in the input pair to extend the lower limit of the input common-mode voltage and increase the gain, benefiting from their intrinsic transconductance (g_m). To effectively suppress flicker noise and offset, chopper stabilization is implemented in the design. The input signal is initially modulated by Switch 1, amplified through the first stage, and then demodulated by Switch 2 to recover the desired signal while up-converting low-frequency noise components. The non-overlapping clock generator, essential for chopper operation, uses GaN-based NOT and NAND gates in ratioed Direct-Coupled FET Logic (DCFL). E-HEMTs act as pull-down devices, and a current-generator block replaces p-channel transistors, ensuring correct logic swing and robust noise margins.

Two pairs of 1:1 cascode current mirrors provide fully differential output in the first stage. The first mirror uses M_{D3}, M_{E9}, M_{D6}, M_{E12}; the second, M_{D4}, M_{E10}, M_{D5}, M_{E11}. The differential outputs of the first stage (nodes M and N) drive two common-source amplifiers implemented by (M_{D8}, M_{E13}) and (M_{D7}, M_{E14}). The quiescent voltage at nodes X and Y is set to $3V_{GS}$ ($2V_{GS}$ from two diode-connected E-HEMTs, $1V_{GS}$ from the current mirror). These diode-connected transistors (M_{E1}-M_{E4}) also serve as level shifters, extending input common-mode range. The small-signal gain at nodes M and N can be approximated as

$$A_{v,\text{nodeM}} \approx g_{mD1}\Big[\Big(r_{oD2} + \frac{1}{g_{mE7}} + \frac{1}{g_{mE8}}\Big) \Big\| \left(r_{oE12}\, g_{mD6}\, r_{oD6}\right)\Big], \tag{2}$$

$$A_{v,\text{nodeN}} \approx g_{mD2}\Big[\Big(r_{oD1} + \frac{1}{g_{mE5}} + \frac{1}{g_{mE6}}\Big) \Big\| \left(r_{oE11}\, g_{mD5}\, r_{oD5}\right)\Big]. \tag{3}$$

The differential outputs of the first stage (nodes M and N) are processed by Switch 2, which drives the second-stage common-source amplifiers. The same switch network subsequently demodulates the amplified signal back to baseband. M_{D6}, M_{D7} are the cascode transistor to boost the gain while M_{E13}, M_{E14} are the common source transistors. The current sources I_{D4} and I_{D5} are used as the active load. The output impedance at nodes P and Q can be evaluated as

$$R_{oP} \approx g_{mD8} r_{oD8} r_{oE13} \,\|\, r_{oID4}, \tag{4}$$

$$R_{oQ} \approx g_{mD7} r_{oD7} r_{oE14} \,\|\, r_{oID5}. \tag{5}$$

The voltage gain magnitude at node P and Q of this stage can be approximated as $g_{mE13}R_{oP}$ and $g_{mE14}R_{oQ}$, respectively.

C. Class AB Output Stage

The class AB output stage in Fig. 1 has low output impedance, suitable for capacitive loads. Differential outputs (nodes P and Q) from the input stage drive the high side (M_{E16}) and low side (M_{E18}) transistors. The current source I_{D6}, along with the diode connected transistor M_{E15}, ensures a constant bias current inside the loop and the required V_{gs} for the level shifting. On the high side, M_{E16} operates as a source follower, providing current to the output node, whereas on the low side, M_{E18} functions as the pull-down device,

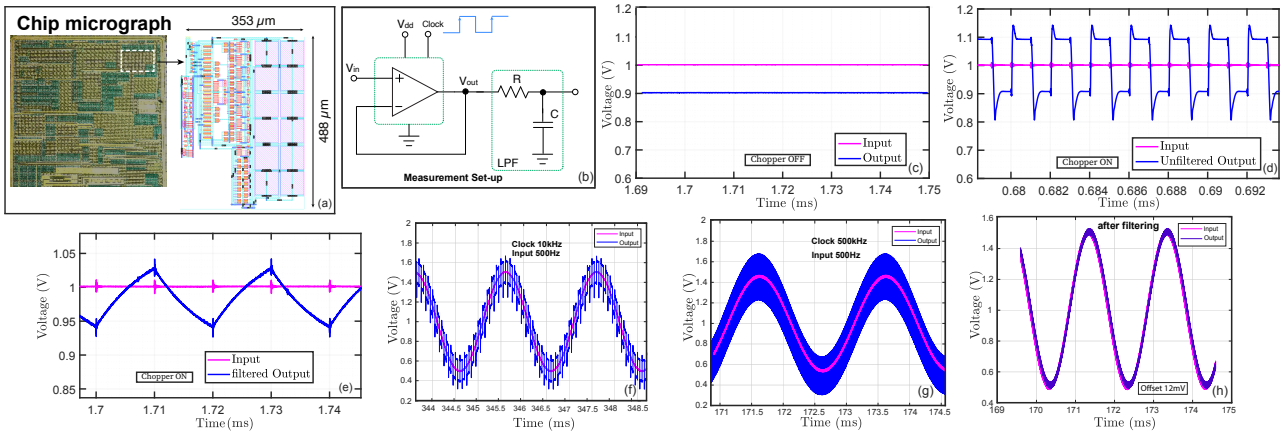


Fig. 2: Measured results of the proposed amplifier: (a) Chip micrograph, (b) measurement setup, (c) input (1 V DC) and output waveform with chopper OFF, (d) output waveform with chopper ON (1 V DC input, 500 kHz clock), (e) filtered output with chopper ON, (f) output waveform with chopper ON (500 Hz input, 10 kHz clock), (g) output waveform with chopper ON (500 Hz input, 500 kHz clock), (h) filtered output with chopper ON.

sinking current from the output (V_{out}). Diode-connected E-HEMT M_{E15} and M_{E17} generate the gate bias voltages for M_{E16} and M_{E18} to maintain a small quiescent conduction near the zero-crossing point. To boost load current without increasing bias, output transistors are sized larger than diode-connected ones (M_{E15}, M_{E17}). With a scaling factor of 5, M_{E16} and M_{E18} can source or sink about five times the bias current set by M_{E15} and M_{E17}, allowing up to ± 10 mA output drive, as given by

$$(W/L)_{M_{E16}} = 5 \cdot (W/L)_{M_{E15}}, \tag{6}$$

$$(W/L)_{M_{E18}} = 5 \cdot (W/L)_{M_{E17}}. \tag{7}$$

C_{C1} connects the first-stage output (cascode drain node M) directly to the amplifier output, while C_{C2} is placed between the second-stage differential output (node Q) and the amplifier output. The combined use of C_{C1} and C_{C2} establishes a controlled pole–zero pair. Specifically, C_{C1} introduces a phase-lead zero near the unity-gain frequency, effectively compensating for the phase lag introduced by non-dominant poles, while C_{C2} introduces a high-frequency pole that attenuates gain increase and stabilizes the frequency response. This coordinated compensation shapes the loop gain, resulting in a smooth roll-off and improved phase margin of $56°$, thereby ensuring stable amplifier operation.

III. Experimental Results

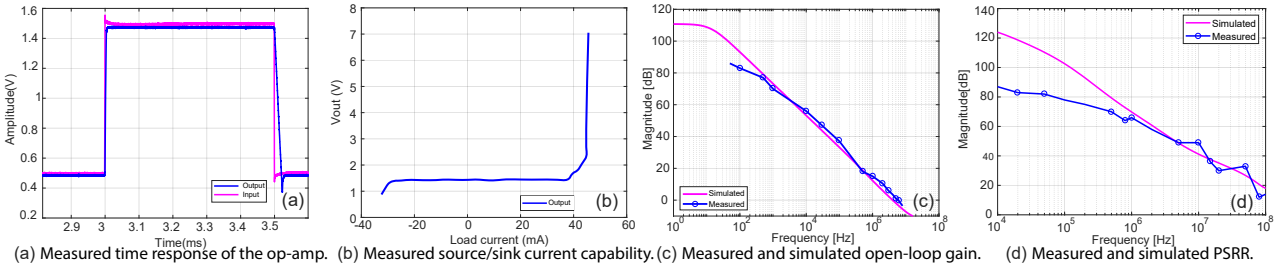
The proposed op-amp was designed using the STpGaN PDK in Cadence Virtuoso. Table I summarizes the measured output offset for various input signals with the chopper on and off. The design was fabricated by STMicroelectronics and tested in a 68-pin Thin Quad Flat Package (TQFP) (Fig. 2(a)), occupying $0.172\,\text{mm}^2$ active area. Input signals were generated with an Agilent 3351A function generator and outputs measured using an R&H RTO 2024 oscilloscope. With

TABLE I: Measured Offset Reduction Using Chopper Stabilization

Chopper	Input Signal	Offset (mV)
✗	1 V DC	90
✓	1 V DC, $f_{clk} = 500$ kHz	8
✗	$f_{in} = 500$ Hz	89
✓	$f_{in} = 500$ Hz, $f_{clk} = 500$ kHz	12

a 7 V supply, the measured current is 150 μA and the input dynamic range is 3.3 V, consistent with simulation results. The chopper-stabilized class-AB op-amp was characterized using the setup in Fig. 2(b). DC measurements in (Fig. 2(c-e)) show a 90 mV offset with the chopper OFF (1 V input), which is reduced to 8 mV after filtering when the chopper is enabled. The spikes observed in the output waveform after chopping originate from the switching action, where the square-wave signal capacitively couples to the amplifier input, appearing as residual offset at the output. For a 500 Hz sine input, increasing the chopping frequency from 10 kHz to 500 kHz shifts offset to higher frequencies, minimizing baseband distortion (Fig. 2(f-g)). The external low-pass filter ($R = 1\,\text{k}\Omega, C = 3\,\mu\text{F}$) suppresses ripple, achieving accurate signal recovery and $\sim$12 mV residual offset.

Although a lower offset (1 mV) has been reported in [9], it reflects an inherently low offset in a different GaN process. In contrast, chopper stabilization in this work achieves a $> 10\times$ reduction (from 90 mV to 8 mV). The residual offset is mainly attributed to switching non-idealities and charge injection. Fig. 3(a) presents the slew-rate measurement: $1.52\,\text{V}/\mu\text{s}$ (rising) and $0.77\,\text{V}/\mu\text{s}$ (falling) for a $0.5\,\text{V}$ input step. A source/sink current of -30 mA and $+40$ mA is obtained, as shown in (Fig. 3(b)). Fig. 3(c) compares measured and simulated open-loop gain, with at least 87 dB at 20 Hz. Measurements below this frequency are limited by $1/f$ noise



(a) Measured time response of the op-amp. (b) Measured source/sink current capability. (c) Measured and simulated open-loop gain. (d) Measured and simulated PSRR.

Fig. 3: Measured performance of the proposed chopper stabilized Class AB operational amplifier

TABLE II: PERFORMANCE COMPARISON

Parameter	**Access 21 [11]**	**TCAS-I 24 [9]**	**SSCL 23 [13]**	**This work**
Technology	p-GaN	GaN IC	CMOS	STpGaN
Supply voltage (V)	12	6	5	7
Gain (dB)	20	60	>70	87
GBW (MHz)	-	25	10	6
Slew Rate ($V/\mu s$)	-	70	5.8	1.52 0.77
PSRR (dB) @ 10 kHz	-	50.4	124	85
Input V_{OS} (mV)	-	1	0.008	8
Area (mm^2)	0.0153	0.0357	≈0.6	0.1723
Power Consumption (mW)	183.6	1.8	4.25	1.05

and offset. The measured gain and response closely match the simulated behavior. Fig. 3(d) presents measured and simulated PSRR, achieving 89 dB at 10 kHz. This is mainly due to cascode configuration, which boosts output impedance, and a high-impedance current generator, combined with a fully differential architecture, which enhances supply noise rejection. Table II shows that the proposed amplifier achieves the highest gain among reported GaN-based designs with low power consumption. It operates at a moderate supply voltage and exhibits improved PSRR. Compared to CMOS designs, it achieves competitive performance while occupying a smaller area. The use of chopper stabilization enables significant offset reduction, addressing a key limitation of GaN technology and highlighting its potential for precision analog applications.

IV. CONCLUSIONS

This work presented a monolithic GaN operational amplifier with a class-AB output stage and, to the best of the authors knowledge, demonstrated the first chopper-stabilized implementation in monolithic GaN technology. Chopper stabilization reduces the DC offset from 90 mV to 8 mV under DC conditions and to 12 mV for a 500 Hz input. These results validate the effective suppression of low-frequency offset and highlight the potential of chopper stabilization for precision analog design in GaN technology.

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