Extensive Analysis of PBTI-induced Retention Degradation in IGZO-based 2T0C Memory

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***Abstract*— We successfully reveal the impact of positive bias temperature instability (PBTI) on memory retention of IGZO-based capacitorless two-transistor (2T0C) cells. The measurement scheme introduced in this work enables the extraction of threshold voltage shift in the write transistor and charge loss from the storage node in parallel. From the correlation of these parameters, we identify that PBTI degrades retention characteristics in two ways: the electrons trapped in gate oxide by the PBTI are released and gate leakage increases due to the PBTI. In actual memory write operation, since short voltage pulses with a small duty factor are used, retention loss due to recovery components like the former becomes negligible. On the other hand, an increase in gate leakage like the latter is a permanent component, making it potentially critical for the memory devices. These findings provide new insights into reliability challenges toward the realization of IGZO-based 2T0C DRAM.**

Keywords—2T0C, Capacitorless, DRAM, InGaZnO, oxide semiconductor, gate bias stress, threshold voltage, retention

I. Introduction

InGaZnO-based capacitorless two-transistor (IGZO 2T0C) memory is a promising candidate for future eDRAM with high memory density and low power consumption [1-4]. In addition to the back-end-of-line compatibility of IGZO thin-film transistors (TFTs) [5], their extremely low off-leakage current enables long retention even without a physical capacitor in the memory cells. In turn, it not only reduces the refresh rate but also contributes to higher integration. Furthermore, the two-transistor configuration (Fig.1(a)), consisting of a write transistor (Wtr) and a read transistor (Rtr), allows non-destructive readout of the stored charges in the storage node (SN). Despite these outstanding advantages, reliability concerns, positive/negative bias temperature instability (PBTI/NBTI) in the IGZO TFTs, remain a major barrier to industrial adaption [6]. The PBTI is dominated by mainly two degradation mechanisms: at room temperature (RT) the PBTI induces only positive threshold voltage shift (ΔV_{th}) due to electron trapping in the gate oxide, while at high temperature (HT) abnormal negative ΔV_{th} becomes prominent due to the doping of hydrogen (H) released from the gate oxide. The NBTI also causes negative ΔV_{th} activated by HT based on H-doping process in a similar way to the PBTI [7]. Under actual memory DRAM operation, write operation applying positive voltage to a gate of Wtrs corresponds to the PBTI, whereas data retention applying negative voltage to the gate corresponds to the NBTI. Although degradation of the Wtr characteristics is expected to directly affect memory retention, its impact has not been investigated so far.

In this work, we investigated the impact of PBTI on retention characteristics in IGZO 2T0C cells using a dedicated measurement sequence developed. PBTI stress was applied to the Wtr, and two consecutive retention measurements were carried out. During these measurements, ΔV_{th} in the Wtr and retention loss – voltage drop in storage node (δV_{SN}) – were monitored, enabling the analysis of their correlation. Note that the measurements were performed at RT, corresponding to focusing on the effect of the electron trapping in the gate oxide. This choice helps avoid involving complex H-doping process and is justified by the fact that this process can be suppressed in AC write pulses with a small duty factor < 25% [8], which is expected from actual write operation. As a result, we found two types of retention degradation via PBTI at RT: 1) inflow of detrapped electrons from the gate oxide into the SN and 2) an increase in gate leakage due to possible damage to the gate oxide. We also discussed the relevance of these factors under practical operation.

II. Device Evaluation Methodology

A. 2T0C structure and measurement sequence

For the 2T0C cells, we used gate-last IGZO TFTs with an oxygen tunnel (Fig.1(b)). The details of the fabrication flow are reported in [9]. 7 nm a-IGZO film for a channel and 10 nm CAAC-IGZO film for raised contacts were deposited using a 300 mm PVD platform with a target of In:Ga:Zn = 1:1:1. 5 nm ALD Al_2O_3 gate oxide with permittivity $\varepsilon = 8.8\ \varepsilon_0$ was deposited at 250 °C. At the end of the process, O_2 annealing was conducted to optimize V_{th}. We used the Rtr with channel width (W) of 1 μm and gate length (L) of 120 nm, while the Wtr with W of 1 μm, 600 nm or 180 nm, and L of 120 nm were utilized.

Fig.2 defined a newly developed measurement sequence for evaluating the impact of PBTI on retention characteristics in the 2T0C cells. At first, V_{th} extraction of the Wtr and retention measurement were carried out as an initial reference. PBTI stress (overdrive voltage V_{ov} = +3.6 V at RT) was applied to the gate (WWL) of the Wtr for a stress time of 2 s, where the stress voltage value was predetermined to achieve a ΔV_{th} of 0.2 ~ 0.3 V after the total stress time of 1300 s. Then, the V_{th} extraction and retention measurement were performed twice. This is because we observed recovery of PBTI during the first retention measurement, which will be discussed in Sec. III A. After the second retention measurement, this sequence was repeated with incrementing the stress time (2, 10, 40, 100, 300, and 848 s) until the total stress time reached 1300 s. In the retention measurements within this whole sequence, the hold voltage ($V_{WWL,Hold}$) to hold the V_{SN} was fixed. A full sequence was performed at different $V_{WWL,Hold}$ from -0.8 V to -1.4 V by 0.1 V step, with five samples taken at each voltage.

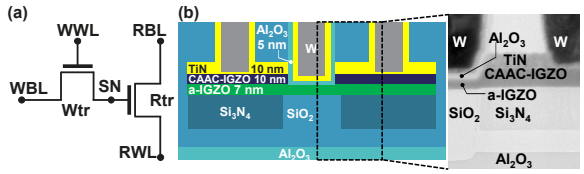

Fig.1 (a) Circuit schematic of a 2T0C DRAM cell with a read transistor (Rtr) and a write transistor (Wtr). (b) A schematic of a cross-sectional view and TEM image of a gate-last IGZO-TFT used for the Rtr and Wtr.

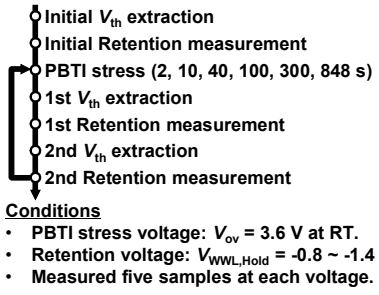

Fig.2 Measurement sequence for evaluating the impact of PBTI on retention characteristics in the 2T0C cells and the corresponding voltage conditions.

B. V_{th} extraction method of Wtr

Since transfer characteristics of the Wtr cannot be measured directly, we extracted V_{th} of the Wtr by utilizing read currents in the Rtr (I_{Rtr}) for different V_{WWL} values (Fig.3(a)). When sweeping the WBL voltage V_{WBL} from -1 V to 2 V, the I_{Rtr} with the WWL voltage V_{WWL} = 1 V began to deviate downward from that with V_{WWL} = 1.5 V at a certain voltage, where the Wtr entered the saturation region for V_{WWL} = 1 V. As shown in Fig.3(b), we calculated I_{Rtr} relative change 1-(I_{Rtr} at V_{WWL} = 1 V/ I_{Rtr} at V_{WWL} = 1.5 V) as a function of V_{WBL} and defined the V_{WBL} at I_{Rtr} relative change = 0.1 as the deviation voltage V_{dev}. Finally, V_{th} of the Wtr was estimated as V_{WWL}(= 1 V) - V_{dev}.

To confirm the validity of this V_{th} extaction method, we compared V_{th} distributions of Wtrs and Rtrs (Fig.4), where V_{th} values of Rtrs were obtained from constant current method I_{Rtr} = 100 pA × (W/L). Although the absolute values were different due the different V_{th} definitions, similar V_{th} distributions were obtained, indicating the validity of our V_{th} extraction method in Wtrs.

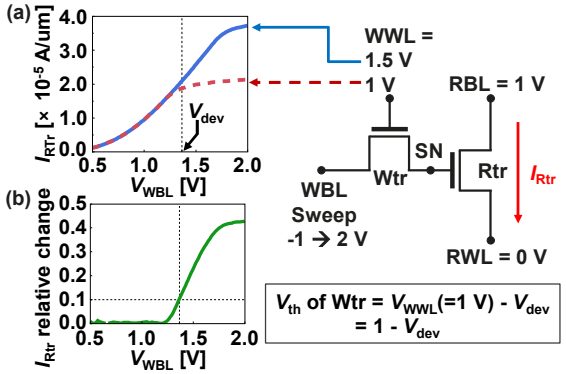

Fig.3 (a) Rtr transfer characteristics (I_{Rtr}-V_{WBL}) at V_{WWL} = 1.5 and 1 V. (b) I_{Rtr} relative change 1-(I_{Rtr} at V_{WWL} = 1 V/ I_{Rtr} at V_{WWL} = 1.5 V). V_{WBL} at the I_{Rtr} relative change = 0.1 is defined as the deviation voltage V_{dev}, which is used to extract V_{th} of the Wtr as V_{th} = V_{WWL}(= 1 V) – V_{dev}.

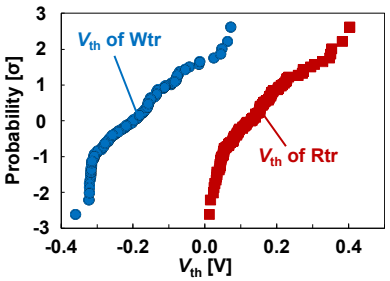

Fig. 4 Probability plots of V_{th} of Wtrs and V_{th} of Rtrs over the 300 mm entire wafer. The V_{th} distributions were similar even in different extraction methods, which validates our V_{th} extraction method in Wtrs.

C. Retention measurement

Fig.5(a) shows voltage conditions and timing diagram for retention measurement with the 2T0C cells. The 400-s retention measurement was performed with the voltages at the WWL and WBL held at $V_{WWL,Hold}$ and 0 V, respectively, after writing 1 V from the WBL to the SN. As a retention loss indicator, we used the δV_{SN} at the hold time of 400 s (Fig.5(b)), where δV_{SN} values were converted from the monitored I_{RTr} using polynomial fitting of the Rtr transfer characteristics [1].

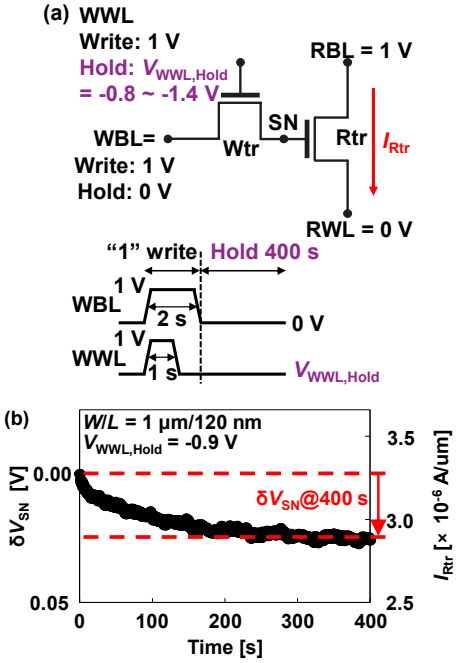

Fig.5 (a) 2T0C circuit diagram and 400-s retention measurement condition. V_{WBL} = 1 V was used for "1" write to the SN and hold voltage $V_{WWL,Hold}$ was used for holding V_{SN}. (b) An example of retention characteristics in a 2T0C device. δV_{SN} is defined as the V_{SN} when V_{SN} drops after 400 s.

III. Results and Discussion

A. Retention degradation due to detrapped electrons

Fig.6(a) and (b) illustrate the ΔV_{th} and δV_{SN} as a function of the total PBTI stress time obtained from the whole measurement sequence for the case of $V_{WWL,Hold}$ = -0.9 V, where each data point represents the median of five samples. As stress time increases, both the first and second ΔV_{th}

increase due to the electron trapping in the gate oxide of Wtr [6]. Remarkably, the second ΔV_{th} was slightly smaller than the first ΔV_{th}, indicating the recovery from the PBTI degradation during the first retention measurement. On the other hand, both the first and second δV_{SN} increase as the stress time increases, while the second δV_{SN} is always smaller than the first δV_{SN}. As a result, the trends of ΔV_{th} and δV_{SN} appear to be correlated, which suggests the following mechanism. First, the PBTI stress induced electron trapping in the gate oxide, which caused positive ΔV_{th}. Then, some of the trapped electrons were detrapped by the negative $V_{WWL,Hold}$ during the first retention measurement, resulting in the V_{th} recovery. In addition, the detrapped electrons flowed into the SN and led to the extra charge loss in the first retention measurement.

To confirm the effect of electron detrapping on the retention loss quantitatively, we calculated the amount of the corresponding charges. The detrapped charges (Q_{detrap}) during the first retention measurement can be estimated as

$$Q_{detrap} = C_{ox}\,\Delta V_{th,recovery}, \quad (1)$$

where $C_{ox} = \varepsilon WL/t_{ox}$ is the gate oxide capacitance of the Wtr and $\Delta V_{th,recovery}$ is the difference between the ΔV_{th} values in the first and second V_{th} extractions as shown in Fig.6(a). On the other hand, the charges related to the extra retention loss ($Q_{Ret,loss}$) can be estimated as

$$Q_{Ret,loss} = C_{tot}\,\Delta V_{Ret,loss}, \quad (2)$$

where C_{tot} is the total capacitance of the storage node, including the gate capacitance the Rtr and all the other parasitic capacitances [10], and $\Delta V_{Ret,loss}$ is the difference between the δV_{SN} values in the first and second retention measurements as shown in Fig.6(b).

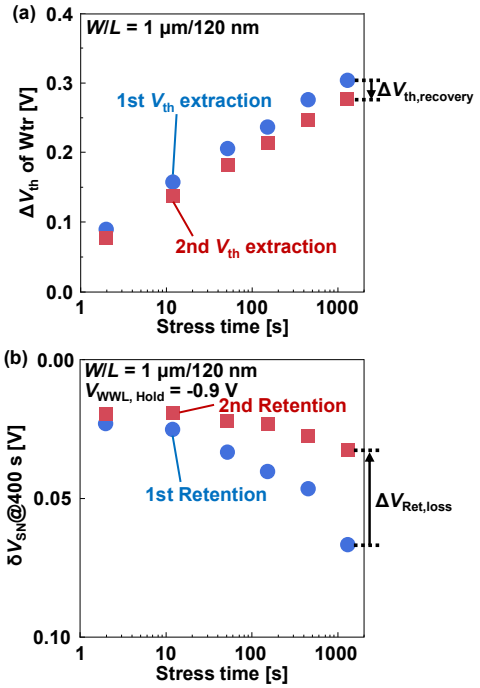

Fig.6 (a) PBTI degradation ΔV_{th} of the Wtr in the first and second V_{th} extractions as a function of stress time. The second ΔV_{th} was slightly smaller than the first ΔV_{th}. (b) Retention loss δV_{SN} after 400-s retention in the first and second retention measurements as a function of stress time. The second δV_{SN} is smaller than the first δV_{SN}.

Fig.7 presents the calculated Q_{detrap} and $Q_{Ret,loss}$ at the total stress time of 1300 s as a function of the $V_{WWL,Hold}$. No clear dependence of the Q_{detrap} on $V_{WWL,Hold}$ is observed, which suggests that detrapped electrons are associated with shallow traps in the gate oxide. Correspondingly, the $Q_{Ret,loss}$ shows no significant dependence on the $V_{WWL,Hold}$. This indicates that the electrons released from the shallow traps flow into the SN, causing the extra retention loss in the first retention measurement.

Fig.8 shows the correlation between the Q_{detrap} and $Q_{Ret,loss}$ for different Wtr channel widths W = 1 μm, 600 nm, and 180 nm, where each data point is their median for different $V_{WWL,Hold}$. Both the Q_{detrap} and the $Q_{Ret,loss}$ are smaller for narrower W, while the ratio $Q_{Ret,loss}/Q_{detrap}$ is greater than unity. This indicates that additional electrons are supplied from the regions other than gate oxide directly above the channel. One possible candidate for this region is the gate oxide on the sidewall of the CAAC-IGZO / TiN stacks on the SN side, because the thickness is ~ 4 nm slightly thinner than the nominal value of 5 nm [11]. Under the PBTI stress, more electrons can be trapped in that region; consequently, more electrons would be detrapped there. In practical memory operation, however, the contribution of the electron trapping and detrapping via the shallow traps can be mostly neglected, since short write pulses (~10 ns) with a small duty factor are applied to the gate of Wtrs [12].

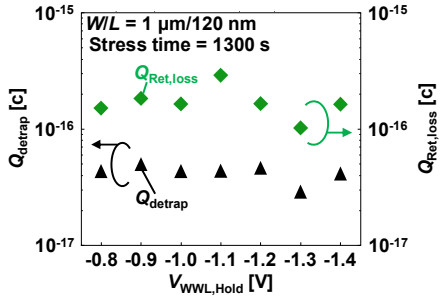

Fig.7 The detrapped charges (Q_{detrap}) during the first retention measurement and the charges related to the extra retention loss ($Q_{Ret,loss}$) as a function of $V_{WWL,Hold}$. The Q_{detrap} and $Q_{Ret,loss}$ are calculated using (1) and (2), respectively.

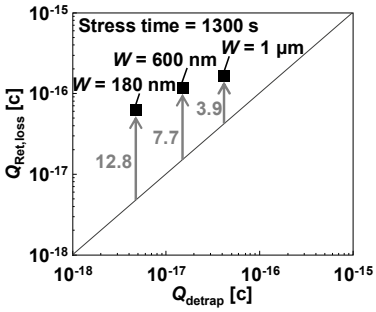

Fig.8 Correlation between $Q_{Ret,loss}$ and Q_{detrap} for different channel widghs (W = 180 nm, 600 nm, and 1 μm) and fixed channel length L = 120 nm or the Wtr. Both the $Q_{Ret,loss}$ and the Q_{detrap} decrease with narrower W, while the $Q_{Ret,loss}$ remains much larger than the Q_{detrap}. The numbers in the figure are $Q_{Ret,loss}/Q_{detrap}$ ratios.

B. Retention degradation due to gate leakage increase

In practice, the remaining component – the second δV_{SN} – after electron detrapping is more important. In Fig.9, $V_{WWL,Hold}$-dependence of the second δV_{SN} after the PBTI

stress is compared to that of the initial δV_{SN}. For stronger $V_{WWL,Hold}$, the δV_{SN} values both before and after PBTI stress increased, which is attributed to an increase of gate leakage current from the SN to the WWL node. This mainly occurs through the gate oxide on the sidewall of the SN in the gate-last IGZO TFTs [11]. The δV_{SN} further degraded after PBTI stress, which is more prominent under stronger $V_{WWL,Hold}$. This phenomenon corresponds to the so-called stress-induced leakage current (SILC). Electron injections during PBTI create electron traps in the gate oxide, which leads to an increase in leakage paths [13].

Typically, an endurance of 1×10^{15} write cycles is required for eDRAM. When assuming the PBTI model as $\Delta V_{th}(T, V_{ov}, t) \propto \exp(-E_A/k_BT)V_{ov}\gamma t^n$ using time kinetic factor (n = 0.2), voltage acceleration factor (γ = 5.2), and activation energy (E_A = 30 mV) in the electron trapping component of our IGZO TFTs [8], ΔV_{th} = 0.3 V at V_{ov} = 3.6 V, 1300 s and 25 °C is projected to be ΔV_{th} = 11 mV at V_{ov} = 1.5 V, 1×10^7 s (1×10^{15} cycles × 10 ns) and 95 °C. This value meets the industrial requirement, which is consistent with the result reported in Ref. [8] using the standard IGZO composition (1:1:1). Therefore, when using this composition, the impact of SILC on retention may not be observable under practical operation. Alternatively, this effect could be significant under different IGZO compositions such as Ga-rich one where electron trapping is enhanced [8].

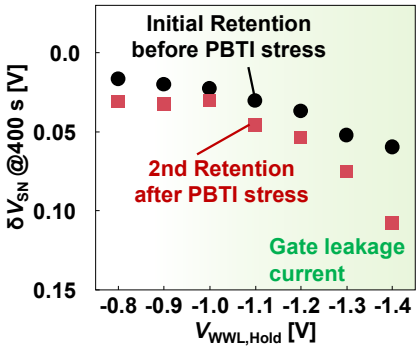

Fig.9 Retention loss δV_{SN} after 400-s retention in the initial retention measurement (before PBTI stress) and in the second retention measurement after 1300-s PBTI stress as function of hold voltage $V_{WWL,Hold}$. The δV_{SN} values after PBTI stress were larger than those befor PBTI stress, which is attributed to an inclease in gate leakage current.

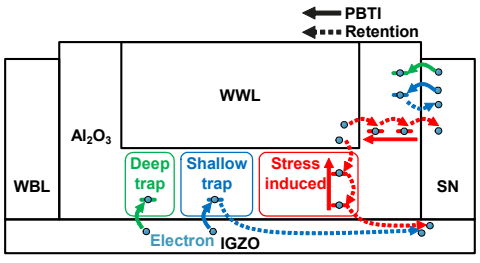

Fig.10 Two possible physical origins of the PBTI-induced retention degradation in IGZO-based 2T0C cells. During PBTI stress, electrons are trapped in deep and shallow traps of gate oxide Al_2O_3 on the IGZO channel and the sidewall of the SN (CAAC-IGZO / TiN stacks), while the gate oxide is damaged, resulting in the formation of new leakage paths. During retention with negative $V_{WWL,Hold}$, 1) the trapped electrons are released from the shallow traps and 2) gate leakage current flows through the additional leakage paths. These two processes can occur on both IGZO channel and the SN sidewall in the gate-last IGZO TFTs.

IV. Conclusion

Based on the measurement procedure developed in this work, we clarified that retention characteristics in 2T0C IGZO cells deteriorated during PBTI even at RT, caused by two possible physical origins (Fig. 10). First, the electrons trapped in shallow traps of the gate oxide due to PBTI stress are subsequently detrapped during retention with negative $V_{WWL,Hold}$ and flow into the SN. Second, PBTI stress creates additional leakage paths in the gate oxide, leading to an increase in gate leakage. The latter SILC corresponds to a permanent component, which could be critical under practical memory operation. Our findings establish the relationship between PBTI and retention behavior, supporting future eDRAM technology development.

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References

[1] A. Belmonte et al., "Capacitor-less, long-retention (>400s) DRAM cell paving the way towards lowpower and high-density monolithic 3D DRAM," in IEDM Tech. Dig., 2020, 28-2.

[2] A. Belmonte and G. S. Kar, "Disrupting the DRAM roadmap with capacitor-less IGZO-DRAM technology", Nature Reviews Electrical Engineering, vol. 2, pp. 220-221, 2025.

[3] W. Tang et al., "Low-Power and Scalable BEOL-Compatible IGZO TFT eDRAM-Based Charge-Domain Computing", IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 70, no. 12, pp. 5166-5179, 2023.

[4] F. Liao et al., "Novel 4F^2 Multi-bit Dual-gate 2T0C for High-density DRAM with Improved Vertical-channel IGZO TFTs by Self-aligned Single-step Process" in IEDM Tech. Dig., 2024, 6-7.

[5] J.-C. Chiu et al., "First Demonstration of a-IGZO GAA Nanosheet FETs Featuring Achievable SS=61 mV/dec, Ioff<10^{-7}μA/μm, DIBL=44 mV/ V, Positive V_T, and Process Temp. of 300°C" in Symp. VSLI Technol., 2023, T17-3.

[6] A. Chasin et al., "Understading and modelling the PBTI reliablity of thin-film IGZO transistor", in IEDM Tech. Dig., 2021, 31-1.

[7] Y. Zhao et al., "Fundamental understanding of NBTI degradation mechanism in IGZO channel devices", 2024 IEEE International Reliability Physics Symposium (IRPS), Grapevine, TX, USA, 2024, pp. 4A-1.

[8] A. Chasin et al., "Unraveling BTI in IGZO Devices: Impact of Device Architecture, Channel Film Deposition Method and Stoichiometry/Phase, and Device Operating Conditions" in IEDM Tech. Dig., 2024, 34-2.

[9] S. Subhechha et al., "Ultra-low leakage IGZOTFTs with raised source/drain for Vt > 0 V and Ion > 30 μA/μm," in Symp. VLSI Technol., 2022, T2-1.

[10] D. Matsubayashi et al., "Accurate off-current evaluation by parasitic capacitance extraction in capacitor-less DRAM cells" in IEEE IMW, 2025, pp.1-4.

[11] K. Izukashi et al., "On the frequency dependence of the bias temperature instability", IEEE Electron Device Lett., vol. 46, no. 7, pp.1111-1114. 2025.

[12] T. Grasser, B. Kaczer, H. Reisinger, P.-J. Wagner, and M. Toledano-Luque, "On the frequency dependence of the bias temperature instability", 2012 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, USA, 2012, pp. XT-8.

[13] A. I. Chou, K, Lai, K, Kumar, P. Chowdhury, and J. C. Lee, "Modeling of stress-induced leakage current in ultrathin oxides with the trap-assisted tunneling mechanism", Appl. Phys. Lett., 70, 3407 (1997).