Cryo-CMOS Reliability Lifetime Prediction and Extension via Cryogenic-Aware Forward Body Bias

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***Abstract*—We present the comprehensive cryogenic reliability assessment of 5-V thick-oxide transistors in a 160-nm CMOS process, investigating Bias Temperature Instability (BTI), Hot Carrier Degradation (HCD), and Time-Dependent Dielectric Breakdown (TDDB) at 4.2 K and comparing the results with the room-temperature behavior. We evaluate device lifetime under cryogenic operation and identify HCD as the dominant degradation mechanism, as its increased severity at low temperatures strongly limits the lifetime of nMOS devices. pMOS devices exhibit an HCD-induced threshold-voltage turnaround effect, which, although accelerated at 4.2 K, does not ultimately limit the cryogenic device lifetime. Furthermore, we demonstrate that device lifetime can be effectively extended through a cryogenic-aware Forward-Body-Biasing (FBB) strategy. These insights represent a valuable step toward reliability-aware design of integrated circuits operating in cryogenic environments, such as the electrical interfaces of quantum computers.**

***Index Terms*—cryo-CMOS, lifetime, BTI, HCD, TDDB, FBB.**

I. Introduction

Cryo-CMOS circuits are considered a key enabler to build large-scale quantum computers [1]. To exploit these circuits on a large scale, demonstrating their reliability is crucial. Previous studies have shown that common reliability mechanisms, such as Bias Temperature Instability (BTI) [2]–[4], Hot Carrier Degradation (HCD) [5]–[8], and Time-Dependent Dielectric Breakdown (TDDB) [9], also affect transistors at cryogenic temperatures, but with distinct characteristics and more strongly technology-dependent severity than at higher temperatures. Most studies focused on individual degradation mechanisms in a specific technology (see Fig. 1). In contrast, this work assesses the severity of BTI, HCD, and TDDB on the same technology, enabling a direct comparison of their impact at 300 K and 4.2 K. The goal is to evaluate their relative severity as a function of temperature and device type, identify lifetime-limiting mechanisms in the cryogenic regime, and explore strategies to mitigate their degradation to extend their lifetime. Our study presents the cryogenic reliability characterization of thick-oxide 5-V MOSFETs fabricated in a 160-nm CMOS technology. By supporting higher operating voltages than scaled-down technologies, these devices are well-suited for high-voltage cryo-CMOS qubit interfaces, such as those required for ion-trap [10] and color-center qubits [11].

Although our earlier work reported preliminary investigations of BTI [4] and HCD [8], the characterization was not sufficiently comprehensive to allow meaningful lifetime predictions. Here, we address this gap by providing the first unified characterization of BTI, HCD, and TDDB for the same technology, enabling reliable lifetime prediction. For BTI, we extract and model the non-recoverable component of the threshold-voltage degradation. We also present the first measurements of TDDB at 4.2 K in this technology node, showing that TDDB is less severe at 4.2 K than at 300 K and does not threaten device lifetime. To confirm the tentative hypothesis of HCD-induced threshold-voltage turnaround effect in pMOS devices [8], we present extended measurements with stress times up to 200 ks to demonstrate its existence and analyze its influence on the lifetime of pMOS devices subject to HCD. Finally, we identify, among all possible degradation mechanisms, the increased cryogenic severity of HCD in nMOS devices as the limiting factor for device lifetime at 4.2 K. To counteract this effect, we demonstrate, for the first time, the use of cryogenic-aware forward body bias (FBB) [12] to reduce the impact of HCD in nMOS devices, showing that it can successfully increase device lifetime at 4.2 K.

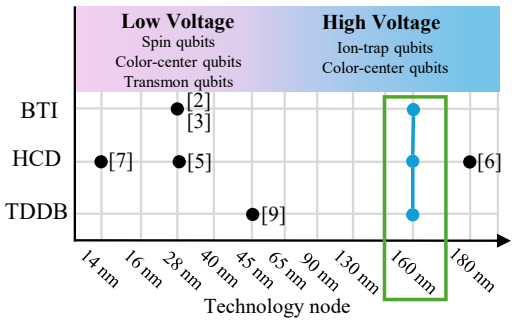


Fig. 1: Reliability mechanisms investigated across different cryo-CMOS technology nodes. The 160-nm node investigated in this work is highlighted.

II. Measurement Methods and Devices

In this study, single-transistor characterizations are performed, ensuring direct access to each device without a multiplexing structure. Every chip contains six transistors of width $W = 10\,\mu\text{m}$: three nMOS (N1-3) of lengths $L_{\text{N1}} = 10\,\mu\text{m}$, $L_{\text{N2}} = 1.2\,\mu\text{m}$, and $L_{\text{N3}} = 0.6\,\mu\text{m}$; three pMOS (P1-3) of lengths $L_{\text{P1}} = 10\,\mu\text{m}$, $L_{\text{P2}} = 1.2\,\mu\text{m}$, and $L_{\text{P3}} = 0.5\,\mu\text{m}$. All measurements are performed on fresh transistors. Each chip is set to the target temperature, and the measurements

are carried out using the selected stress voltage. Once all transistors on a chip are characterized, a new chip is used for the successive measurement conditions. The chip under test is wire-bonded, packaged, and mounted on a PCB connected to a dipstick, which is used to immerse the chip in liquid Helium during cryogenic measurements, reaching a temperature of 4.2 K. Measurements were performed using a B1500A Semiconductor Device Parameter Analyzer.

III. Results and Discussion

A. Bias Temperature Instability (BTI)

BTI was characterized using the extended Measure-Stress-Measure (eMSM) method [4], in which stress and measurement phases are alternated. Unlike other technology nodes where some defects freeze out leading to negligible BTI at 4.2 K [2]–[3], BTI degradation is observable at cryogenic temperature for both nMOS and pMOS devices [4]. However, BTI is significantly reduced in pMOS transistors at 4.2 K, whereas in nMOS devices it remains of the same order of magnitude as at 300 K, thereby potentially limiting cryogenic operation. After each stress phase, the threshold voltage shift (ΔV_{th}) exhibits logarithmic recovery. In this work, we extract and model the non-recoverable component of BTI degradation for device lifetime prediction. While a significant fraction of the threshold-voltage shift is recoverable, this component strongly depends on timing, recovery conditions, and device operation. For this reason, only the non-recoverable component is used in the proposed technology-oriented lifetime modeling and estimation, as is common in the literature. The non-recoverable component $\Delta V_{\mathrm{th,BTI-NR}}$ shown in Fig. 2 follows a power-law trend with time:

$$\Delta V_{\mathrm{th,BTI-NR}} = A_{\mathrm{BTI}} \cdot t^{\alpha} \tag{1}$$

where A_{BTI} and α are fitting parameters depending on the stress voltage applied at the gate, temperature and device type. Even though the recoverable component does not contribute to permanent device degradation, it could potentially lead to severe temporary errors. However, since application-specific assumptions on duty cycle and recovery dynamics are fundamental for such circuit-level reliability assessment, this is left for follow-up studies.

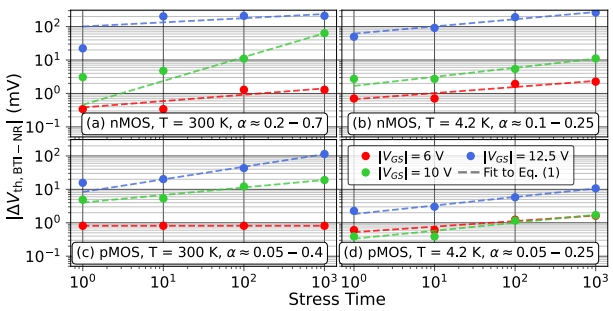


Fig. 2: Non-recoverable component of BTI-induced $|\Delta V_{\mathrm{th}}|$. The curves are the average $|\Delta V_{\mathrm{th}}|$ obtained from devices of the three different dimensions.

B. Hot Carrier Degradation (HCD) and its mitigation via cryogenic-aware Forward Body Bias (FBB)

HCD was characterized using the Measure-Stress-Measure (MSM) method to assess the degradation of V_{th} and current. As shown in Fig. 3, a positive ΔV_{th} (corresponding to a reduction in $|V_{\mathrm{th}}|$) is observed in the measured pMOS devices suggesting the presence of a turnaround effect [13] for the first time at 4.2 K [8]. Extended measurements with stress times up to 200 ks (corresponding to a 40× increase compared to previous stress times) confirm the occurrence of the turnaround. The degradation exhibits two distinct phases, as shown in Fig. 4. In the first phase (highlighted by the fitting in Fig. 4), V_{th} shifts toward less negative values (i.e., positive ΔV_{th}), accompanied by an increase in the drain current, also shown in Fig. 5. This initial behavior is attributed to the accumulation of negative charges in the oxide. At longer stress times, positive charges associated with interface trap generation progressively compensate for this effect, eventually dominating the degradation. As a result, the V_{th} shifts toward more negative values, leading to a reduction in the drain current. These results provide important insights for pMOS lifetime prediction, as the initial phase prior to the turnaround can induce a positive ΔV_{th} large enough to cause circuit failure. The HCD-induced ΔV_{th} degradation in pMOS can be modeled with two competing power laws:

$$\Delta V_{\mathrm{th,HCD,P}} = A_{\mathrm{HCD,P}} \cdot t^{\beta} - B_{\mathrm{HCD,P}} \cdot (t - t_{\mathrm{TA}})^{\gamma} \tag{2}$$

where $A_{\mathrm{HCD,P}}$ and $B_{\mathrm{HCD,P}}$ are fitting parameters depending on the stress voltage applied at the drain and temperature, β

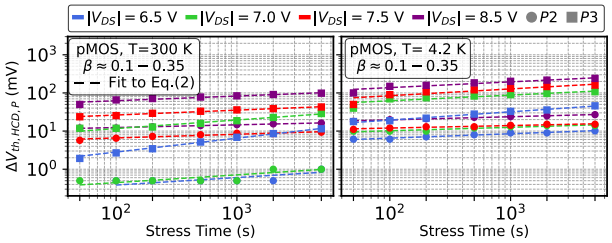


Fig. 3: HCD-induced V_{th} shift for pMOS devices. P1 shows no HCD effects, independently on temperature and stress voltage.

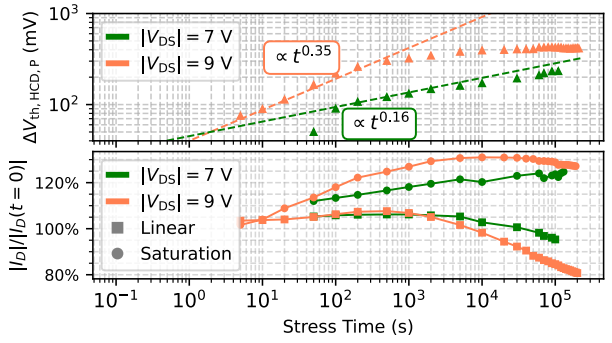


Fig. 4: HCD-induced turnaround effect at 4.2 K in ΔV_{th} (top) and drain current (bottom) in the linear ($|V_{\mathrm{DS}}| = 100\,\mathrm{mV}$) and saturation ($|V_{\mathrm{DS}}| = 3\,\mathrm{V}$) regimes for a $|V_{\mathrm{GS}}| = 3\,\mathrm{V}$ in P3.

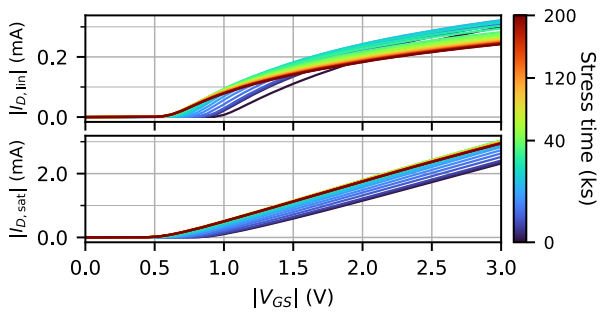


Fig. 5: HCD-induced turnaround effect at 4.2 K in drain current degradation for P3 in the linear ($|V_{\mathrm{DS}}|$ = 100 mV) and saturation ($|V_{\mathrm{DS}}|$ = 3 V) regimes for a stress voltage $|V_{\mathrm{DS}}|$ = 9 V.

and γ are fitting exponents of the negative charge and positive charge contribution, respectively, and t_{TA} is the time at which the turnaround starts taking place.

In nMOS devices, HCD effects significantly worsen at 4.2 K (see Fig. 6). The HCD-induced ΔV_{th} can be modeled with a power law:

$$\Delta V_{\mathrm{th,HCD,N}} = A_{\mathrm{HCD,N}} \cdot t^{\delta} \tag{3}$$

where $A_{\mathrm{HCD,N}}$ and δ are fitting parameters depending on the stress voltage applied at the drain and temperature. While at room temperature $\delta \approx 0.2 - 0.3$, in the cryogenic regime it increases significantly, becoming $\delta \approx 0.75 - 0.9$.

The increased HCD severity at very low temperatures raises concerns about long-term cryogenic circuit operation and suggests investigating mitigation strategies. In [6], FBB was shown to be ineffective in extending the lifetime of nMOS devices at 4.2 K, primarily due to the onset of the kink effect and limited bulk-source voltage. We demonstrate, for the first time at 4.2 K, how cryogenic-aware Forward Body Bias (FBB) [12] can be effectively used to reduce HCD in nMOS: the increased bulk diode turn-on voltage at 4.2 K allows the application of much higher FBB voltage than at 300 K during stress phases. As shown in Fig. 7, HCD effects are successfully reduced in nMOS at 4.2 K by applying an FBB of 1 V during the stress phase. At room temperature, such a high voltage cannot be applied and an FBB of 0.5 V does not provide comparable mitigation.

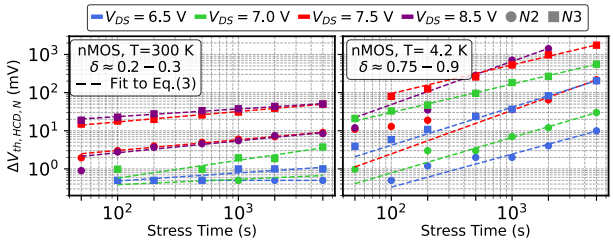


Fig. 6: HCD-induced V_{th} shift for nMOS devices. N1 shows no HCD effects. N3 at V_{DS} = 8.5 V for T = 4.2 K does not survive the first stress phase.

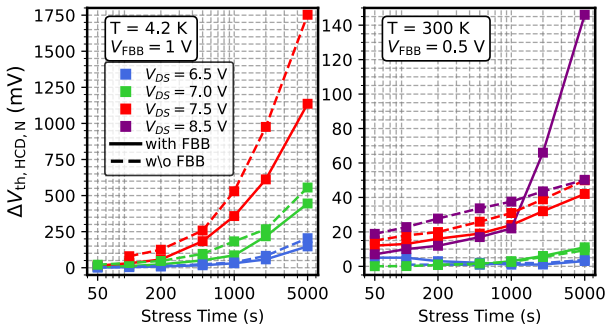


Fig. 7: Effect of FBB on HCD-induced ΔV_{th} in N3. Left: at 4.2 K FBB can be pushed to 1 V and effectively reduces ΔV_{th}. Right: at 300 K FBB is limited to 0.5 V and shows little to no improvement.

C. Time-Dependent Dielectric Breakdown (TDDB)

TDDB measurements were performed using a constant stress voltage and monitoring the gate current. As shown in Fig. 8, TDDB is generally slower at cryogenic temperatures, due to the lower defect generation rate [9], making this failure mechanism less severe than at room temperature. TDDB is therefore not the limiting factor in the lifetime of cryo-CMOS devices. TDDB also takes place more rapidly in devices with larger areas. For this reason, the measurements for the larger area devices (N1 and P1) have been used for lifetime extrapolation, as shown in Fig. 9.

IV. Lifetime Prediction and Extension

The models presented in the previous sections have been used to perform lifetime predictions, where the end-of-life is defined as a ΔV_{th} of 10 mV for BTI and HCD. Fig. 10a shows that the 10-year lifetime requirement of the non-recoverable

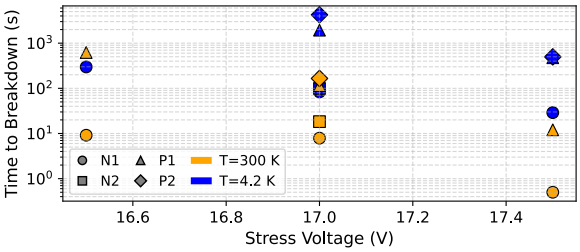


Fig. 8: Time to breakdown under constant gate-voltage stress for nMOS and pMOS devices at 300 K and at 4.2 K.

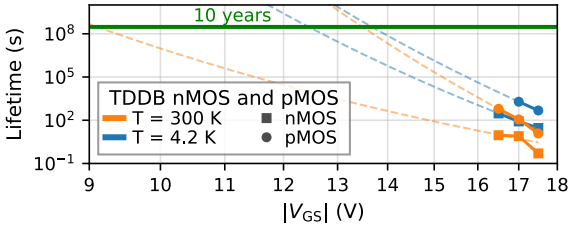
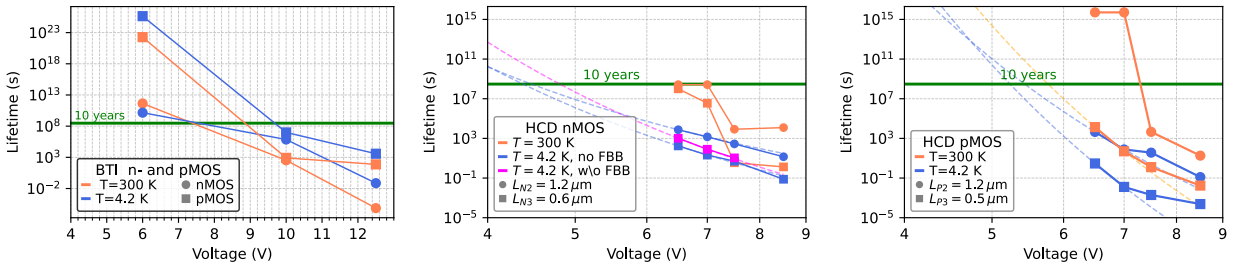


Fig. 9: Lifetime extrapolation for nMOS and pMOS devices subject to TDDB. The largest-area devices (N1 and P1) have been used for lifetime prediction as they represent the worst-case scenario.



(a) Lifetime for BTI in n- and pMOS devices. (b) Lifetime for HCD in nMOS devices. (c) Lifetime for HCD in pMOS devices.

Fig. 10: Lifetime prediction, where the end-of-life is defined as $\Delta V_{\mathrm{th}} = 10\,\mathrm{mV}$. For BTI, the 10-year goal is already reached for voltages higher than V_{DD} (5 V). The first phase before the turnaround is considered for pMOS HCD lifetime prediction. As HCD in nMOS is the limiting factor, FBB successfully extends the lifetime and, when devices are operated at a maximum of 4.5 V (90 % of V_{DD}), they can reach the 10-year lifetime requirement with a wide margin.

component of BTI degradation is met already for voltages higher than V_{DD} (5 V). pMOS devices have a longer lifetime at 4.2 K in case of BTI degradation compared to room temperature, while the effect is comparable for nMOS. Fig. 10b and Fig. 10c show the lifetime prediction for HCD in nMOS and pMOS devices, respectively. The lifetime extrapolations are performed according to the models in Section III, where the stress-dependent parameters are modeled using the following stress-voltage dependence [6] for :

$$\Delta V_{\mathrm{th}} \propto exp\left(\frac{D}{V_{\mathrm{Stress}}}\right) \tag{4}$$

where D is a fitting parameter and V_{Stress} is the stress voltage. In this technology, HCD effects in pMOS are driven by contrasting charge accumulations causing the turnaround, making them quite resilient. The limiting factor for the lifetime is instead HCD in nMOS devices at 4.2 K, as they do not meet the 10-year lifetime requirement. While cryogenic-aware FBB mitigation brings performance close to the target, combining FBB with a 10% reduction in V_{DD} provides an adequate reliability margin in the cryogenic regime, where HCD effects are more severe, as summarized in Fig. 11.

V. Conclusions

This paper reports the first comprehensive cryogenic reliability evaluation at 4.2 K, assessing the impact of BTI, HCD, and TDDB effects on 160-nm, 5-V thick-oxide CMOS transistors. Our results show that pMOS devices remain quite reliable in the cryogenic domain, while HCD dominates the degradation of nMOS devices at 4.2 K, significantly limiting device lifetime compared to BTI and TDDB. To counteract such degradation, cryogenic-aware FBB can effectively extend transistor lifetime. Combined with a reduction of 10% in operating voltages, this technique provides a viable strategy for reliable large-scale cryo-CMOS circuits. These findings provide key insights to support reliability-aware cryo-CMOS circuit design for long-term operation in highly integrated quantum computing systems.

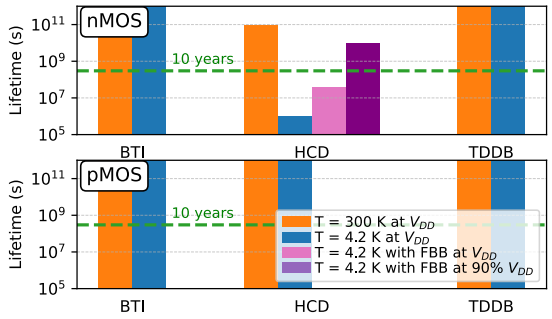


Fig. 11: Summary of lifetime predictions for BTI, HCD ($\Delta V_{\mathrm{th}} = 10\,\mathrm{mV}$), and TDDB. At 4.2 K, HCD limits the lifetime of devices. FBB extends it, allowing to reach the 10-year requirement, if devices are operated for voltages lower than 4.5 V (90% of nominal V_{DD}).

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