A 12-bit 2-GS/s 2× TI Pipelined-SAR ADC Using a Passive T/H with kT/C Cancellation and Pre-Sampling Bootstrap

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***Abstract*—This paper presents a 12-bit 2-GS/s power-efficient two-channel time-interleaved (TI) pipelined-SAR ADC. The architecture employs a low-power passive track-and-hold (T/H) front-end, which inherently eliminates the need for TI timing-skew calibration. To address the signal attenuation and nonlinearity of passive T/H, a parallel and bandwidth-unlimited kT/C cancellation technique and a pre-sampling bootstrap switch are proposed. Fabricated in 28-nm CMOS, the prototype achieves 59.4-dB SNDR at the Nyquist input. It consumes 16.1 mW (including reference buffer), yielding a state-of-the-art 167.3 dB FoMS and 10.6 fJ/conv-step FoMW among ADCs with >50 dB SNDR and ⩾2 GS/s sampling rate.**

Keywords—Passive T/H, time-interleaved, kT/C cancellation, bootstrap switch.

I. Introduction

Modern wireless communication and radar systems increasingly demand multi-GS/s high-resolution ADCs for direct digitization of wideband RF signals. Time-interleaved (TI) ADCs provide a promising solution for high-speed conversion but suffer from channel mismatches, particularly time skew. While a front-end track-and-hold (T/H) stage can intrinsically eliminate skew errors, implementing a high-speed T/H remains a significant challenge. Traditional source-follower-based T/Hs suffer from high power consumption and limited linearity [1]. Conversely, passive T/Hs [2] achieve superior energy efficiency but face two critical bottlenecks: signal attenuation caused by the large sampling capacitor of ADC core required for kT/C noise suppression, and nonlinearity induced by the signal-dependent parasitic capacitances of the sampling switches as shown in Fig. 1.

To mitigate signal attenuation in passive T/Hs, a parallel and bandwidth-unlimited kT/C noise cancellation technique is introduced, enabling the use of a small sampling capacitor. Although a smaller capacitor reduces attenuation, the resulting increase in kT/C noise is effectively suppressed by the proposed cancellation scheme. Moreover, the passive T/H converts the input signal into DC, thereby eliminating the input bandwidth limitation typically introduced by kT/C noise cancellation as in [3]. As a result, the passive T/H and kT/C cancellation are complementary.

To improve linearity, a pre-sampling bootstrap technique is employed. By maintaining nearly constant gate-to-source (V_{gs}) and gate-to-drain (V_{gd}) voltages, the nonlinearity induced by the parasitic capacitances of the sampling switch is significantly reduced. Unlike conventional bootstrap schemes, the proposed technique pre-samples the input signal

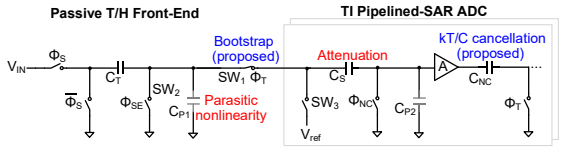

Fig. 1 TI pipelined-SAR ADC with passive T/H front-end and techniques for mitigating attenuation and parasitic-induced nonlinearity.

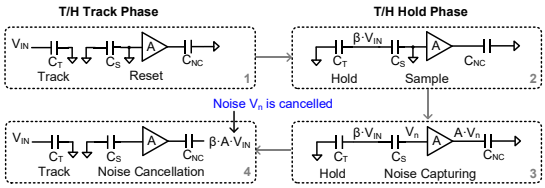

Fig. 2 Operation of the proposed kT/C cancellation.

to avoid additional loading on the T/H, eliminating extra attenuation and nonlinearity.

The kT/C cancellation and pre-sampling bootstrap jointly enable a passive T/H with low attenuation and high linearity. Leveraging this front-end, the 12b 2× TI pipelined-SAR ADC achieves a 2-GS/s sampling rate without skew calibration while consuming 16.1 mW. At Nyquist input, the ADC achieves an SNDR of 59.4 dB and an SFDR of 73.9 dB, corresponding to a FoM_S of 167.3 dB and a FoM_W of 10.6 fJ/conversion-step.

II. Proposed Low-Attenuation and High-Linearity Passive Track-and-Hold

The detailed block diagram of the TI pipelined-SAR ADC with a passive T/H is shown in Fig. 1. The input signal V_{IN} is sampled onto capacitor C_T and then transferred to the ADC sampling capacitor C_S. To reduce transfer attenuation, C_S is minimized. Although this increases the associated kT/C noise, the proposed kT/C noise cancellation effectively suppresses it, preserving a large signal amplitude at the ADC input and improving the overall SNR.

Another key challenge in passive transfer is the nonlinearity introduced by the parasitic capacitances of the switches (SW_1–SW_3) in the transfer net, as shown in Fig. 1. The parasitic capacitances of switch (C_{gs} and C_{gd}) are significantly larger in the on-state than in the off-state [4]. During the transfer phase, only SW_1 is on, and its parasitics dominate the overall nonlinearity. To address this issue, SW_1 employs a pre-sampling bootstrap technique that maintains nearly constant V_{gs} and V_{gd}. As a result, the variations in C_{gs} and C_{gd} are minimized, significantly improving the linearity of the passive T/H.

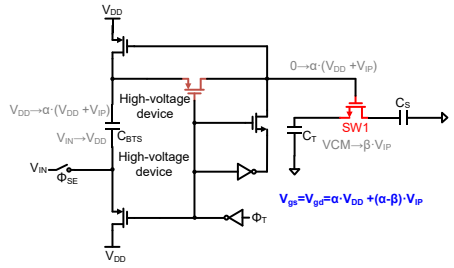

Fig. 3 Proposed pre-sampling bootstrap switch

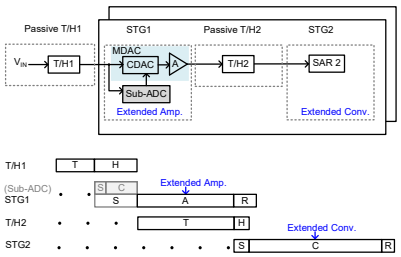

Fig. 4 Pipelined architecture based on passive T/H enabling extended first-stage amplification and second-stage conversion time.

A. *Proposed kT/C Cancellation*

The operation of the proposed kT/C noise cancellation is illustrated in Fig. 2, consisting of four steps. First, during the track phase, the input signal is sampled onto the passive T/H capacitor C_T, while the first-stage sampling capacitor C_S is reset. Second, during the hold phase, the left plate of C_S is connected to C_T, sampling the held voltage with a gain of $C_T/(C_T + C_S)$. Third, the right plate of C_S is disconnected from the reset voltage, generating a kT/C noise voltage Vn at the amplifier input, which is amplified and stored on the left plate of the noise-storage capacitor C_{NC}. Finally, the first stage transfers and amplifies the signal to the right plate of C_{NC}, thereby cancelling the stored noise Vn. The proposed kT/C noise cancellation enables the use of a small first-stage sampling capacitor C_S, reducing the attenuation of the passive T/H. Moreover, it facilitates reference-friendly operation, as C_S is reused as the DAC capacitor for residue generation.

The proposed kT/C noise cancellation operates in parallel with first-stage sampling and does not limit the input bandwidth, making it well suited for high-speed and wideband applications. In [3], kT/C noise cancellation enables a small DAC for easier driving. However, the input bandwidth is limited due to amplifier saturation caused by signal variations during noise capture. In [5], kT/C noise is captured in a separate phase to avoid saturation, at the cost of reduced speed. In addition, the split sampling disrupts the high-linearity property enabled by bottom-plate early turn-off. In the proposed architecture, the passive T/H converts the input signal into DC, preventing bandwidth limitations during noise capture. Furthermore, the kT/C noise cancellation is performed in parallel with first-stage sampling, avoiding additional phases and thus maintaining high-speed operation. In contrast to [3] and [5], the proposed scheme does not impose bandwidth limitations nor introduce additional phases.

Therefore, the proposed kT/C noise cancellation and passive T/H are complementary. The kT/C cancellation mitigates attenuation in the passive T/H, while the passive T/H eliminates the bandwidth limitation associated with kT/C noise cancellation. Moreover, the interstage amplifier of the pipelined-SAR ADC is reused during its idle phase for kT/C noise cancellation, incurring minimal additional overhead. Although the kT/C noise cancellation does not introduce additional phases, it requires a longer operation time than passive transfer, slightly reducing the speed of the passive T/H.

B. *Proposed Pre-sampling Bootstrap Switch*

In the design, a bootstrap control signal is required to drive SW_1 in Fig. 1 to reduce the variation of C_{gs} and C_{gd} during voltage transfer. However, directly using the held signal for bootstrapping introduces additional attenuation and nonlinearity. To address this issue, a pre-sampling bootstrap switch is proposed, as shown in Fig. 3. During the track phase, the bootstrap capacitor C_{BTS} samples the input signal V_{IN} concurrently with the T/H sampling capacitor C_T. During the transfer phase, the bottom plate of C_{BTS} is switched to V_{DD}. Since the common-mode voltage of the differential input is $V_{DD}/2$, the resulting voltage variation at the bottom plate is V_{IP}. Considering parasitic effect, the top plate voltage of C_{BTS}, which serves as the control signal of SW_1, becomes $\alpha\cdot(V_{DD} + V_{IP})$, where α denotes the attenuation factor due to parasitics.

Accordingly, the V_{gs} and V_{gd} of SW_1 can be expressed as $\alpha\cdot V_{DD} + (\alpha - \beta)\cdot V_{IP}$, where β is the attenuation factor of the passive T/H. By designing $\alpha = \beta$, the signal-dependent term is eliminated, and both V_{gs} and V_{gd} reduce to $\alpha\cdot$VDD, independent of the input signal. This significantly suppresses the variation of parasitic capacitances and improves the linearity of the passive T/H.

The overhead of the pre-sampling bootstrap switch is the additional load introduced by C_{BTS} to the input buffer. Fortunately, C_{BTS} can be kept small, making this overhead negligible. Moreover, the bootstrap switch loads the input buffer rather than the passive T/H, thereby avoiding degradation of the passive T/H gain and linearity.

III. Timing-Relaxed Pipelined Architecture Based on Passive T/H

Another advantage of the passive T/H is its short transfer time enabled by charge sharing, compared to active T/H implementations. This feature is leveraged to reduce the effective sampling time in both stages of the single-channel pipelined-SAR ADC, as shown in Fig. 4.

In the proposed architecture, although the first stage samples the T/H1, its sampling time is slightly extended due to the kT/C noise cancellation. To address this issue, a sub-ADC is introduced in the first stage. The sub-ADC samples T/H1 within a short time window and immediately starts conversion, while the MDAC of the first stage continues sampling. After the sub-ADC completes conversion, its output is directly used by the MDAC for residue amplification. In this way, the long MDAC sampling period is reused for conversion, reducing the effective sampling time to the short sub-ADC sampling window.

In a conventional pipelined-SAR ADC, the sampling time of the second stage is constrained by the long residue amplification phase. An additional T/H stage (T/H2) is typically inserted between the two stages, as in [6]. With T/H2, the residue from the first stage is sampled during the amplification phase and transferred to the second stage within a short time window.

With the proposed structure, the first-stage amplification and second-stage conversion are extended, relaxing the

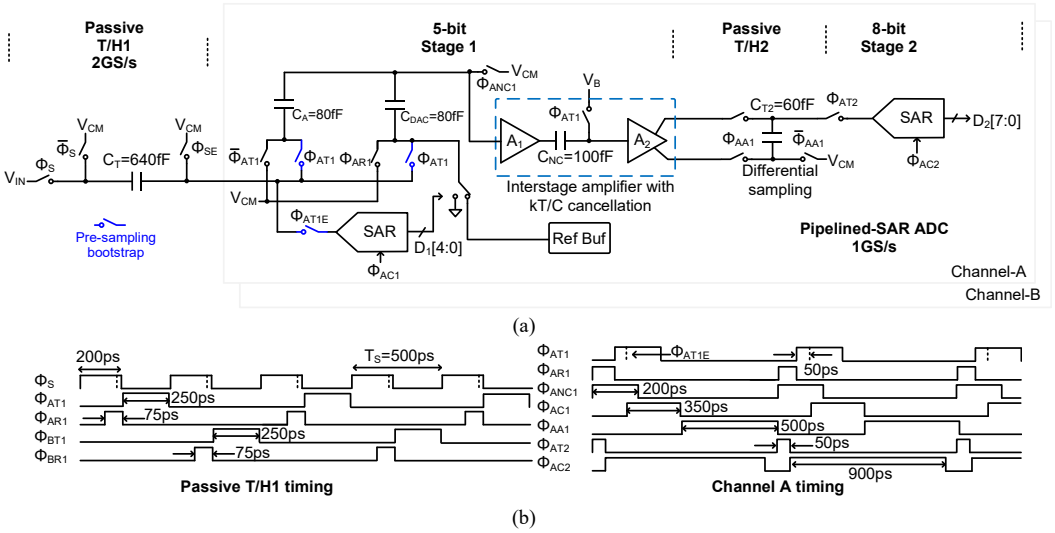

Fig.5 The proposed 12bit 2GS/s 2× TI Pipelined-SAR ADC: (a) Block diagram and (b) timing diagram.

timing constraints of both stages. The additional T/H stage introduces a latency overhead of half a clock cycle. With the two-stage pipelined-SAR architecture, the per-channel latency increases from two to four pipeline stages, yet remains lower than that of conventional deep-pipelined designs.

IV. Implementation of the Proposed 2× TI Pipelined-SAR ADC with Passive T/H

The block and timing diagram of the proposed TI pipelined-SAR ADC are shown in Fig. 5 The design integrates a 2GS/s passive T/H1 and two 1GS/s 12-bit pipelined-SAR ADCs. Each channel is configured as a 5b first stage and an 8b second stage with 1b interstage redundancy, connected by a passive T/H2. T/H1 employs a 640fF C_T with bottom-plate sampling to achieve low-noise and high-linearity sampling. The first-stage MDAC adopts a 160fF C_S to sample T/H1 with 0.8 attenuation, while the induced kT/C noise is cancelled. The pre-sampling bootstrap switch introduces an additional 45 fF load to the input buffer, increasing the total input capacitance from 750 fF (640 fF from T/H1 and 110 fF parasitics) to 795 fF, corresponding to a 6% increase in input loading.

For improved DAC operation, the reference is boosted to 0.8V driven by a flipped-voltage-follower (FVF) buffer. Only 80fF of C_S is used for DAC operation, corresponding to a 1Vpp ADC full swing. The sub-ADC is a 5-bit SAR ADC with two comparators operating alternately to accelerate conversion, with their offsets corrected through background calibration. Owing to the small residue from the 5-bit first stage, the interstage amplifier employs two gm-R stages with gain of 10, providing sufficient linearity. Considering the 0.8 attenuation caused by parasitics, the nominal interstage gain is 8. A 100fF C_{NC} is inserted between the two amplifier stages for noise storage. The second stage is a conventional 8-bit SAR ADC with 60fF sampling capacitor. The passive T/H2 with 60fF sampling capacitor adopts differential sampling [6] to compensate for 0.5 attenuation of passive transfer.

The conversion sequence begins with T/H1 sampling for 200ps, followed by 250ps of first-stage sampling. The bottom plate of C_S connects to C_T for 250ps, while top plate is reset to V_{CM} during the first 125ps. In the subsequent 125ps, the kT/C noise on the top plate is amplified and stored on C_{NC} for

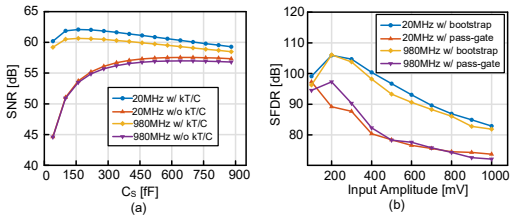

Fig. 6 Simulated performance: (a) ADC SNR versus first-stage sampling capacitor C_S; (b) SFDR of the passive T/H front-end versus input amplitude.

cancellation. Simultaneously, the sub-ADC samples T/H1 for only 50ps and completes 5b conversion in 350ps. The residue is subsequently amplified and transferred to T/H2. Afterwards, the second stage samples the T/H2 output in 50ps and performs the 8-bit conversion in 900ps. The first and second stages require 75ps and 50ps, respectively, for reset before reconnecting to the T/H.

With these T/H stages enabling fast sampling, the first-stage amplification and second-stage conversion time are extended to 500ps and 900ps. Benefiting from kT/C noise cancellation, the first-stage sampling capacitor is minimized to 160fF, achieving a reduced T/H1 attenuation of 0.8. Moreover, the reference buffer with a 500μA bias current is sufficient to drive the 80fF DAC. Besides, the pre-sampling bootstrap switch improves the linearity of the passive T/H1.

With a 1 Vpp input, the simulated SNR results of the ADC are shown in Fig. 6(a). The proposed kT/C noise cancellation improves the maximum SNR by 4.5 dB at 20 MHz and 3.7 dB at 980 MHz compared to the case without cancellation. This improvement arises from two factors. First, the use of a small C_S reduces the attenuation of the passive T/H, thereby suppressing the noise contribution from the pipelined-SAR ADC core. Second, the increased kT/C noise associated with the small C_S is effectively cancelled by the proposed technique. With kT/C cancellation, the optimal first-stage sampling capacitor C_S is approximately 160 fF, indicating a trade-off rather than monotonic improvement with decreasing C_S. This is because reducing C_S mitigates the attenuation of the passive T/H, but increases the signal attenuation caused by the parasitic capacitance C_{P2} at the amplifier input (Fig. 1).

Fig. 6(b) shows that the proposed pre-sampling bootstrap technique improves the SFDR from 73.7 dB to 82.9 dB at 20

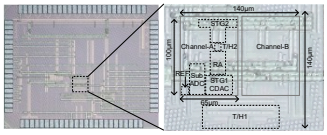

Fig. 7 Die photo.

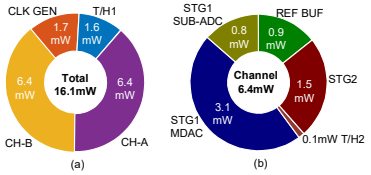

Fig. 8 Power breakdown.

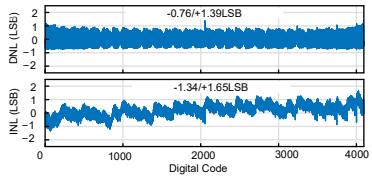

Fig. 9 Measured DNL and INL

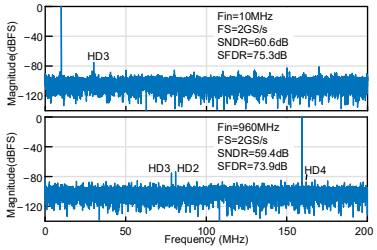

Fig. 10 Measured output spectra (decimated by 5).

MHz and from 72.1 dB to 81.9 dB at 980 MHz, compared to a conventional pass-gate switch, demonstrating improved linearity of the passive T/H.

V. Measurement Results

The prototype ADC is implemented in a 28-nm CMOS process and occupies an active area of 0.02 mm² (Fig. 7). The first-stage CDAC mismatch is corrected using foreground calibration, while the interstage gain error is calibrated off-chip in the background. Offset and gain mismatches between the two channels are calibrated by comparing long-term averages. The ADC consumes 16.1 mW from a 1 V supply at 2-GS/s, including 1.6 mW for T/H1, 12.8 mW for the two channels, and 1.7 mW for clock generation (Fig. 8). For each channel, the core consumes 5.5 mW and the reference buffer consumes 0.9 mW. Fig. 9 shows the measured DNL and INL, with DNL ranging from −0.76 to 1.39 LSB and INL ranging from −1.34 to 1.65 LSB. The measured output spectra with a decimation factor of 5 at 10 MHz and 960 MHz inputs are shown in Fig. 10. The measured Nyquist SNDR is 59.4 dB, corresponding to a FoM_S of 167.3 dB and a FoM_W of 10.6 fJ/conversion-step. Fig. 11 shows the SNDR versus input frequency and the multi-chip measurement results under different supply voltages at a 10 MHz input.

Table I summarizes the performance of the proposed ADC and compares it with state-of-the-art high-speed and high-resolution designs. This work achieves 12-bit resolution at 2-GS/s without TI skew calibration while consuming only 16.1 mW. Fig. 12 shows the FoM comparison, indicating that this work achieves the highest FoM_S and FoM_W among

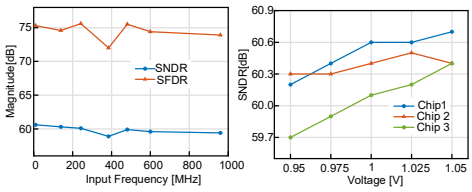

Fig. 11 Measured SNDR versus input frequency and multi-chip performance under different supply voltages.

TABLE I PERFORMANCE SUMMARY AND COMPARISON OF STATE-OF-THE-ART HIGH-SPEED AND HIGH -RESOLUTION ADCS

	This work	Y.Cao ISSCC'23	M.Gu ISSCC'25	Y.Cao ISSCC'24	B.Rui VLSI'25	B.Hershberg ISSCC'19
Architecture	T/H Assisted TI Pipe-SAR	Pipe	Pipe	×4 TI Pipe	Pipe	×4 TI Pipe
Process [nm]	28	28	28	28	28	16
Area [mm²]	0.02	0.034	0.04	0.24	0.1368	0.194
Supply [V]	1	1	1	1	1	0.85
Resolution [bit]	12	12	12	12	14	13
fs [GS/s]	2	2	3	12	3	3.2
fs/Channel [GS/s]	1			3		0.8
SNDR @ Nyq. [dB]	59.4	60.4	58.8	54.1	62.3	61.7
SFDR @ Nyq. [dB]	73.9	75.8	70.7	66.0	81.1	73.3
Power [mW]	16.1	27.0	32.5	179.8	125.4	61.3
FoM_S [dB]	167.3	166	165	159	163.1	165.9
FoM_W [fJ/conv-step]	10.6	15.8	15.2	36.2	39.1	19.3
Skew Cal. Required	No	No	No	Yes	No	Yes

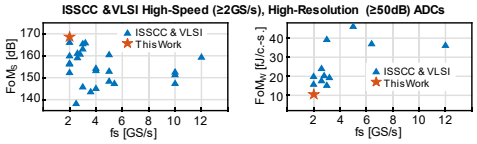

Fig. 12 FoM comparison among ADCs with SNDR > 50 dB and sampling rates ⩾ 2 GS/s.

reported ADCs with SNDR > 50 dB and sampling rates ⩾ 2 GS/s. These results demonstrate the power efficiency of the proposed TI pipelined-SAR ADC with a low-attenuation and high-linearity passive T/H.

VI. Conclusion

This work proposes kT/C noise cancellation and a pre-sampling bootstrap technique to realize a low-attenuation and high-linearity passive T/H. Leveraging this front-end, a 2× TI pipelined-SAR ADC achieves 12-bit resolution at 2-GS/s without skew calibration. The prototype achieves 59.4 dB SNDR at Nyquist input while consuming 16.1mW, corresponding to a FoM_S of 167.3dB, highlighting its high power efficiency for multi-GS/s ADCs.

References

[1] A. M. A. Ali *et al.*, "16.1 A 12b 18GS/s RF sampling ADC with an integrated wideband track-and-hold amplifier and background calibration," *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2020, pp. 250-252.

[2] Q. Yu *et al.*, "A 12b 3 GS/s passive T/H assisted time-interleaved pipelined SAR ADC with metastability reduction technique and dynamic-bias RA," *2024 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Hiroshima, Japan, 2024, pp. 1-3.

[3] M. Zhan *et al.*, "A 0.004mm2 200MS/s pipelined SAR ADC with kT/C noise cancellation and robust ring-amp," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 164–166.

[4] M. -J. Seo *et al.* "A single-supply CDAC-based buffer-embedding SAR ADC with skip-reset scheme having inherent chopping capability," *Journal of Solid-State Circuits*, vol. 55, no. 10, pp. 2660-2669.

[5] Q. Huang *et al.*, "A 16b 5MS/s 93.7dB-SNDR SAR ADC with a split sampling technique and SRM-assisted self-calibration," *Custom Integrated Circuits Conference (CICC)*, Denver, CO, USA, 2024, pp. 1–2.

[6] Y. Shen *et al.*, "A 12-bit 1.5-GS/s single-channel pipelined SAR ADC with a pipelined residue amplification stage," *Journal of Solid-State Circuits*, vol. 60, no. 1, pp. 260-271.