A 79 dB SNR, 36.6 µV Resolution Adaptive Read-Out Circuit for Non-Linear Stress Sensors in Biomedical Applications

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***Abstract*—This work presents a novel readout system for biomedical sensors that directly digitises small amplitudes with high resolution, eliminating the need for a conventional amplifier and thereby saving power and area. The proposed 13-bit Voltage-to-Time-to-Digital Converter (VTDC) can achieve a resolution upto 36.6 µV and SNR upto 79 dB. The complete system consumes ≈270 µW during active conversion and ≈712 nW during idle state with 1.8 V supply. The proposed converter can provide an adjustable resolution, which can be dynamically set according to the expected input signal ranges. This flexibility is particularly useful for applications where the sensor sensitivity varies due to assembly or fabrication processes. The conversion time is programmable from 975 µs for a 13-bit configuration to 225 µs for a 10-bit configuration. which can be further reduced based on the application's resolution requirements.**

***Index Terms*—ADC, VCO-based ADC, Non-linear sensor read-out, High Resolution ADC, Voltage-to-Time-to-Digital Converter.**

I. Introduction

Biomedical signals typically have low amplitudes (µV to mV) and low frequencies (0.05 to 100 Hz). Due to their sensitivity to flicker noise, these signals require advanced bandpass filters or chopping techniques to achieve the desired noise performance and resolution. These circuits often have high power and area requirements, which limit their suitability for IoT or biomedical applications. This paper presents a sensor readout circuit for such low-amplitude biomedical applications that is particularly useful for non-linear signals, such as those from pressure, humidity, capacitance, or temperature sensors. The operating principle is inspired from Voltage Controlled Oscillator (VCO) based ADCs. Many recent publications have made remarkable improvements to the VCO ADC concept and linearity [1], [2], however, a system where the data output is a frequency is not suitable for applications like "tactile skin" [3] where the sensor array data must be transmitted over large distance via a shared I2C bus. The converter works well over a wide range of DC bias voltages and can even be shared with different types of sensors via multiplexing.

II. Proposed Converter Concept

The basic principle behind the proposed converter design is shown in Fig. 1. When a voltage-controlled current charges a capacitor, the output voltage is directly proportional to the charging time. Even small differences in V_{in} can result in significant differences in V_{out} over time. To avoid limiting the "amplification" due to saturation at the supply voltage, the principle can be modified as shown in Fig. 2, where identical capacitor cells are placed in series. When a cell reaches its threshold $(V_{dd}/2)$, it triggers the next cell to start charging. Since all cells charge at the same rate, controlled by a mirrored PMOS current source, only two cells will be actively charging and consuming power at any time. The input signal is then quantified by counting the number of cells fully charged within the allotted period.

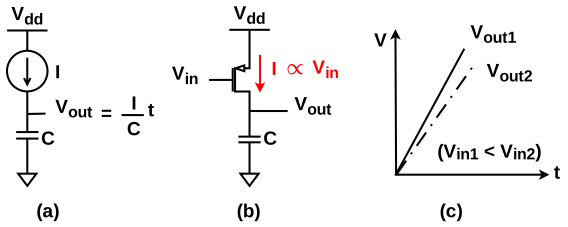

Fig. 1. A capacitor charging cell using: (a) an ideal current source, (b) a voltage-controlled current source. (c) Relationship of V_{out} with respect to V_{in} and integration time)

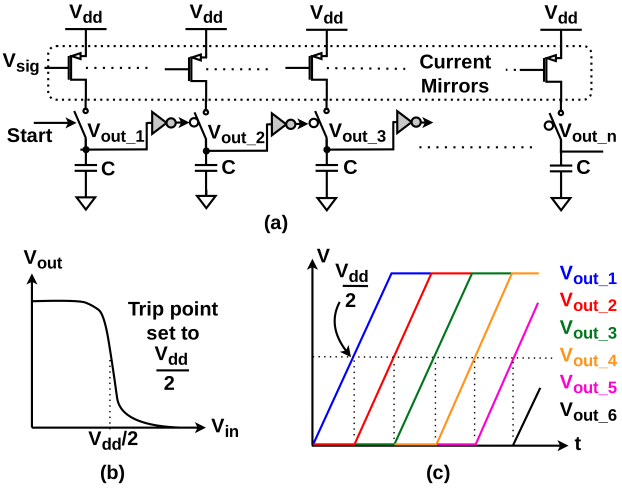

Fig. 2. A sequentially charged chain of capacitor cells. The low-amplitude V_{sig} is superimposed on a DC bias voltage (V_{bias}) to keep the current-mirror MOSFETs in the saturation region at all times.

III. Complete System Implementation

Fig. 3 shows how the concept works with respect to a reference (or differential input) voltage. Two identical capacitor chains operate simultaneously. One is charged by the reference

signal, and the other is charged by the sense signal. The reference chain has 2^N cells, where N is the desired converter resolution. The sense chain has twice as many cells (2^{2N}) as the reference chain. When the reference chain finishes charging, it stops the charging process on the sense side. The difference between V_{ref} and V_{sense} affects charging time, making the sense side charge faster or slower than the reference.

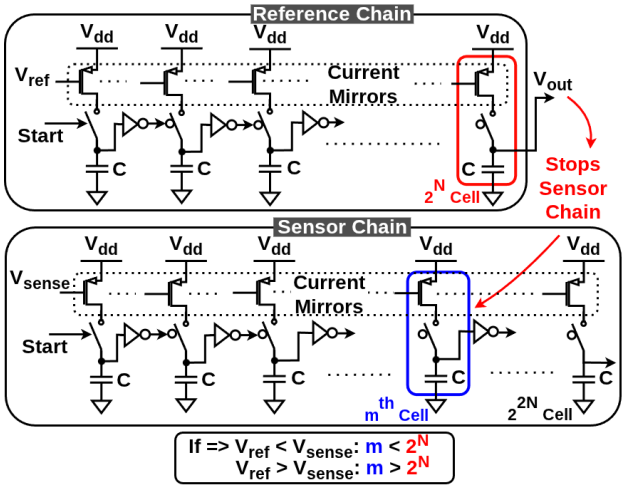

Fig. 3. Simultaneous charging of sensor and reference chains. The difference in input voltages results in a difference in charging time, which is then digitized by a counter.

To resolve very small voltages, many cells are needed. To avoid this, we use a chain of 8 cells connected in a loop. When the 8th cell is charged, it triggers the first cell to begin charging again. To achieve this, the basic charging cell is modified as shown in Fig. 4(a). The charging (Charge) and discharging (Clear) signals for each cell are shown in Fig. 4(b). When the 4th cell is charged, it triggers the 1st cell's capacitor to discharge. The 5th cell discharges the 2nd cell, and so on. This keeps the charging loop running smoothly. The complete recursive chain is shown in Fig. 4(c). A counter counts the number of times the 8th cell charges. It is worth noting that the first cell must be started with an active-low pulse at the beginning of each new conversion operation, after which charging occurs only via M_2 when triggered by the 8th cell. For other cells, the 'Start' signal is always high, so the path through M_3 remains open. At the end of each conversion, the INIT signal discharges all cells and resets the counters to zero.

Fig. 5 shows the reference and sense blocks. When the reference counter reaches the set Counter Stop Value (CSV), it sends a 'Count Finish' signal, which stops the charging process in both chains and disables the counters. The sense counter output gives the number of complete loop charges of the 8-cell chain. To detect the number of cells charged in the current loop, a simple digital logic (Fig. 6) is used. Any charge above the threshold ($V_{dd}/2$) in the last cell gives the residual voltage, V_{res}.

Fig. 7 shows the complete system overview. The total number of cells charged in the reference side (N_{ref}) and sense side (N_{sense}) can be calculated as follows:

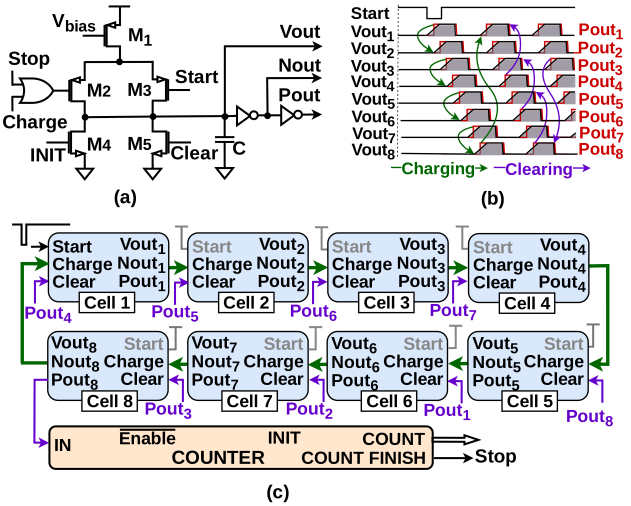

Fig. 4. (a) Modified recursive charging cell. (b) 'Charge' and 'Clear' signal waveforms for 8-cells. (c) Complete recursive loop. The counter increments after the 8th cell is charged.

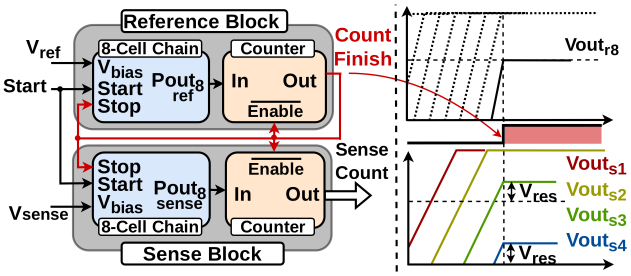

Fig. 5. Reference and sense blocks and the V_{out} waveforms at the end of the counting operation.

Cell	1	2	3	4	5	6	7	8
Vout	V_{dd}	V_{dd}	> $V_{dd}/2$	< $V_{dd}/2$	0	0	0	0
Nout	0	0	0	V_{dd}	V_{dd}	V_{dd}	V_{dd}	V_{dd}
Pout	V_{dd}	V_{dd}	V_{dd}	0	0	0	0	0
Code	0	0	V_{dd}	0	0	0	0	0

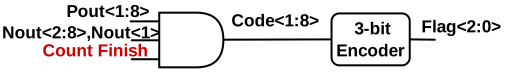

Fig. 6. Digital logic to calculate the number of "fully-charged" cells in the last charging cycle on the sense-side.

$$N_{ref} = \text{Counter Stop Value} \times 8 \quad (1)$$

$$N_{sense} = (\text{Sense Count} \times 8 + \text{Flag}) \quad (2)$$

The difference between N_{ref} and N_{sense} ($D_{out} = N_{ref} - N_{sense}$) yields the digitised output of the sensor signal relative to the reference signal. If a higher resolution is needed, V_{res} can further be digitised using a low-resolution ADC.

IV. Measurement Results and Discussions

Fig. 8(a) presents the converter output as a function of input signal amplitudes ($\Delta V_{in} = V_{ref} - V_{sense}$). The converter demonstrates consistent performance across four measured samples, under different package stresses from sealed and molded packaging [4], without external trimming or calibration. The converter maintains a linear output within an input range of ±50 mV (Fig. 8(b)) but shows nonlinearity at higher

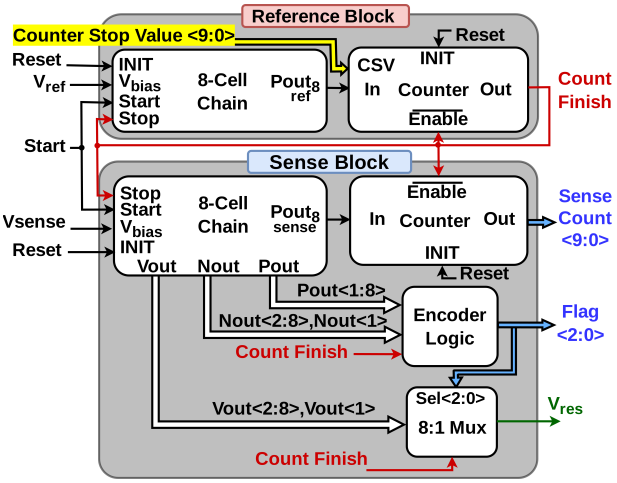

Fig. 7. Top-level block diagram of the Voltage-to-Time-to-Digital Converter. Conversion time and resolution are set by the Counter Stop Value. The resolution can further be increased by digitising V_{res}.

signal amplitudes. The linearity and input dynamic range of the converter are tunable by adjusting the DC bias voltages (V_{bias}) of the reference and sense signals (Fig. 8(c)). System offsets arising from sensor electrodes or assembly can be digitally compensated by subtracting the corresponding 'zero-signal' converter output from all other digitised values. This eliminates the need for large-area filters or trimming logic. The converter's resolution is dynamically adjustable by modifying the stop value of the reference counter (Fig. 8(d)).

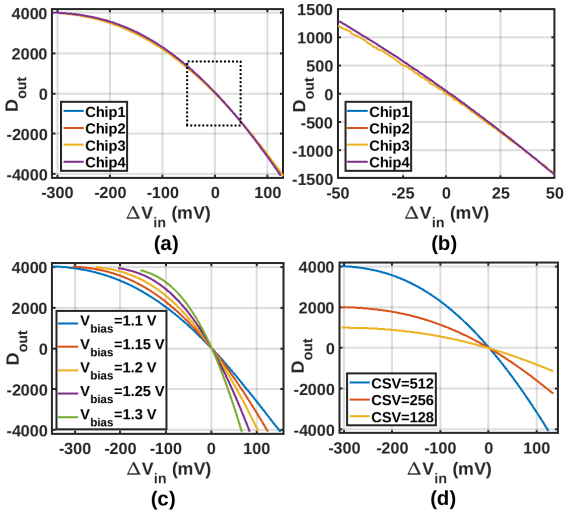

Fig. 8. (a),(b) Converter transfer function for 4 samples under nominal conditions†. (c) Transfer function as a function of V_{bias} and (d) CSV.

Fig. 9 shows the converter output under varying supply voltages and temperatures. Changes in supply voltage have a negligible impact on the converter behaviour as long as the V_{bias} scales accordingly. Temperature variations show a minimal effect on the overall gain of the transfer curve that can be calibrated either via trimming the temperature coefficients of the charging current, or external compensation after measurement. Fig. 10 shows the system's measured power consumption and conversion time. Under nominal conditions†, the converter consumes ≈270 µW of power. The average power consumption depends only on the bias voltage, which sets the charging current through each converter cell, and is independent of the converter resolution. The PMOS-based current mirror reduces the charging current as the bias voltage increases, thereby increasing the time required for the reference chain to reach the stop value, and hence the overall conversion time. Longer integration time due to lower currents also improves the overall noise performance of the converter.

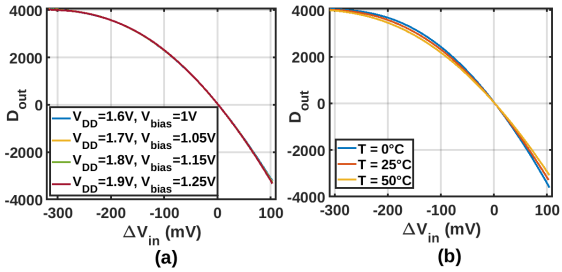

Fig. 9. Converter transfer function for CSV = 512 under varying (a) supply voltages (@ T = 25°C), and (b) temperatures (@ V_{DD} = 1.8 V, V_{bias} = 1.15 V).

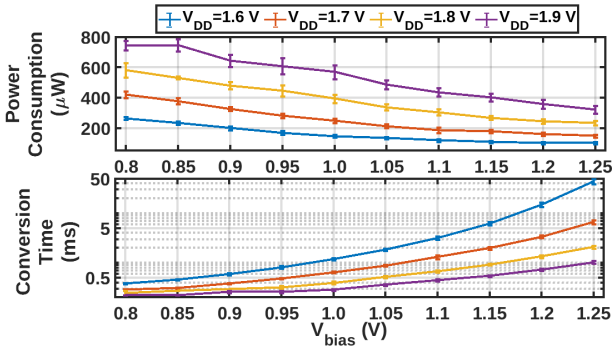

Fig. 10. Power consumption and conversion time for different V_{bias} and V_{DD}.

Noise analysis was performed by doing 1000 repeated DC measurements at each input voltage to calculate the standard deviation (σ_{noise}) of the output code in term of LSB. The SNR/ENOB, and FOM$_s$ (shown in Fig. 11 and Fig. 12 respectively) are then calculated using the following formulae:

$$\mathrm{SNR(dB)}^{\S} = 20 \times \log\left(\frac{\mathrm{Mean}(D_{out})}{\sqrt{2}\ \sigma_{noise}}\right) \quad (3)$$

$$\mathrm{ENOB} = \frac{\mathrm{SNR(dB)} - 1.76}{6.02} \quad (4)$$

$$\mathrm{FOM_s(dB)} = \mathrm{SNR(dB)} + 10 \times \log\left(\frac{1}{\mathrm{Power} \times \mathrm{Conversion\ Time}}\right) \quad (5)$$

V. Conclusion and Future Scope

The paper presented a VCO-inspired converter for low-frequency signals. The proposed circuit is implemented using

†V_{bias} = 1.15 V for both V_{sense} and V_{ref}, CSV = 512, V_{dd} = 1.8 V, Temperature = 25°C.

§Since D_{out} is normalised w.r.t to the input amplitude (and not the peak-peak range) a division factor of 2 is removed while calculating the rms signal.

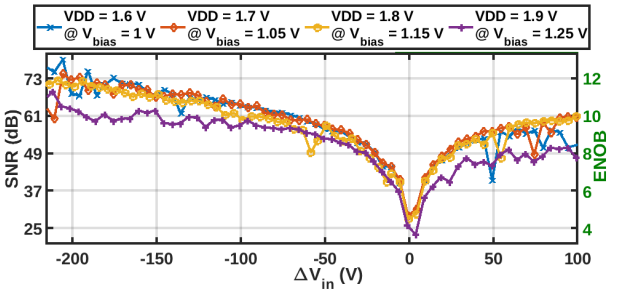

Fig. 11. Measured SNR (in dB - left axis) and ENOB (in bits - right axis) for different input and supply voltages.

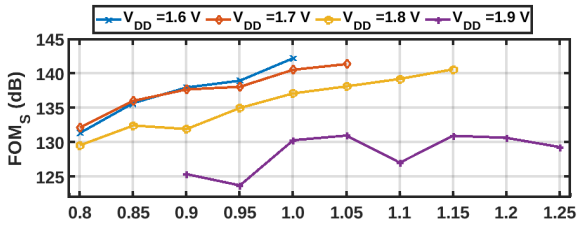

Fig. 12. FOM_s (dB) for $\Delta V_{in} = -200$ mV under different V_{bias} and V_{DD}.

a standard CMOS 0.18 µm process and occupies an area of 0.069 mm^2 (Fig. 13). The gain, input voltage range, and non-linearity can be customised by adjusting the DC bias voltage. This characteristic makes the converter well-suited for silicon-based piezoresistive sensors (Fig. 14), where the stress response is inherently nonlinear between tensile and compressive stress. The converter shows consistent performance across varying temperature and voltage conditions, with a peak SNR of 79.3 dB. The overall power and conversion time (and hence the FOM_s) can be further improved by reducing the cell current and capacitance; however, flicker and switching noise must be considered during the optimisations. It is evident from Fig. 10 and Fig. 12 that the efficiency of the system increases at lower supplies making such a topology suitable for lower technology nodes. Table I provides a summary of the converter's performance and a comparison with other state-of-the-art read-out systems for stress sensing applications.

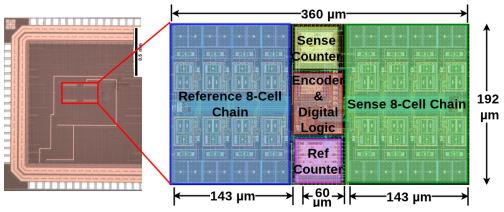

Fig. 13. The die photograph and layout dimensions of the complete converter.

VI. Acknowledgement

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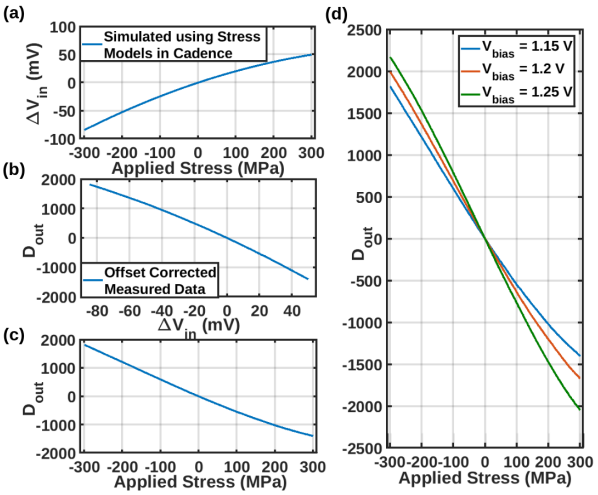

Fig. 14. (a) Simulated response of a non-linear stress sensor, (b) Measured converter response using the simulation results as input voltages, (c) Mapping the converter output to the stress input, (d) Linearity of the converter at different V_{bias}.

TABLE I
Performance Comparison with Prior Art.

	This Work		[5] JSSC'20	[6] ISSCC'23		[7]Sensors Journal'26
Process (nm)	180		130	180		180
Supply (V)	1.6-1.9		1.8-3.3	1.8		1.2
Readout Principle	VCO (Count-Based)		ΔΣ	SAR		IΔΣ
Area (mm^2)	0.069		0.46	0.89		0.594
Resolution (kPa/LSB)	13-bit 92[a]		11-bit 175	12-bit 11[b]	178	11-bit ±322/157[c]
Dynamic Range (MPa)	-380 to 300[a]		-100 to 360	±22.53[b]	±364.55	±330/161[c]
Power (µW)	148[d]	270[e]	357[j]	1280[f]		2410[g]
SNR (dB)	79.3[d]	72.88[e]	-	76[b]		-
Conversion Rate (kHz)	0.824[d]	1.066[e]	15.3[h]	0.7 to 22.5[i]		40[h]
FOM_s	142.3[d]	140.6[e]	-	-		-

[a]From experiments using simulation data. Can be further reduced by adjusting V_{bias} for lower dynamic range; [b]Corresponding to lower dynamic range; [c]Shear/Normal stress; [d]Converter only @V_{DD}=1.6 V; [e]Converter only @V_{DD}=1.8 V; [f]For entire chip @10 MHz SPI; [g]For entire chip including 48 sensor sites; [h]Sampling frequency; [i]Adjustable, max. 22.5 kS/s for single sensor; [j]Analog only.

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