A Calibration-Free Impedance-Invariant Phase and Amplitude Control Unit Achieving $< 2°$ RMS Phase Error for C-Band Phased Arrays

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***Abstract*—This paper presents a calibration-free C-band phase and amplitude control unit (PACU) that eliminates code-dependent impedance variation using a replica-path-assisted impedance-invariant vector-modulator phase shifter (I^2VMPS). Coordinated main/replica switching maintains a constant output impedance and enables phase-code generation through direct mathematical derivation. In addition, a current-mode attenuator (CM-ATT) enables current-domain gain control (GC), facilitating scalable parallel integration across array elements. With an compact continuous-time linear equalizer (CTLE), the proposed PACU realizes a 66.7% fractional bandwidth (FBW) without a large-area matching network. Fabricated in 65-nm CMOS, it occupies a core area of 0.128 mm² and achieves 7-bit phase shift and 5-bit gain control with rms errors below 2.04° and 0.15 dB, respectively, outperforming state-of-the-art PACUs.**

***Index Terms*—Calibration-free, C-band, impedance-invariant vector-modulator phase shifter (I^2VMPS), current-mode attenuator (CM-ATT), continuous-time linear equalizer (CTLE)**

I. Introduction

C-band phased arrays, extensively employed in weather radar, satellite links, and unmanned aerial vehicles (UAVs), require precise phase shifting (PS) and gain control (GC), placing stringent demands on the per-element phase and amplitude control unit (PACU). Compared with passive phase shifters, vector-modulator phase shifters (VMPSs) are preferred for their high resolution, accurate phase control, and compact area. However, in a conventional high-resolution VMPS, switching the high-bit variable-gain amplifier (VGA) cells introduces large variations in the output parasitic capacitance, severely degrading linearity.

Existing VMPS techniques mainly follow two routes: improving the intrinsic phase-shifting linearity and employing phase calibration. Higher intrinsic linearity reduces the calibration burden. VMPSs based on bias-controlled VGAs are usually calibrated through the bias DAC [1]–[3]. A cascaded common-emitter/common-base (CE/CB) bias-controlled VGA can partially enhance intrinsic linearity by exploiting complementary phase–frequency characteristics, as shown in Fig. 1(a), yet this remains insufficient for calibration-free operation [4].

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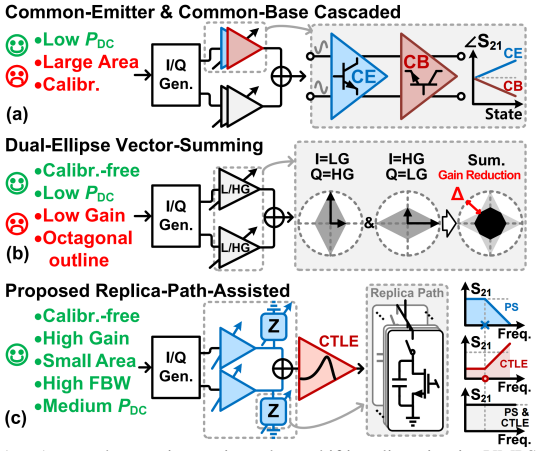


Fig. 1. Approaches to improving phase-shifting linearity in VMPSs: (a) CE-CB cascaded structure for phase compensation [4]; (b) VMPS with an octagonal amplitude contour enabled by a mode-switchable VGA [9]; and (c) proposed replica-path-based impedance-invariant VMPS architecture.

In contrast, VMPSs using switched-cell VGAs exploit redundant phase states through elaborate calibration, which is widely adopted but complex [5]–[7]. To mitigate capacitance discontinuities, switched-cell VGA commonly keeps the VGA bits always ON, but incurs state redundancy and increases area and power consumption [5]–[7]. Digitally assisted VMPSs further improve linearity by combining VGA-based amplitude control with current-DAC tuning, but they still rely on precise calibration of the DAC [8]. In [9], a dual-ellipse vector-summing technique realizes an octagonal phase trajectory, enabling calibration-free operation by avoiding circular constellations. Nevertheless, it suffers from gain reduction and inherent gain mismatch, as shown in Fig. 1(b). In addition, for GC, variable gain phase shifters (VGPS) aggravate PS-induced gain variation [4], while power-mode attenuators or VGAs require bulky output matching and combining [9].

In response, this paper presents a calibration-free PACU based on a replica-path-assisted impedance-invariant vector-modulator phase shifter (I^2VMPS). Coordinated switching of the main and replica-paths maintains a nearly constant output impedance across all phase states, while analytically

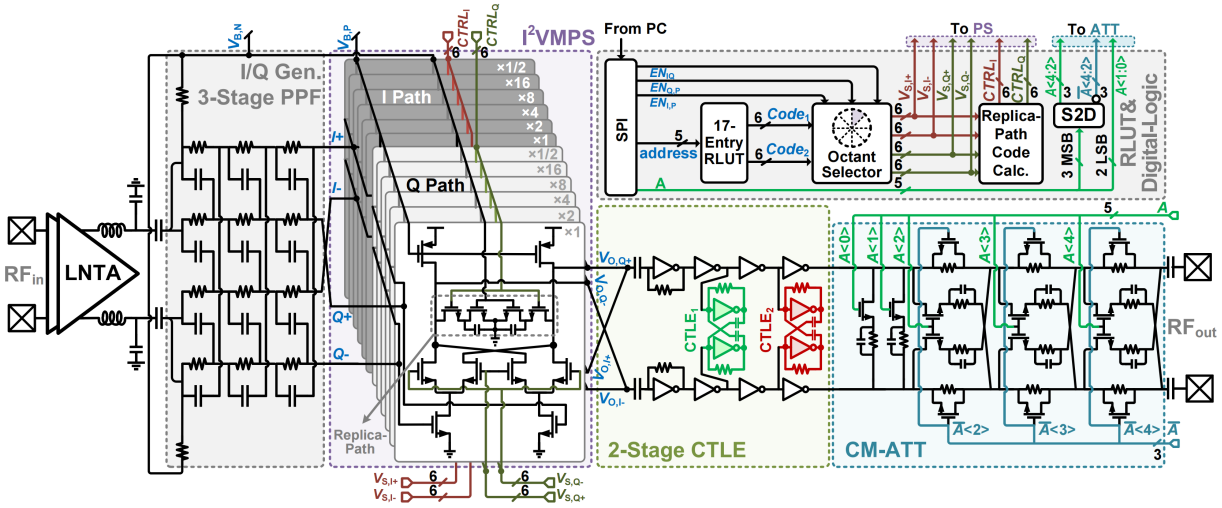


Fig. 2. Overall architecture of the proposed PACU.

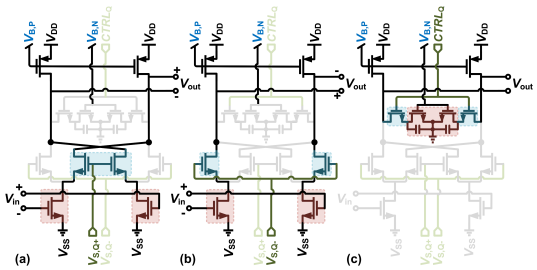


Fig. 3. Three operating modes of a single VGA slice in the proposed I²VMPS: (a) main path on for in-phase output; (b) main path on for anti-phase output; (c) replica path on for output-impedance compensation.

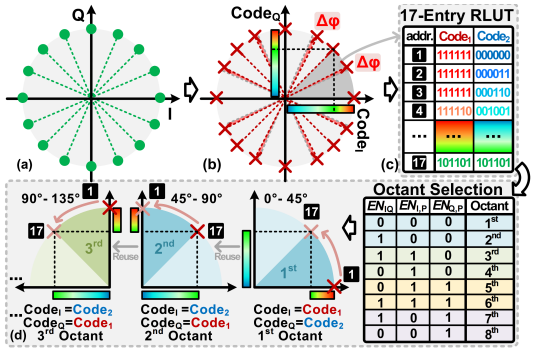


Fig. 4. Code-determination method of the proposed I²VMPS: (a) ideal phase calculation; (b) theoretical phase-code calculation; (c) RLUT data storage scheme; and (d) data reuse through an octant selector.

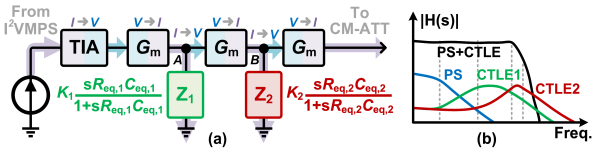


Fig. 5. (a) Equivalent signal-flow model of the CTLE; (b) frequency responses of the CTLE and I²VMPS.

derived codes stored in a reusable lookup table (RLUT) enable calibration-free 7-bit phase control over 0–360°. A compact two-stage CTLE replaces the interstage LC matching network to reduce area, compensate for the I²VMPS-induced pole shift, and preserve wideband S_{21}. In addition, a 5-bit current-mode attenuator (CM-ATT) provides GC.

II. Proposed Impedance-Invariant PACU

The overall architecture of the proposed PACU is shown in Fig. 2. It consists of a 2-stage low noise transconductance amplifier (LNTA), a 3-stage poly-phase filter (PPF), an I²VMPS, a two-stage CTLE, a CM-ATT, the RLUT and digital control logic. The input RF signal is first amplified and converted into quadrature components, and is then processed in the current domain for PS, bandwidth equalization, and GC.

A. Replica-Path-Assisted Impedance-Invariant VMPS

Fig. 2 also details the replica-path-assisted I²VMPS. Each VGA slice is implemented as a Gilbert cell, in which the input nMOS pair is biased in saturation by $V_{B,N}$ fed through the PPF, while V_{DD} is supplied through the upper pMOS devices, thereby avoiding large DC-feed inductors. In the replica path, the nMOS devices use the same sizing and biasing as those in the main-path to emulate its impedance, while shunt capacitors are added to further improve linearity. Fig. 3 shows the three operating modes of each VGA slice: in-phase output, anti-phase output, and main-path turn-off with the replica path enabled for impedance compensation. To limit the power overhead introduced by replica-path activation, the I²VMPS adopts a low-voltage design with V_{DD} = 0.6 V and independently optimized pMOS ($V_{B,P}$) and nMOS ($V_{B,N}$) bias voltages. In addition, a ½-bit unit is added to both I- and Q-path VGAs for fine gain tuning. This is realized by doubling the channel length L of the input nMOS pair while keeping the width W unchanged, thus avoiding the need for an additional highest-weight VGA cell with 64 slices. These approaches enable high-resolution VGA operation without significantly increasing layout area, while the replica path

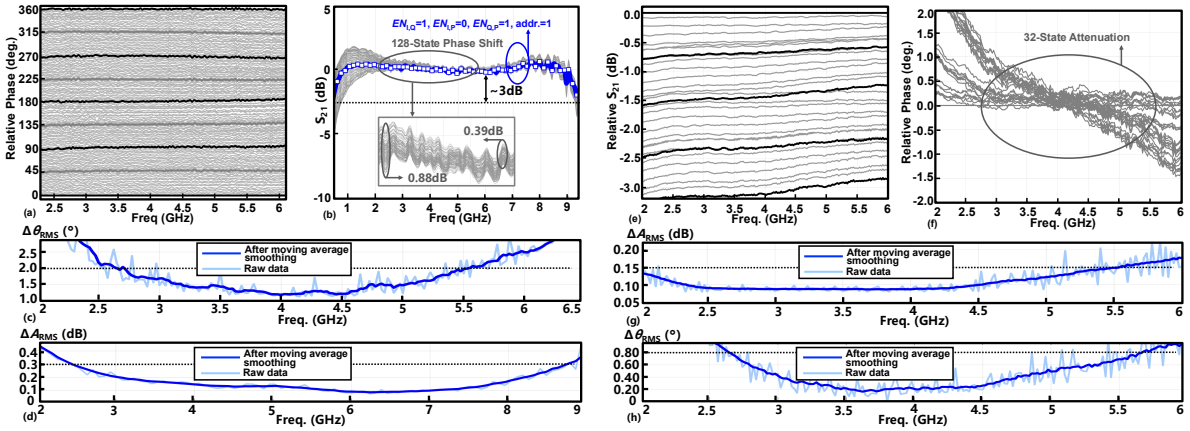


Fig. 6. Measured PS and GC performance of the proposed PACU: (a) relative phase and (b) S_{21} of the 128 phase-shift states; (c) $\Delta\theta_{\mathrm{RMS}}$ and (d) ΔA_{RMS} of the I^{2}VMPS without calibration; (e) relative S_{21} and (f) relative phase of the 32 gain-control states; and (g) ΔA_{RMS} and (h) $\Delta\theta_{\mathrm{RMS}}$ of the CM-ATT.

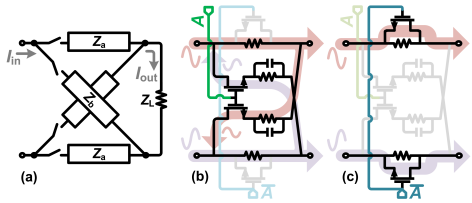


Fig. 7. Equivalent models of the CM-ATT: (a) two-port lattice model; (b) attenuation state; and (c) reference state.

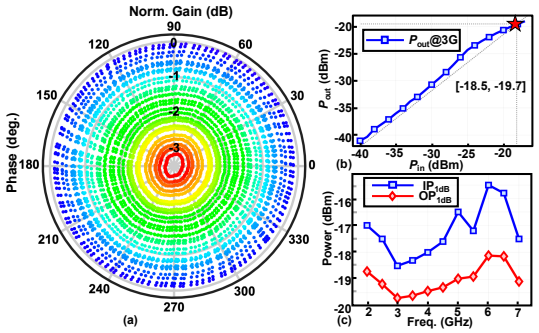


Fig. 8. (a) Measured vector constellation at 4.5 GHz without calibration; (b) output power versus input power at 3 GHz; and (c) measured $\mathrm{IP_{1dB}}$ and $\mathrm{OP_{1dB}}$ in the maximum gain state.

preserves linearity. Since the corresponding phase codes are inherently frequency-independent, the two 6-bit VGAs in each path achieve calibration-free 7-bit PS over the full bandwidth with high accuracy, compact area, and low DC power.

B. Reusable LUT and Digital Logic

Fig. 4 illustrates the analytical code-selection procedure of the I^{2}VMPS. Instead of relying on iterative measurements, the VGA codes are directly calculated from the target phase resolution. For the k-th nominal phase state, the corresponding 6-bit I- and Q-path control codes are obtained by

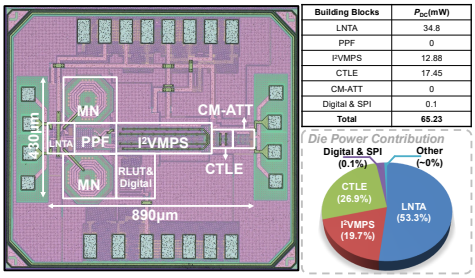
$$(\mathrm{Code}_{\mathrm{I},k}, \mathrm{Code}_{\mathrm{Q},k}) = \mathrm{round}\left[63 \cdot (|\cos\phi_k|, |\sin\phi_k|)\right] \quad (1)$$

where $\mathrm{round}[\cdot]$ denotes element-wise nearest-integer quantization, and $\phi_k = 2k\pi/128$ for $k = 0, 1, \ldots, 16$. The signs of the I/Q codes are controlled separately by the VMPS-cell polarity. As illustrated in Fig. 4(a) and (b), the residual mapping error introduced by the 6-bit quantization is negligible. Only 17 independent code pairs within the first octant (0°–45°) need to be stored in the RLUT. The remaining phase states are generated through I/Q code swapping and polarity inversion, enabling calibration-free 7-bit phase coverage over the full 360° range, as shown in Fig. 4(c) and (d).

Fig. 2 shows the digital control architecture. A 5-bit address is fed into the 17-entry RLUT to generate two pre-stored 6-bit codes ($\mathrm{Code_1}$ and $\mathrm{Code_2}$). The octant-selection signals, $\mathrm{EN_{IQ}}$, $\mathrm{EN_{Q,P}}$, and $\mathrm{EN_{I,P}}$, are then used to produce four 6-bit control words, $V_{\mathrm{S,I+}}$, $V_{\mathrm{S,I-}}$, $V_{\mathrm{S,Q+}}$, $V_{\mathrm{S,Q-}}$, for the main path of the I^{2}VMPS. These signals are further processed by the replica-path code calculator to generate the corresponding replica-path control words, $\mathrm{CTRL_I}$, $\mathrm{CTRL_Q}$, thereby ensuring impedance consistency across all phase states. Meanwhile, the CM-ATT control code is converted through a single-ended-to-differential (S2D) interface to configure the attenuation states.

C. CTLE-Based Inductorless Broadband Design

To realize a compact inductor-less interface with wide-band interstage transfer, a two-stage CTLE equalizer is inserted between the I^{2}VMPS and the CM-ATT attenuator. A front-end transimpedance amplifier (TIA) first terminates the current-mode output of the I^{2}VMPS with a low input impedance, thereby suppressing residual code-dependent output-impedance variation while converting the signal into the voltage domain. As shown in Fig. 5(a), the CTLE can be modeled by an equivalent signal-flow representation consisting of a TIA followed by three G_{m} stages, where Z_1 and Z_2 denote the effective impedances at the two inter-stage nodes, A and B. The two equalization paths are approximated as $K_1 \cdot sR_{\mathrm{eq},1}C_{\mathrm{eq},1}/(1+sR_{\mathrm{eq},1}C_{\mathrm{eq},1})$ and $K_2 \cdot sR_{\mathrm{eq},2}C_{\mathrm{eq},2}/(1+sR_{\mathrm{eq},2}C_{\mathrm{eq},2})$, where K_1 and K_2 are the equalization gains, and $R_{\mathrm{eq},1}$, $R_{\mathrm{eq},2}$, $C_{\mathrm{eq},1}$, and $C_{\mathrm{eq},2}$ set the corresponding frequency-shaping characteristics. Consequently, $\mathrm{CTLE_1}$ compensates



Building Blocks	P_{DC}(mW)
LNTA	34.8
PPF	0
I²VMPS	12.88
CTLE	17.45
CM-ATT	0
Digital & SPI	0.1
Total	65.23

Fig. 9. Die micrograph and power breakdown.

the dominant roll-off of the I^{2}VMPS, while CTLE_2 further boosts the upper-band response. As shown in Fig. 5(b), the proposed two-stage CTLE effectively extends the bandwidth of the I^{2}VMPS without bulky inductive matching, thereby preserving wideband S_{21} while maintaining PACU compactness.

D. CM-ATT

The proposed CM-ATT employs cascaded attenuation cells to achieve high-resolution GC for differential current-mode signals (see Fig. 2). As shown in Fig. 7(a), the 3 MSBs are implemented as a two-port lattice terminated by the effective load impedance Z_L of the subsequent stage, where the through and cross arms are represented by Z_a and Z_b, respectively. The 2 LSBs use a simple parallel-branch structure for fine gain tuning. In the attenuation state (Fig. 7(b)), the cross-arm path is enabled to redistribute the current and partially cancel the recombined output current, thereby reducing the output amplitude. In the reference state (Fig. 7(c)), the signal mainly propagates through the direct path with minimal loss. By properly selecting Z_a and Z_b, precise attenuation steps can be achieved with limited phase disturbance. Owing to the symmetry of the lattice structure, the input impedance remains approximately constant in both states, eliminating the need for additional matching and making the CM-ATT naturally compatible with the preceding CTLE.

III. Measurements

Fabricated in 65-nm CMOS, the proposed PACU occupies a core area of 0.128 mm^2 and consumes 65.23 mW, or 30.43 mW excluding the LNTA, as shown in Fig. 9. It operates from 2.8 to 5.6 GHz with 66.7% fractional bandwidth (FBW). The I^{2}VMPS provides 7-bit phase resolution with a 2.8125° step size, enabling full 360° coverage (Fig. 6(a)), with measured RMS phase and gain errors ($\Delta\theta_{\mathrm{RMS}}$ and ΔA_{RMS}) of 1.18°–2.04° and 0.10–0.22 dB under phase tuning (see Fig. 6(c) and (d)). The 5-bit CM-ATT achieves a 0.1–dB step size, inducing $<\pm1.2°$ phase shift during gain tuning (Fig. 6(e) and (f)), with 0.16°–0.76° $\Delta\theta_{\mathrm{RMS}}$ and 0.08–0.15 dB ΔA_{RMS} (see Fig. 6(g) and (h)), confirming good phase/gain isolation. Fig. 6(b) shows that the peak gain of the PACU reaches 0.3 dB. The measured vector constellation forms a circular trajectory, validating the proposed impedance-invariant architecture, as shown in Fig. 8(a). Fig. 8(b) plots output versus input power at 3 GHz, with IP1dB of -18.5 to -16.5 dBm (Fig. 8(c)),

TABLE I
Comparison With State-of-the-Art PACUs

		This Work	Z.Zhang ESSERC'25 [9]	Q. Zhang JSSC'25 [4]	Y.Xiong TCAS-I'23 [2]	B.Dou TCAS-II'22 [6]	K. Koh JSSC'07 [3]	T. Li TVLSI'20 [5]	H.Wang CICC'07 [7]
Technology (nm)		65 CMOS	28 CMOS	130 SiGe	250 GaAs	180 CMOS	130 CMOS	65 CMOS	130 CMOS
Topology		LNTA + I^{2}VMPS + CM-ATT	VMPS+ VGA	VGPS	VGPS	VMPS	VMPS	VMPS	VMPS
Freq. (GHz)		2.8~5.6	25~31	32~38	2~20	4~10	6~18	2~24	0~7.6
FBW (%)		66.7	21.4	16.7	163.6	85.7	100	169.2	200
Calibration		No	No	Yes	Yes	Yes	Yes	Yes	Yes
Phase Tuning	Reso. (°)	2.8125	5.625	2.8125	5.625	5.625	22.5	15	11.25
	Reso. (bit)	7	6	7	6	6	4	/	5
	$\Delta\theta_{\mathrm{RMS}}$ (°)	1.18~ 2.04	0.29~ 1.30	0.33~ 1.61	<2.92	1.0~ 2.25	3~ 10	1.42	<±2 (peak)
	ΔA_{RMS} (dB)	0.10~ 0.22	0.19~ 0.30	0.10~ 0.72	<0.45	0.20~ 0.56	0.5~ 1.7	<±0.75 (peak)	/
Gain Tuning	Reso. (dB)	0.1	0.875	0.468	0.468	/	/	/	/
	Reso. (bit)	5	3	4	4				
	Range (dB)	3.2	7	7.5	7.5				
	$\Delta\theta_{\mathrm{RMS}}$ (°)	0.16~ 0.76	0.38~ 1.55	0.23~ 0.62	<2				
	ΔA_{RMS} (dB)	0.08~ 0.15	0.07~ 0.44	0.08~ 0.26	<0.34				
Peak Gain (dB)		0.3	-8.4	-1.6	-3.1	-5[&]	-0.2	-2	7.8
IP_{1dB} (dBm)		-18.5~ -16.5	/	-6.4~ -5.5	>2.5	7.5~ 15.2	/	/	/
P_{DC} (mW)		65.23 30.43*	0.98	<12.2	575	28	8.7	9.2	/
Active Area (mm^2)		0.128	0.188	0.51	4.5	0.42	0.45	0.38	0.215

*w/o LNTA; [&]Estimated from simulation results

indicating moderate linearity suitable for phased-array receiver front ends. A comparison with recent state-of-the-art designs is summarized in Table I. Overall, the work achieves high phase and amplitude accuracy, wide FBW, and compact area without calibration.

IV. Conclusions

A C-band phase and amplitude control unit based on an impedance-invariant vector-modulator phase shifter is presented. The proposed design enables calibration-free, high-resolution, and accurate phase/amplitude control. It further achieves a favorable tradeoff among peak gain, fractional bandwidth, and core area, making it well suited for phased-array applications.

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