Design of Wideband Doherty Power Amplifier with 35% Fractional Bandwidth, 22dBm Psat and 25% 6dB-PBO PAE in 40nm Bulk CMOS

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***Abstract*—This paper presents a millimeter-wave Doherty power amplifier (DPA) that integrates a reconfigurable output matching network (OMN) and a fast-response adaptive dynamic bias (FR-ADB) scheme to improve back-off efficiency over a wide bandwidth. The OMN employs only two tunable capacitors to alleviate the bandwidth-efficiency-load-modulation trade-off. The FR-ADB suppresses AM–AM distortion and improves back-off efficiency with active-inductor peaking further ensuring fast response of dynamic bias under wideband modulation. Two DPAs, covering 17-25 GHz and 25-32 GHz respectively, are integrated into a wideband transceiver front-end. It achieves 22.7 dBm saturated output power and 22.4 dBm OP1dB, with 32.8%/41.0% peak PAE/DE and 28.1%/35.0% PAE/DE at 6-dB back-off. Under 5G NR FR2 256-QAM modulation with 400 MHz bandwidth, the front-end delivers 11 dBm average output power while reaching -27.7 dB EVM and -32.0 dBc ACLR.**

***Keywords*—Doherty PA, reconfigurable output matching network, fast-response adaptive dynamic bias, back-off efficiency.**

I. Introduction

The demand for high-speed, low-latency wireless communications has propelled the advancement of 5G and low-earth-orbit satellite systems into millimeter-wave bands, as shown in Fig.1. To simultaneously address these application requirements, the transceiver front-ends must operate across wide frequency ranges. Meanwhile, higher data rates are achieved using complex modulation schemes, imposing significant challenges on the power-back-off (PBO) efficiency of power amplifiers in the front-end, as they must handle signals with wide bandwidths (e.g., 400 MHz) and high peak-to-average power ratios (e.g., >10 dB).

The Doherty architecture employs an auxiliary PA to achieve active load modulation, effectively enhancing PBO efficiency [1], [2]. However, it heavily relies on quarter-wavelength transmission lines as impedance inverters, which inherently limits its bandwidth. Recent works [3]–[5] have used lumped elements to reduce the footprint, but their efficiency is often limited by the low efficiency of the passive OMN. Multi-way Doherty architectures extend efficiency enhancement into deeper back-off regions [6], [7], yet the complex amplitude and phase dependencies among multiple amplifier paths compromise their performance. With the load-modulated balanced PA (LMBA) offers a potential wideband solution [8], [9], its dependency on continuously tunable couplers often limits its application.

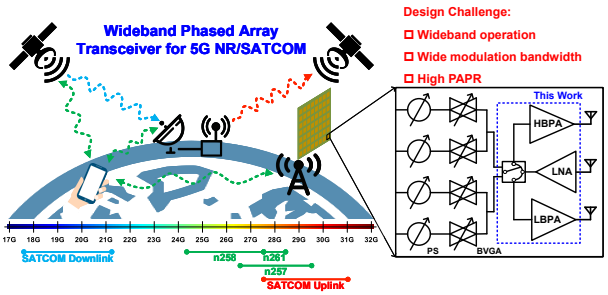

Fig. 1. Application of phased array systems and implementation of a phased array transceiver front-end.

To address these limitations, a Doherty power amplifier utilizing reconfigurable OMN and fast-response ADB technique is proposed. By employing a tunable capacitor, this architecture enables active load modulation over a wide frequency range while the dynamic biasing scheme enhances linearity and PBO efficiency. The fast response of the biasing circuit allows the amplifier to maintain excellent performance under wideband modulated signals.

II. Architecture and Circuit Implementation

Fig.2 illustrates the schematic of the proposed DPA. The reconfigurable OMN realizes the desired load modulation across the operating frequencies, while the FR-ADB circuit provides real-time bias adaptation.

A. Reconfigurable OMN for Wideband Impedance Modulation

The work in [2] and [10] proposed a Doherty architecture that achieves excellent area performance by using single transformer in the output matching network. By introducing two tunable capacitors, as shown in Fig.3(a), we decouple load modulation (TL1) from impedance transformation (TF1) and

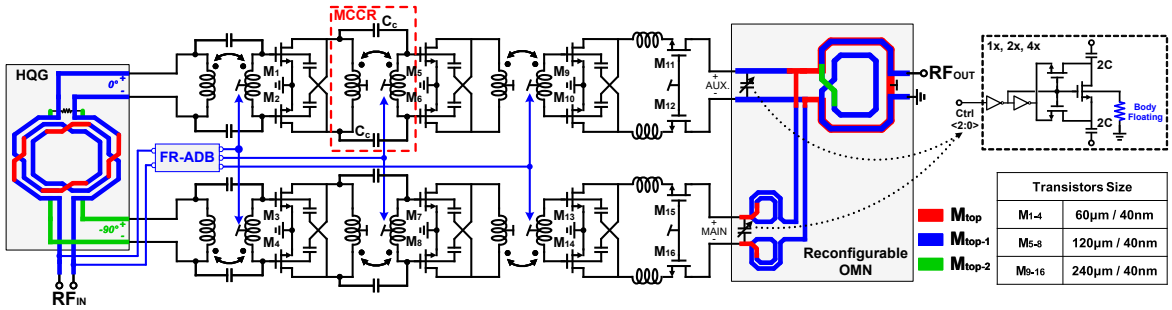

Fig. 2. Simplified schematic of the proposed Doherty PA.

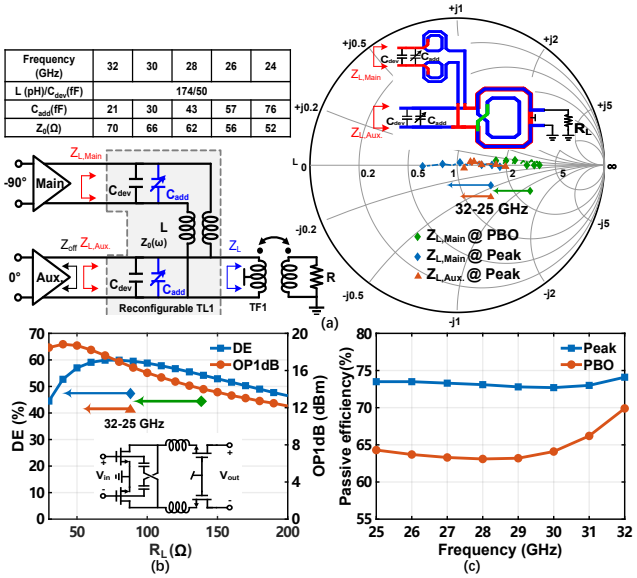

Fig. 3. (a) DPA with reconfigurable OMN and implementation results; (b) Efficiency and linearity of cascode PA unit with various load; (c) Efficiency of the proposed reconfigurable OMN.

reconfigure the quarter-wavelength transmission line across frequencies. Off-chip SPI-programmed static control enables OMN reconfiguration with negligible on-chip overhead. Simulation results in Fig.3(a-b) suggest an approximately resistive load over the band while meeting (1), and the PA core retains high efficiency under these loads with proper sizing. Fig.3(c) plots the passive efficiency of the reconfigurable OMN, exceeding 63% at PBO and 73% at Peak. The high-frequency end is limited by TF1 insertion loss, while the low-frequency end is constrained by tunable-capacitor loss. These co-designed features ensure high overall efficiency of the PA.

$$Z_{L,Main}@\text{Peak} \approx Z_{L,Aux.}@\text{Peak} \approx \frac{1}{2} Z_{L,Main}@\text{PBO} \quad (1)$$

B. Fast-Response Adaptive Dynamic Bias

The PA exhibits severe gain compression under high load impedance when the auxiliary PA is off, leading to linearity degradation. To improve linearity, co-design of the ADB circuit [11] and auxiliary-PA switching is adopted in this work. The proposed ADB circuit employs a self-mixer for envelope tracking, a variable-gain amplifier (VGA) for gain-expansion control, and a low-dead-zone, low-delay comparator

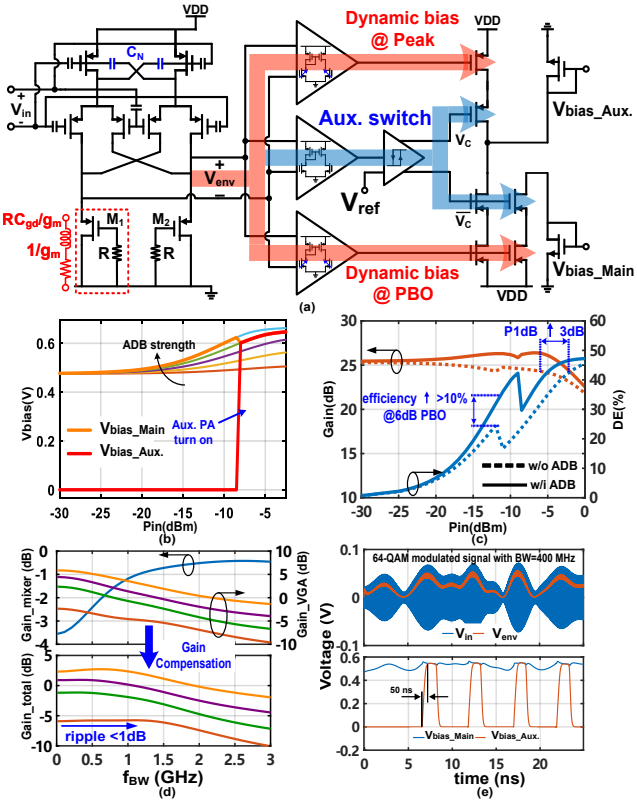

Fig. 4. (a)Schematic of the proposed FR-ADB circuit; (b)Bias of the main and auxiliary PAs versus input power; (c)Gain and drain efficiency of the Doherty PA; (d)Frequency response of the self-mixer and VGA with modulated signal bandwidth, simulated via 2-tone signals spaced by f_{BW}; (e) Transient waveform of the proposed FR-ADB circuit driven by a modulated signal.

for auxiliary-PA switching, as shown in Fig.4(a). The comparator enables rapid and accurate switching of the auxiliary PA with minimal timing error around the desired threshold. Continuous-wave simulation results in Fig.4(b-c) demonstrate that the proposed ADB circuit achieves a 10% improvement in PBO efficiency and more than 3 dB enhancement in linearity, while maintaining the gain ripple within ± 1 dB. Active-inductor peaking is introduced in the self-mixer to compensate for the high-frequency gain roll-off of the subsequent VGA stage, shown in Fig.4(d), while the high-speed comparator enables rapid PA-bias switching with a simulated delay below 50 ns, thereby realizing a fast-response ADB for Doherty PAs under wideband modulated signals. Transient simulation of the

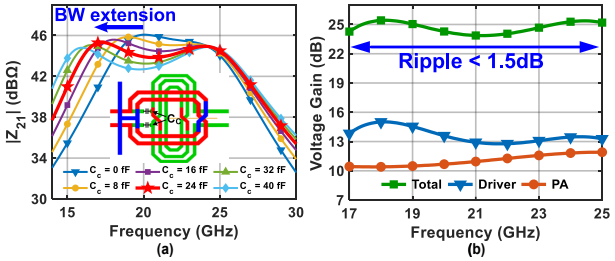

Fig. 5. MCCR for bandwidth extension in LBPA: (a) Frequency response of MCCR; (b) Sub-1.5dB in-band ripple via gain compensation.

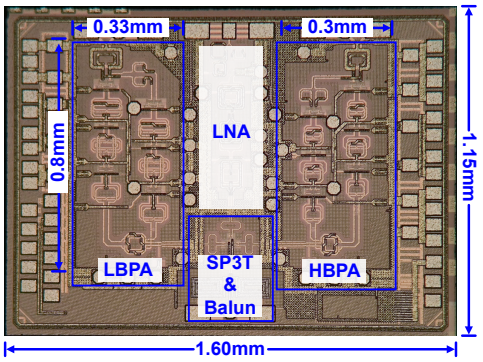

Fig. 6. Chip micrograph of the proposed front-end.

FR-ADB circuit using a 400-MHz-bandwidth 64-QAM modulated signal further demonstrates its capability to dynamically adjust the PA bias and switch the auxiliary PA on and off, as shown in Fig.4(e).

C. Chip Implementation

A low-band PA (LBPA), a high-band PA (HBPA), and a LNA are integrated into a single chip to cover 17-32 GHz, and a single-pole triple-throw (SP3T) switch enables T/R and band switching, as shown in Fig.6. The proposed Doherty PA inherently exhibits a high-frequency gain peak, while a low-frequency peak is purposely introduced in the driver for gain compensation. In the LBPA, a magnetically-capacitively-coupled resonator (MCCR) shifts the low-frequency gain boundary from 20 GHz to 17 GHz, resulting in <1.5dB gain ripple and >35% fractional bandwidth, as shown in Fig.5.

III. Measurement Results

The proposed transceiver front-end is prototyped in 40nm bulk CMOS, and each PA occupies a core area of approximately 1×0.3 mm^2. The chip micrograph is shown in Fig.6. Fig.7 shows the measured S-parameters of the front-end. LBPA exhibits a gain of 22.4-24.4 dB in 17-25 GHz, while HBPA exhibits a gain of 20-22.8 dB in 25-32 GHz.

Fig.8 presents the continuous-wave measurement results of the transceiver front-end. At 21 GHz, the LBPA achieves a saturated output power of 22.7 dBm, an OP1dB of 22.4 dBm, a peak drain efficiency of 41.0%, and a PAE of 32.8%. At 6dB power back-off, the auxiliary PA is automatically switched off, yielding a drain efficiency of 35.0% and a PAE of 28.1%. Under the same operating scheme, the 6dB back-off drain

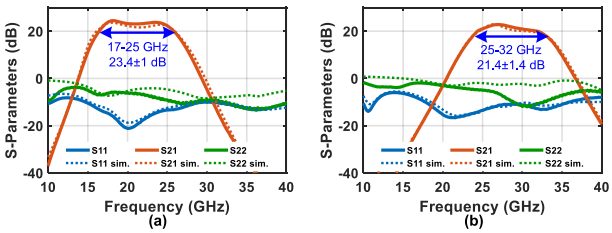

Fig. 7. S-parameter measurement results of : (a) LBPA; (b)HBPA.

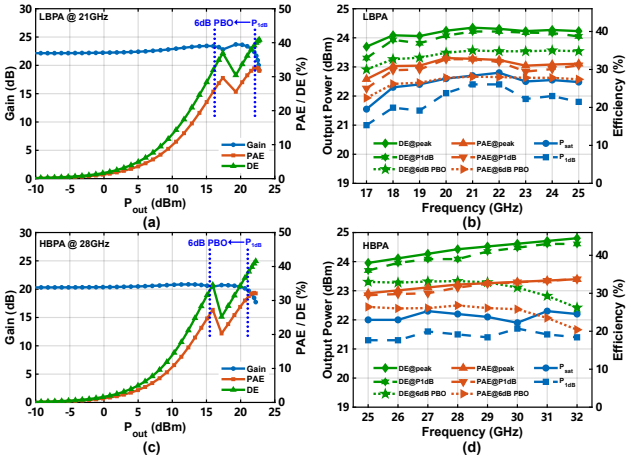

Fig. 8. Continuous wave measurement results of: (a) LBPA at 21 GHz; (b) LBPA in 17-25 GHz; (c) HBPA at 28GHz; (d) HBPA in 25-32 GHz.

efficiency and PAE remain above 30% and 22%, across 17-25 GHz. At 28 GHz, the HBPA achieves a saturated output power of 22.2 dBm, a 1dB compression point of 21.5 dBm, and peak drain efficiency and PAE of 41.6% and 32.3%, respectively. At 6dB power back-off, the drain efficiency and PAE are 33.2% and 26.8%. Across 25-32 GHz, the 6dB back-off efficiency remains above 26% (DE) and 20% (PAE), confirming the effectiveness of the proposed Doherty topology in improving back-off efficiency.

Fig.9 presents the measurement results of the 5G NR FR2 256-QAM modulated signal. With 100/400 MHz 5G NR FR2 modulated input, the front-end achieves an EVM lower than –27.7 dB and an ACLR below –32.0 dB, while delivering an average output power of 11 dBm. The state-of-art EVM benefits from the proposed FR-ADB scheme.

IV. Conclusion

This paper introduces a millimeter-wave DPA that incorporates a reconfigurable output matching network and a fast-response adaptive dynamic bias technique for enhanced back-off efficiency over a wide bandwidth. The OMN uses a simple pair of tunable capacitors to improve the trade-off among bandwidth, efficiency, and load modulation. FR-ADB with active-inductor peaking allows the PA to accommodate wideband signals and improve PBO efficiency. The two mm-wave PAs fabricated in a 40nm CMOS process cover 35% fractional bandwidth, further improve efficiency compared to previous works, and achieve state-of-art EVM with 400MHz 5G NR FR2 modulated input.

TABLE I
COMPARISON WITH RECENTLY REPORTED SILICON-BASED KA-BAND DPAS.

Parameters	This work		RFIC-2025	ISSCC-2022	JSSC-2024	ISSCC-2026	ESSCIRC-2022
	LBPA	HBPA	[10]	[6]	[5]	[12]	[13]
Technology	40nm		28nm FDSOI	55nm	45nm SOI	22nm SOI	130nm SiGe
Frequency (GHz)	17–25	25–32	23-29.2	28	22–40	27	24-30
Topology	Reconfigurable OMN with FR-ADB		Single T.F DPA	3-Way DPA	Parallel–Series DPA	Compact DPA w/i Reciprocal MN	Voltage-Combined DPA
Gain (dB)	24.4	22.8	20.2	16.1	11.8–15.3	16.8	18.5*
Psat / OP1dB (dBm)	22.7/22.4	22.2/21.5	19.8/NA	25.5/24.3	NA/22.5–23.9	20.5/19.9	23.6/23.3
Peak DE / PAE (%)	41.0/32.8	41.6/32.3	35/30*	NA/25.2	NA/26.2–38.2	NA/29.2	24.5/23.85
DE / PAE @6dB-PBO (%)	35.0/28.1	33.2/26.8	25/20*	NA/20.4	NA/18.1–34.5	NA/22.5	NA/19
Modulation Scheme	256-QAM		64-QAM	64-QAM	64-QAM	256-QAM	64-QAM
Modulation BW (MHz)	100 / 400		100	250	100	400	400
Signal PAPR (dB)	13.17		>10	NA	9.64	NA	NA
EVM (dB)	-27.7		-25	-25.2	-25	-27.8	-26.1*
ACLR (dBc)	-32.0		-28.3	-27	-27.4	-32.8	NA
Pavg / PBO** (dBm / dB)	11/10.5		14.7/NA	17.7/6.6	16.7/7.2	8.9/10.9	15.4/7.9
Core Area (mm^2)	0.3	0.27	0.1	0.54	1.55	0.16	0.3
ITRS_FOM (dB)#	88.70	89.04	83.40	83.55	84.85	80.58	84.50

*Estimated from the figure. **$\mathrm{PBO(dB)} = \mathrm{OP1dB(dBm)} - \mathrm{Pavg(dBm)}$.
#$\mathrm{ITRS\_FOM} = \mathrm{Gain(dB)} + \mathrm{Psat(dBm)} + 20\log(\mathrm{fc(GHz)}) + 10\log(\mathrm{Peak\ PAE(\%)})$.

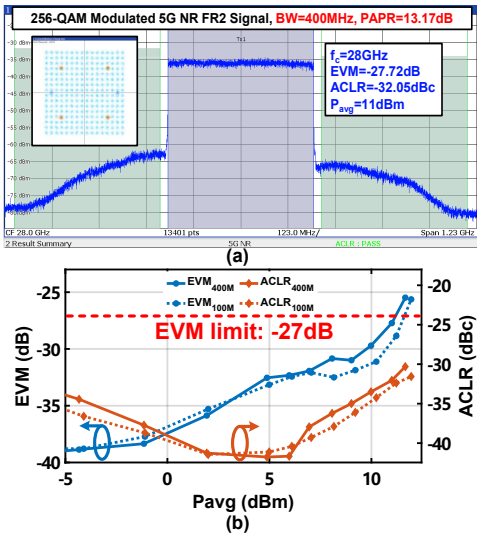

Fig. 9. Modulated signal measurement at 28 GHz using 5G NR FR2 256-QAM-OFDM signal, PAPR=13.17 dB. (a) Constellation and spectrum; (b)EVM and ACLR with bandwidth of 100 MHz and 400 MHz.

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REFERENCES

[1] E. Liu and H. Wang, "A 28-GHz Extremely Compact Doherty Power Amplifier With a Single Transformer-Based Doherty Active Load Modulation Matching Network," *IEEE Journal of Solid-State Circuits*, pp. 1–12, 2025.

[2] H.-C. Park, S. Kim, J. Lee, J. Jung, S. Baek, T. Kim, D. Kang, D. Minn, and S.-G. Yang, "Single Transformer-Based Compact Doherty Power Amplifiers for 5G RF Phased-Array ICs," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 5, pp. 1267–1279, 2022.

[3] M. Pashaeifar, L. C. N. de Vreede, and M. S. Alavi, "A Millimeter-Wave CMOS Series-Doherty Power Amplifier With Post-Silicon Inter-Stage Passive Validation," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 2999–3013, 2022.

[4] G. Diverrez, E. Kerherve, M. De Matos, and A. Cathelin, "A 22-44 GHz 28nm FD-SOI CMOS 5G Doherty Power Amplifier with Wideband $\mathrm{PAE}_{6\mathrm{dBPBO}}$ Enhancement and 3:1 VSWR Resiliency," in *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2024, pp. 131–134.

[5] E. Liu and H. Wang, "A Broadband Four-Way Parallel–Series Doherty Power Amplifier for 5G Communications," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 5, pp. 1312–1322, 2024.

[6] Z. Ma, K. Ma, K. Wang, and F. Meng, "A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier With 20.4%/14.2% PAE at 6-/12-dB Power Back-off and 25.5dBm PSAT in 55nm Bulk CMOS," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 320–322.

[7] X. Zhang, H. Guo, and T. Chi, "32.1 A 47GHz 4-way Doherty PA with 23.7dBm P1dB and 21.7% / 13.1% PAE at 6 / 12dB Back-off Supporting 2000MHz 5G NR 64-QAM OFDM," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, 2024, pp. 520–522.

[8] V. Qunaj and P. Reynaert, "A Ka-Band Doherty-Like LMBA for High-Speed Wireless Communication in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3694–3703, 2021.

[9] W. Zhu, J. Ying, L. Chen, J. Zhang, G. Lv, X. Yi, Z. Zhao, Z. Wang, Y. Wang, W. Chen, and H. Sun, "32.8 A 27.8-to-38.7GHz Load-Modulated Balanced Power Amplifier with Scalable 7-to-1 Load-Modulated Power-Combine Network Achieving 27.2dBm Output Power and 28.8%/23.2%/16.3%/11.9% Peak/6/9/12dB Back-Off Efficiency," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, 2024, pp. 534–536.

[10] H.-W. Choi, J. Yun, J. Jeong, I. Lee, G. Park, Y. Kim, H. Choi, H.-C. Park, and C.-H. Park, "An Ultra-Compact, >17 dBm POUT, >30% PAE, Single Transformer- Based Doherty PA in 28-nm CMOS FD-SOI for 5G FR2 UE AiP Products," in *2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2025, pp. 67–70.

[11] J. Zhao, H. Jia, Q. Peng, W. Deng, Z. Gao, X. Duo, Z. Wang, and B. Chi, "A K-band Process-Corner Robust Balanced Power Amplifier Utilizing Current-Mode Adaptive Biasing Network in 65-nm CMOS," in *2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2025, pp. 227–230.

[12] L. Liu, Y. Fang, Q. Zhou, T. Chi, and S. Li, "A mm-Wave Doherty Power Amplifier in a Single-Path Footprint Using Compact Reciprocal Doherty Networks," in *2026 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 69, 2026, pp. 344–346.

[13] H. Gao, S. M. Mahani, D. Seebacher, M. Bassi, and G. Hueber, "A 24-30 GHz Broadband Doherty PA with a maximum 15.37 dBm Pavg and 14.6% PAEavg in 0.13 m SiGe for 400 MHz BW 5G NR," in *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, 2022, pp. 337–340.