Analog FoMs and Programmable Analog Building Blocks of TIG-RFETs in 22 nm FDSOI Technology

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***Abstract*—In this work, TIG-RFETs fabricated on a 22 nm FDSOI technology are evaluated for analog applications from the device level to the circuit level. Device measurements show useful analog figures of merit (FoM) in both n- and p-configurations, together with monotonic tuning by the program gates and the back gate. This tunability is then transferred to circuit operation through demonstration of a common-source amplifier and an RFET-based current mirror. The current mirror shows a clear saturation-like output region and a finite compliance voltage range, while preserving RFET-specific polarity programmability. We demonstrate in simulations that the same concepts can be applied to more practical designs, such as a Wilson current mirror. These results position FDSOI RFETs as an attractive technology for programmable and tunable low-power analog designs by exploiting their extra electrostatic degree of freedom.**

***Index Terms*—Reconfigurable Field Effect Transistors, 22nm FDSOI, Tunable Analog FoM, Current Mirrors.**

I. Introduction

As CMOS scaling approaches its physical and economic limits, novel device concepts are increasingly being explored to provide functions beyond conventional CMOS and to enable more flexible circuit design. Reconfigurable field-effect transistors (RFETs) are attractive in this context because their polarity can be programmed during operation. This property has already been exploited in digital circuits for polymorphic logic and hardware security [1]–[4], while in analog circuits, the ambipolar and gate-tunable nature of RFETs has enabled functions such as frequency doubling [5]. Importantly, RFETs can be integrated into existing FDSOI technology without new materials or complex process modifications, which makes them promising for practical circuit implementation [5]–[7].

Beyond polarity switching, the program gates of an RFET also provide an additional electrostatic degree of freedom for tuning the device characteristics [8], [9]. This is highly relevant for analog design, where tunability is increasingly needed to cope with process spread, mismatch, supply variation, and low-voltage operation. Recent TCAD studies on multi-gated RFETs have shown that electrical tuning can strongly affect key analog and RF FoM, indicating strong potential for tunable analog building blocks [10]. However, these studies remain mainly simulation-based, and experimental validation on fabricated devices is still limited [11]. RFET tunability can be transferred from device level to circuit level, opening new possibilities for analog circuit design [9], [12], [13]. Recently, a Ge RFET current mirror able to electrostatically tune the I_{OUT}/I_{IN} ratio was demonstrated as a proof-of-principle study [14]. While this result established RFET tunability at circuit level and experimentally demonstrated an electrostatically adaptable current mirror, the study mainly emphasized ratio tunability. In addition, a more detailed examination of the output characteristics of the mirror, including the I_{OUT}-V_{OUT} behavior, output resistance, and compliance voltage, can further expand the analog relevance of RFET-based current mirrors.

In this work, we experimentally investigate the analog potential of TIG-RFETs fabricated in a 22 nm FDSOI technology by combining device-level characterization with circuit-level validation. We first evaluate the analog FoM in both n- and p-configurations and examine their electrostatic tunability through the program and back gates, thereby establishing the accessible analog design space of the RFET. We then study basic analog circuits to assess how this tunability is transferred to circuit operation. For the current mirror, we move beyond ratio tunability and directly discuss the output behavior relevant for practical use, including the I_{OUT}-V_{OUT} characteristics, output resistance, and compliance voltage. Finally, simulation of a Wilson current mirror suggests that RFET tunability can support a broader range of analog circuit concepts.

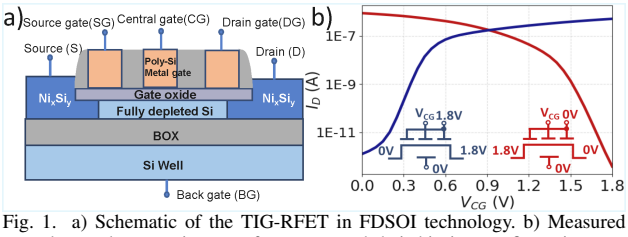

Fig. 1. a) Schematic of the TIG-RFET in FDSOI technology. b) Measured n- and p-mode saturation transfer curves and their biasing configurations.

II. FDSOI RFET Analog FoM and its Tuning Knobs

The focus of this work is on the TIG-RFET, a three-independent-gate Schottky barrier transistor fabricated in 22 nm FDSOI technology on 300 mm wafers [7]. As shown in Fig. 1a), TIG-RFETs employ Schottky source and drain contacts. The source gate (SG) and drain gate (DG) overlap the two Schottky junctions and control carrier injection at the source and drain sides, respectively. The central gate (CG),

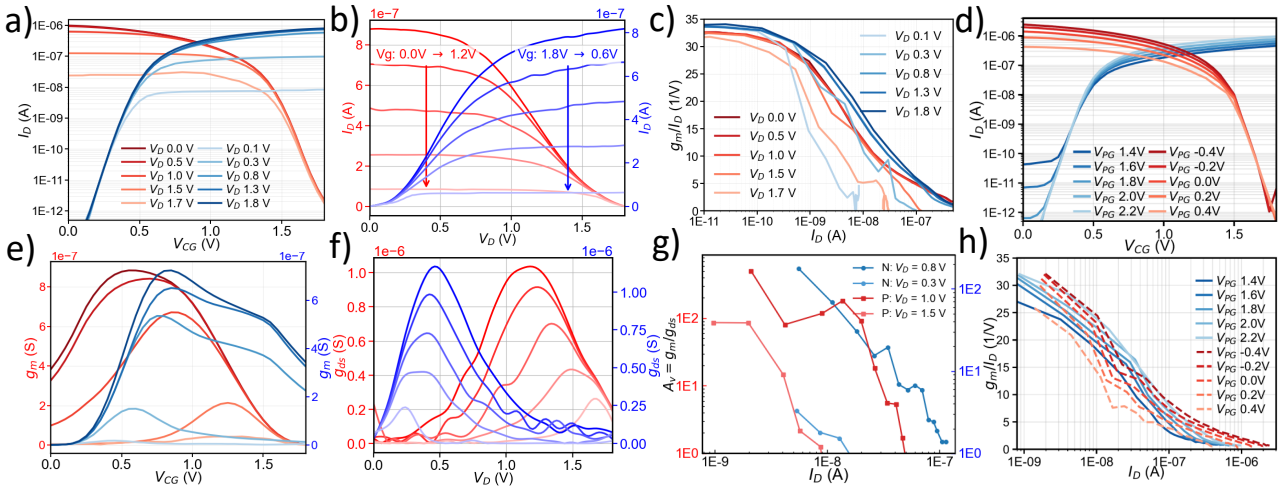

Fig. 2. Measured I-V characteristics and analog FoM of the FDSOI RFET. a) Transfer characteristics at different V_D. b) Output characteristics at different V_G. c) Transconductance efficiency at different V_D. d) Transfer characteristics for different V_{PG}. e) Transconductance g_m-V_G characteristics. f) Output conductance g_{ds}-V_D characteristics. g) Intrinsic gain $A_v = g_m/g_{ds}$ versus I_D. h) Transconductance efficiency for different V_{PG}.

located between them, controls the potential barrier in the middle of the channel. The DG defines the device polarity by suppressing the injection of unwanted carrier type from the drain. The device can operate in different modes depending on whether the SG or CG gate is used as the steering gate. Since SG steering shows contact-limited transconductance behavior [15], which is less suitable for analog operation, this work focuses on CG steering, in which the current is modulated by thermionic emission over a potential barrier in the middle of the channel. In the CG steered configuration, the SG and DG are biased together and act as the program gate (PG). The SG controls carrier injection from the source, while the DG suppresses the opposite carrier type, and together they provide an additional degree of freedom for current tuning. As shown in Fig. 1b), both the n- and p-configurations operate within the same voltage range (0-1.8V) while maintaining symmetric on currents. In FDSOI, the back gate (BG) provides an additional tuning knob and can further adjust both the threshold voltage and the drive current.

Fig. 2 summarizes the main I-V characteristics and analog FoM of the CG steering mode RFET in both n- and p-mode. The transfer curves show clear gate control and a strong increase of I_D with V_D. The extracted g_m reaches about 7×10^{-7}S and 8.2×10^{-7}S in n- and p-mode, respectively, confirming that both polarities can provide a useful transconductance. The g_m/I_D characteristics show peak values close to 31–34 V^{-1} for both modes, which indicates that the FDSOI RFET can keep a high transconductance efficiency in the low current region. In this region, the dependence on V_D is relatively weak, indicating that the RFET maintains a stable low-power analog bias window at small drain current. However, at higher current levels a clear dependence on V_D emerges, showing that g_m/I_D is not determined by drain current alone but is also strongly affected by the drain bias. This suggests that a sufficiently large V_D is required to establish a stable analog operating region. From the output characteristics in Fig. 2b) and f), a clear reduction of g_{ds} is observed as the device moves from low V_D to the saturation region, which is the main condition for voltage gain. As a result, the extracted intrinsic gain $A_v = g_m/g_{ds}$ shows a meaningful analog operating window in both polarities, as shown in Fig. 2g). In n-mode, the most representative behavior is obtained at V_D = 0.8 V, where A_v remains around 10 over a broad current range and increases further at lower current. At V_D = 0.3 V, the gain degrades quickly, indicating that too small drain bias is less favorable for voltage amplification. In p-mode, the clearest gain window is obtained at V_D = 1.0 V, where A_v falls in the 10 to 10^2 range. These results indicate that the FDSOI RFET provides a bias-tunable and polarity-reconfigurable analog operating window, with finite intrinsic gain, useful transconductance efficiency, and well-defined bias regions relevant to amplifier operation.

In Fig. 2d), the I_D-V_G curves under different V_{PG} show a clear modulation of the current level. Taking the n-mode as an example, as the SG and DG voltages increase simultaneously, the source Schottky barrier becomes thinner, which enhances electron tunneling injection and increases the current level. Meanwhile, the drain has a raised Schottky barrier for holes, suppressing the injection of the opposite carrier type from the drain side and thereby lowering the off-current. As a result, the transfer curve becomes steeper and the on/off ratio improves. Fig. 2h) shows that increasing V_{PG} shifts the g_m/I_D characteristics toward higher I_D. This means that a similar transconductance efficiency can be maintained at a larger drain current under higher V_{PG}. This is particularly relevant for analog design, since g_m/I_D is commonly used as a measure of transconductance efficiency and to evaluate the trade-off among gain, power efficiency, and speed. The right shift therefore indicates that increasing V_{PG} enables operation at higher current levels while preserving a comparable g_m/I_D.

The back gate offers another tuning knob, mainly for threshold adjustment. Static back-gate biasing has been used for analog circuits mismatch compensation [16]. As shown in Fig. 3a), both the n- and p-type transfer curves shift systematically with V_B, indicating that the back gate provides a strong and monotonic threshold-tuning effect. To evaluate whether this tuning remains suitable for analog operation, Fig.

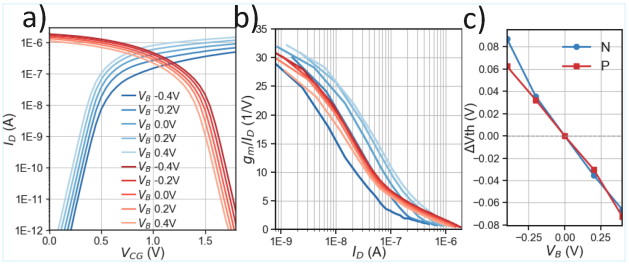

Fig. 3. Back-gate tuning characteristics of FDSOI RFET. a) Transfer curves under different V_B. b) Transconductance efficiency under different V_B. c) Extracted V_{th} shift versus applied V_B.

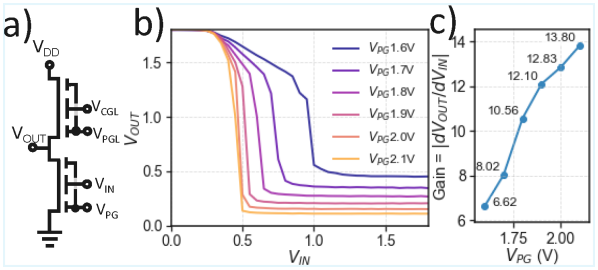

Fig. 4. PG tuning of a common-source amplifier. a) Schematic of the amplifier. The suffix L denotes the RFET used as an active load. b) Voltage transfer characteristics measured for different V_{PG} values. c) Extracted voltage gain, defined as $|dV_{OUT}/dV_{IN}|$

3b) compares transconductance efficiency. It shows p-curves are largely unchanged but n-type g_m/I_D changes with V_B, indicating V_B is not a perfectly orthogonal knob in this recent technology iteration. However, the overall g_m/I_D behavior remains reasonably preserved, especially over the current range relevant for circuit operation. Besides, the behavior and trend remain monotonic and predictable, so the back gate is a practical and quantitative knob for ΔV_{th} mismatch correction, even though it is not a perfectly orthogonal tuning parameter.

III. RFET-based Amplifier and Current Mirrors

Above DC electrical characterizations probe intrinsic device properties, but they do not yet represent amplifier operation, since no circuit-level load or output node is defined. To evaluate voltage amplification, the RFET was implemented in a common-source amplifier using an inverter structure, with the upper transistor biased as an active load. For a fair gain extraction, the amplifier was biased at its switching threshold. With V_{DD} = 1.8 V, the input voltage (V_{IN}) was fixed at V_{DD}/2 = 0.9 V, and the gate bias of the upper transistor (V_{CGL}) was swept to shift the voltage transfer characteristic. A sharp output transition across V_{DD}/2 was obtained when V_{CGL} was around 0.98 V. This bias point was therefore selected for the measurements, since it places the inverter close to its switching point, where the VTC slope is maximized, and the voltage gain can be extracted consistently. As shown in Fig. 4b) and c), increasing V_{PG} leads to a progressive steepening and left shift of the voltage transfer characteristic. The gain increases monotonically from 6.62 to 13.8 as V_{PG} is raised from 1.6 V to 2.1 V. The circuit trend follows the device trend, confirming that V_{PG} tuning can be directly translated from device physics to analog functionality.

In order to further confirm that PG tuning remains effective at the circuit level, an RFET-based current mirror is implemented, as shown in Fig. 5a), and characterized. Fig. 5b) and c) show that the same topology can operate either as a current sink or as a current source when the RFETs are programmed in the n-type and p-type configurations, respectively. More importantly, the measured output characteristics show a clear transition from a low V_{OUT} region to a saturation-like region, where I_{OUT} depends only weakly on V_{OUT}. This indicates that the circuit exhibits the essential output behavior of a practical current mirror, namely a finite compliance range and a non-zero output resistance. The dependence on I_{IN} further supports this interpretation. In Fig. 5c), increasing I_{IN} mainly shifts the output-current level, while the overall output shape is maintained. The extracted I_{OUT}-I_{IN} relation in Fig. 5d) remains monotonic, which confirms controlled current scaling in the mirror operating region. Although the mirror ratio is below unity under the present bias condition, the behavior is systematic and reproducible. The program gate provides an additional circuit-level tuning knob. As shown in Fig. 5e), increasing V_{PG2} continuously raises the mirrored current while preserving a clear saturation-like region in the I_{OUT}-V_{OUT} characteristics. The corresponding I_{OUT}-I_{IN} curves in Fig. 5f) show that the effective mirror ratio can be tuned electrostatically. Therefore, the extra gate degree of freedom of the RFET is transferred from device-level programmability to analog circuit functionality. Unlike prior work that mainly emphasized ratio tunability, these results also reveal the output characteristics expected from a usable current mirror.

One extra RFET can be used to form a Wilson current mirror, as depicted in Fig. 6a), which can stabilize the current over a wide V_{DS} range. This design was simulated using a compact model in [17] to validate the transferability of the tunability concept to more advanced low-power analog topologies. As illustrated in Fig. 6b), the topology gives rise to a high intrinsic output resistance (R_{out}) over a wide output voltage swing, even when the RFET model with sloped saturation region is used. The Wilson current mirror can adjust the input-to-output current ratio by varying the V_{PG} voltage. With I_{IN} = 10 nA, the output current can change by a factor of five. As illustrated in Fig. 6c), the presented circuit can work with input currents ranging from 100 pA to 20 nA, however, the I_{OUT}–I_{IN} ratio becomes increasingly nonlinear for lower V_{PG} voltages, indicating that sufficiently high V_{PG} is required for proper current mirroring.

IV. Conclusion

In this work, we experimentally evaluated the analog potential of TIG-RFETs from 22nm FDSOI technology, from device level to circuit level. At device level, the measured transfer and output characteristics, together with the extracted small-signal parameters, show that the RFET provides meaningful analog FoMs in both n- and p-configurations, while the program gate and back gate offer monotonic electrostatic tuning of the operating point. A common-source amplifier further confirms that this extra gate degree of freedom is preserved at the circuit level and can be used to tune analog behavior after fabrication. Most importantly, the RFET-based current mirror not only provides electrostatic ratio tuning, but

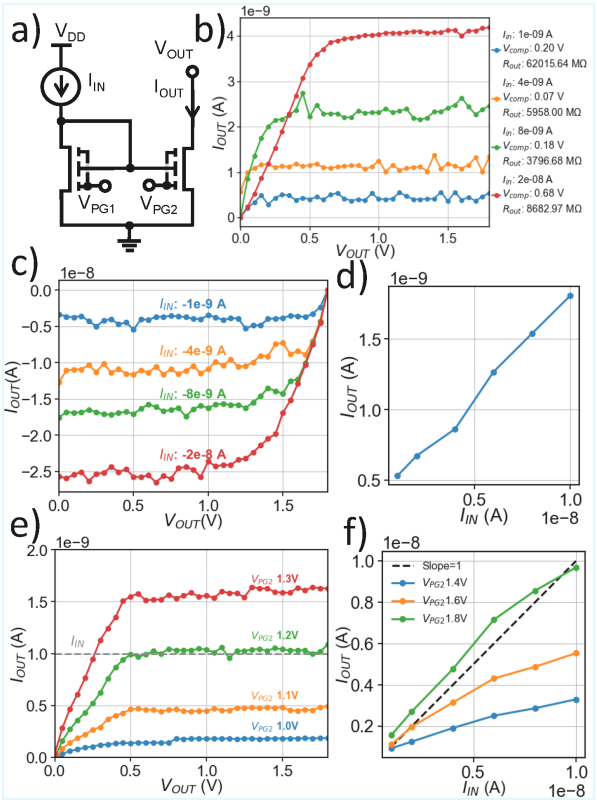

Fig. 5. a) Schematic of the TIG-RFET current mirror. b) Measured output characteristics in sink mode for different I_{IN}, with extracted compliance voltage and output resistance. c) Measured output characteristics in source mode for different I_{IN}. d) Extracted I_{OUT} as a function of I_{IN} in the operating region V_{OUT}=1.8V. e) Measured I_{OUT}-V_{OUT} characteristics for different V_{PG2} and f) corresponding I_{OUT}-I_{IN} at V_{OUT}=1.8V, with V_{PG1} fixed at 1.8 V.

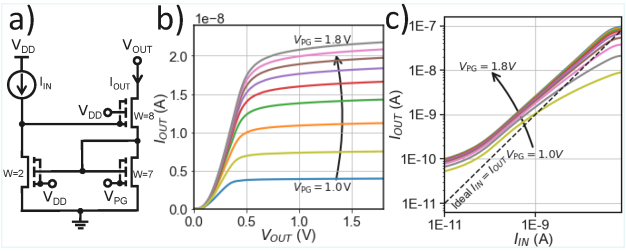

Fig. 6. a) Schematic of TIG-RFET Wilson current mirror. W denotes the relative transistor size used in the simulation. b) Simulated DC characteristics of the RFET Wilson current mirror. The 10nA input current can be tuned with V_{PG} to output currents from 4 nA to 22 nA. c) The RFET Wilson current mirror can operate with input currents I_{IN} ranging over more than two decades.

also exhibits favorable mirror output characteristics, including a saturation-like output region, finite compliance range, and controlled current transfer. In addition, RFET-specific polarity programmability is retained, allowing the same topology to operate as either a current source or a current sink. Finally, preliminary simulation of a Wilson current mirror suggests that the measured device properties can be extended to more advanced low-power analog topologies. These results show that RFETs in FDSOI technology are promising candidates for tunable analog building blocks that combine polarity reconfigurability with practical analog functionality.

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