A 20 MHz Bandwidth, 100 dB Dynamic Range Logarithmic Detector with ±1 dB Log-Conformance Error

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***Abstract*—Log-conformance error (LCE) of a successive detection logarithmic amplifier (SDLA) can be reduced using signal-strength detectors with linear or sub-linear dependence on input amplitude. This work combines absolute-value detectors to reduce the LCE, clamps to reduce internal swings, and increase the bandwidth, and appropriate temperature dependence for amplifier bias currents to implement a logarithmic detector with > 100 dB dynamic range, ±1 dB LCE, and 20 MHz bandwidth over the −40 to 125°C temperature range. Measurement of 32 devices shows a 43.1 mV/dB nominal slope, and an untrimmed slope variation of ±2.8% across this temperature range. The minimum detectable is 21 μV_p and improves to 10 μV_p with a front-end LNA.**

I. Introduction

In recent years, ultrasound sensors have been used in various applications such as proximity measurement and object detection. The need to detect the strongest as well as the weakest echoes of the transmitted signal mandates wide dynamic range receivers. One of the methods for wide dynamic range signal-strength detection is to use a logarithmic detector (LD)[1], [2]. Due to its open-loop structure, logarithmic detectors are attractive in high-speed applications, but accuracy is a concern[3]. Applications like double sheet detection, bubble detection, material detection, and wireless spectrum sensing require a dynamic range of more than 80 dB and bandwidths of the order of a MHz to tens of MHz[4], [5].

This paper describes a successive-detection logarithmic detector IC with a dynamic range exceeding 100 dB, and a log-conformance error (LCE) of less than ±1 dB. It has a 20 MHz bandwidth, and maintains a ±2.8% accurate slope over a −40°C to 125°C temperature range across 32 devices. It is shown that log-conformance error (LCE) can be reduced using an absolute-value signal-strength detector instead of the conventional square-law detector. High bandwidth for large-signal operation is maintained by suitably clamping the internal nodes of the signal-strength detector. Slope accuracy over temperature is maintained by using a combination of proportional-to-absolute temperature (PTAT) bias currents in the amplifier chain and zero-temperature coefficient (ZTC) bias currents in the signal-strength detector. A front-end low-noise amplifier (LNA) and an external band-pass filter (BPF) are optionally used to reduce the minimum detectable signal.

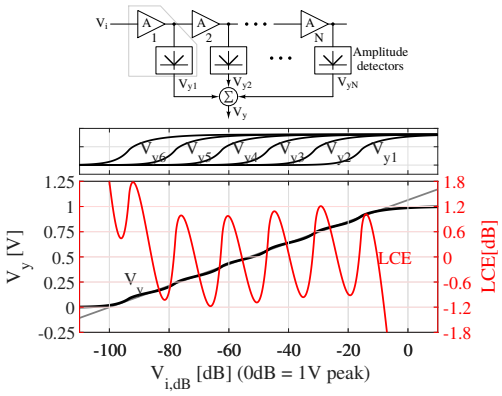

Fig. 1. Successive-detection logarithmic amplifier and typical characteristics[2].

II. Successive detection logarithmic detector

Fig. 1 shows the successive detection logarithmic amplifier (SDLA). It consists of a cascade of amplifiers with saturating amplitude detectors from the output of each stage. The amplitude detector outputs are summed to get the logarithmic detector output. The figure also shows the individual amplitude-detector outputs V_{y1} to V_{y6} and the log detector output V_y. V_{y1} to V_{y6} are geometrically spaced. Their separation equals the amplifier gain A. When added, they result in the logarithmic curve V_y. V_y versus (log) input amplitude is a straight line with ripples over a certain range. The deviation from the ideal logarithmic line is called the log-conformance error (LCE) and is also shown in the figure. The error comes from the constant gain between the saturation points of two successive stages. The amplitude detector can be realized using any even function. Fig. 2(a) shows some examples. It includes a linear full-wave rectifier realizing $|X|$ and a square-law detector realizing $|X|^2$. The characteristics in Fig. 1 assumed a square-law amplitude detector and $A = 6$. Fig. 2(b) shows the logarithmic detector characteristics when $|X|$ and $|X|^2$ are used for amplitude detection. The ripple is visibly higher in the latter. The peak-peak LCE is 1.8 dB with $|X|$ and 3 dB with $|X|^2$. This is because $|X|$ has a higher gain at low signal-strength and a lower gain for a high signal-strength compared to $|X|^2$, which more mimics the logarithmic function. Therefore $|X|$ amplitude detection is used in this design. The LCE generally depends upon the interstage gain A [6]. For a given dynamic

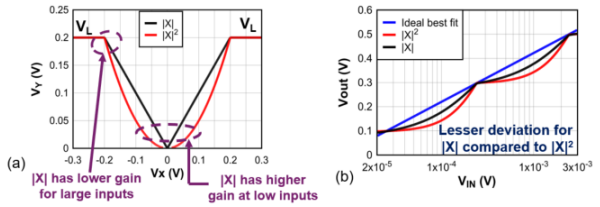

Fig. 2. (a) Amplitude-detector characteristic examples, (b) logarithmic detector characteristics using $|X|$ and $|X|^2$ for the amplitude detector.

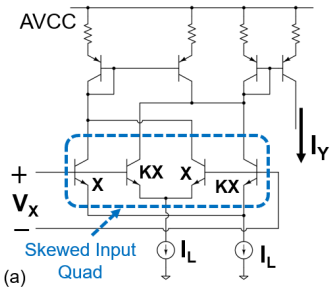

Fig. 3. Conventional amplitude detector using two skewed differential pairs[7], [8].

range, reducing the gain and increasing the number of cascaded stages in the successive detection logarithmic amplifier makes the characteristics smoother and reduces LCE. But more stages with smaller gain imply a higher power consumption, more die area, and a higher input-referred noise. The present design uses six stages with $A = 10\,(20\,\text{dB})$ to realize a target dynamic range exceeding 100 dB.

III. Amplitude Detector with Rectifying Characteristics

Fig. 3 shows the conventional amplitude detector using a parallel combination of two $K:1$ skewed differential pairs[7], [8]. Its output current is given by

$$I_Y = \frac{2I_L(K^2-1)}{K^2 + 2K\cosh(V_X/V_t) + 1} \tag{1}$$

where V_X is the input, and V_t is the thermal voltage. For small inputs, it follows the square-law expression given below.

$$I_Y(V_X) \approx \frac{2I_L(K-1)}{K+1}\left[1 - \frac{K}{(K+1)^2}\left(\frac{V_X}{V_t}\right)^2\right] \tag{2}$$

As discussed in Section II an absolute-value amplitude detector yields a lower LCE. Fig. 4 shows the proposed implementation. The input V_X is applied to the differential pair $Q_{1,2}$ with a tail current $2I_L$. The bias current I_L is subtracted at the collectors using the transistors $Q_{3,8}$. The difference currents are mirrored using two current mirrors $Q_{4,5}$ and $Q_{6,7}$. The current mirror outputs are added to obtain the output current I_Y. During positive half cycles of the input V_X, Q_7 cuts off, and the positive half cycle is mirrored through $Q_{4,5}$. During negative half cycles of the input V_X, Q_4 cuts off, and the positive half cycle is mirrored through $Q_{6,7}$. Thus, full-wave rectification is achieved. Q_9 and Q_{10} are used to clamp the collector nodes. Without them, during negative half cycles of the input, the collector of Q_1 gets pulled up to AVCC because of the current pushed from Q_3. During the positive half cycles, the collector is pulled down to AVCC-VEB. The resulting large-signal swing limits the bandwidth of the amplitude detector. With this technique, the detector's bandwidth increases by 250% with an extra bias current of only about 10%. When Q_9 and Q_{10} are added, the collector voltage is clamped to $V_{c,ref}$+VEB. To ensure robust operation, $V_{c,ref}$ is generated using a replica circuit to ensure that the collector swings of $Q_{1,2}$ are minimized across PVT corners.

The maximum output of Fig. 4 is I_L. When used in an SDLA with amplifiers of gain A, the slope (referred to dB input) is $I_L/20\log(A)$ [6]. To maintain a constant slope, I_L and A are kept constant in this design. Fig. 5(a) shows the amplifiers are realized as differential pairs with resistive loads followed by emitter-follower buffers. PTAT current is used in this stage to maintain a constant gain with temperature. Therefore, a ZTC current reference is used for I_L. With this choice, the gain (voltage to current) of the amplitude detector falls with temperature in complimentary-to-absolute temperature manner but its input-referred saturation voltage increases in PTAT ($4V_t$) manner. When this cell is used in an SDLA, both the minimum and maximum values increases by the same factor, keeping the dynamic range same with temperature.

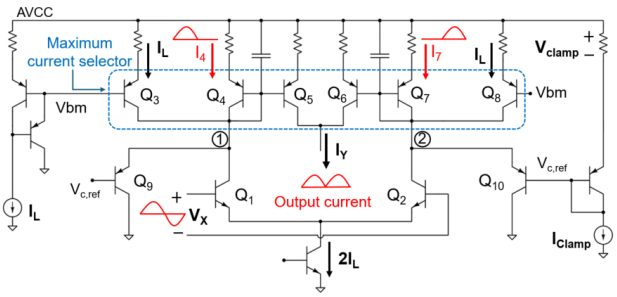

Fig. 4. Proposed rectifying amplitude detector.

Fig. 5(b) shows the simulated characteristics of the conventional (Fig. 3) and the proposed (Fig. 4) amplitude detectors. Fig. 5(c) shows the SDLA characteristics using the two amplitude detectors. The smaller ripple and LCE with the proposed detector are evident. Tab. I shows the comparison of simulated performance with the SDLAs of equal power consumption, showing 55% LCE improvement, and for equal dynamic range, there is 40% of power reduction.

IV. Prototype Chip

Fig. 6 shows the six-stage SDLA implemented in the prototype. It consists of three amplifier stages, a unity gain stage, and two attenuation stages, a combination of cascade and parallel gain stage implementation to achieve maximum dynamic range. A comparator is added at the end of the amplifier chain. It toggles at the input signal frequency, which helps to determine whether

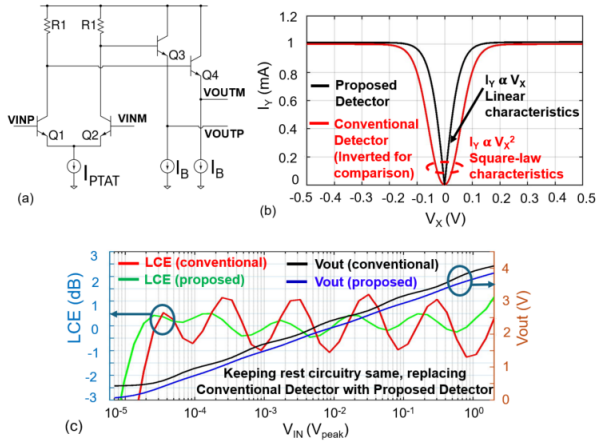

Fig. 5. (a) Amplifier stage, (b) Characteristics of the conventional and proposed amplitude detectors, (c) Simulated SDLA characteristics based on them.

TABLE I
SIMULATED COMPARISON OF THE SDLA USING THE CONVENTIONAL AND PROPOSED AMPLITUDE DETECTOR CELLS

	For equal power		For equal performance	
	Proposed	Conventional	Proposed	Conventional
Power	7.8 mW	7.8 mW	7.8 mW	13.2 mW
LCE	±0.5 dB	±1.1 dB	±0.5 dB	±0.5 dB
Input range	15 μV_p to 1.4V_p	22 μV_p to 2.2V_p	15 μV_p to 1.4V_p	15 μV_p to 1.4V_p
Dynamic range	99.4 dB	100 dB	99.4 dB	99.4 dB

the received signal is the desired one. The comparator has a sensitivity of 300 μV_p for 20 MHz at SDLA input across the temperature range. The SDLA can be used with single-ended or differential inputs.

Fig. 7 shows the IC block diagram. It consists of a closed-loop front-end low-noise amplifier(LNA) with ~ 20 dB gain and a −3 dB large-signal bandwidth (LSBW) of 36MHz. An external bandpass filter(BPF) centered at the desired frequency can be optionally connected between the LNA and the SDLA to filter out the noise of the LNA and out-of-band signals. The current output of the SDLA is driven to off-chip R_F and C_F, which set the slope and response time, respectively. The detector tail current I_L is also generated using an external resistor to get constant output voltage. The input can be applied to the LNA for processing small inputs and directly to the SDLA for large inputs. Both the LNA and SDLA are internally dc biased and ac-coupled using external capacitors. External capacitors help to operate at the desired frequency band.

V. Measurement Results

The IC is implemented in a BiCMOS process. Fig. 8 shows the chip photograph. The chip operates from 3 V to 5.5 V. The SDLA consumes 3.9 mA and the LNA consumes 2.1 mA. Fig. 9 shows the measured results with a 5 V supply. Fig. 9(a) shows the results for the AFE (LNA + off-chip BPF + SDLA). For LCE = ±1 dB, the minimum detectable signal is 4/4.5/10 µV peak with 40kHz/1MHz/20MHz inputs with correspondingly centered BPFs with BPF gain of −17dB/−4.4dB/−7dB, and

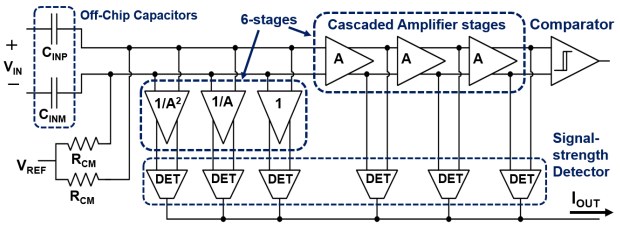

Fig. 6. SDLA implemented on the chip.

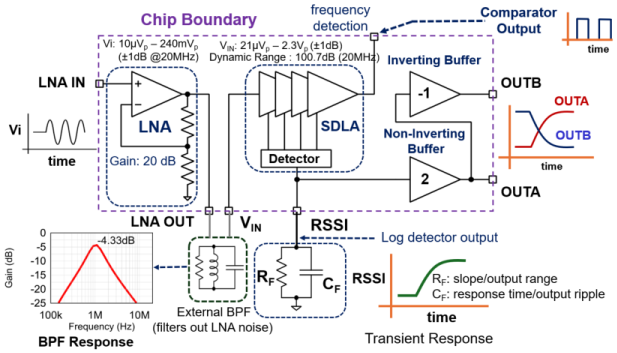

Fig. 7. Chip block diagram.

the maximum signal is 240 mV peak. This corresponds to a dynamic range of 95.7/95/87dB at 40kHz/1MHz/20MHz. Fig. 9(b) shows the measured SDLA results. For LCE = ±1 dB, the minimum detectable signal is 20/21 µV peak and the maximum signal is 2.7/2.3V peak corresponding to a dynamic range of 102.6/100.7dB at 1MHz/20MHz. Fig. 9(d-f) show the consistency in the slope and minimum detectable signal across 32 devices. The SDLA achieves a slope drift of 120ppm/°C and a variation of ±0.45 dB of dynamic range across the temperature range for 20MHz. Fig. 9(c) shows the consistent LCE from −40°C to 125°C within an input range from 23.7 µV peak to 2.23V peak at 20MHz. Table II shows the performance summary and comparison. The standalone logarithmic detector (without the LNA) is compared to other logarithmic detectors. The chip presented here has a much higher bandwidth than [3], which has a comparable dynamic range and has a much higher dynamic range than the wide bandwidth designs in [1], [2], [6], [9]. The SDLA with the LNA and external BPF centered at 20MHz is compared to the ultrasound analog front-end in [10]. The work presented here has a higher bandwidth. The higher figure-of-merit confirms the overall performance of the proposed design. Fig. 10 shows the test setup for double-sheet detection and the measured signal levels with single and double sheets.

VI. Conclusions

Log-compliance error (LCE) of a SDLA depends on the gain of amplifier stages(A) used in the chain and also on the individual signal-strength detector characteristics. It is shown that LCE is lower for absolute value detectors compared to

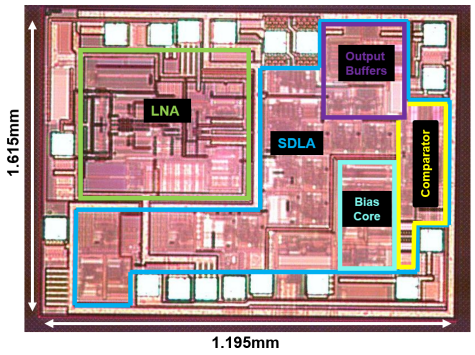

Fig. 8. Chip photograph. Die area = 1.93 mm^2.

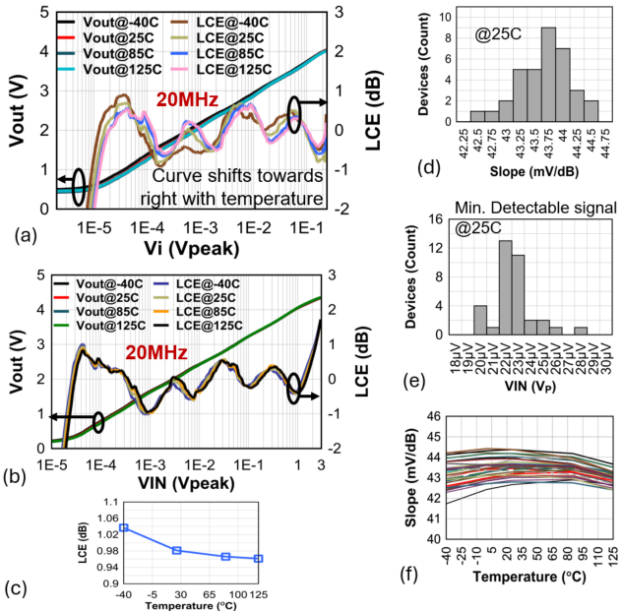

Fig. 9. Measurement results from −40°C to 125°C: (a) LNA+BPF+SDLA characteristics, (b) SDLA characteristics, (c) LCE (dB) of SDLA, (d)-(f) Measured results across 32 devices.

square-law detectors. Using a combination of rectifying signal-strength detectors and appropriate temperature dependence for the bias currents, stable and wide-dynamic range operation with low LCE is demonstrated over a wide temperature range and a large number of devices.

VII. Acknowledgment

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TABLE II
Performance summary and comparison

Performance Metrics	Standalone Logarithmic Detector						LNA + BPF + SDLA	
	This Work (SDLA)	Pranav SSCS-L'23 [2]	Byun TCAS-I'14 [6]	Huang JSSCC'00 [1]	Wu[a] JSSC'05 [9]	Siemssen[b] ISSCC'25 [3]	This Work (AFE)	TUSS4440[c] [10]
Process	BiCMOS	65nm CMOS	180nm CMOS	600nm CMOS	350nm CMOS	180nm SOI-BCD	BiCMOS	CMOS
Active Area (mm^2)	1.93	0.08	0.6	0.4	2.25	1.33	1.93	-
Bandwidth (MHz) (±1dB LCE)	0 – 20	1 - 22	30	22.6	110	0.136[d]	0 - 20	0 - 1
Dynamic Range (dB) (±1dB LCE)	100.7	70	55	75	80	101.9	86.9	77
Input Range (mV_{peak}) (±1dB LCE)	0.021 – 2300	0.8 – 2514	0.1414 – 3552	-	-	0.00316 – 400	0.0109 – 241	0.007 - 50
Signal Frequency Detection	Yes	No	No	No	No	No	Yes	No
Typical LCE (dB)	±1	±1	±0.5	±1	±0.7	±0.5	±1	±1
Supply (V)	5	1.5	1.8	2	3	5	5	3.1
Quiescent Current (mA)	3.9	0.36	2.6	3.1	13	1.53	6	11.5
Power dissipation (mW)	19.5	0.54	4.68	6.2	39	7.65	30	34.5
Figure of Merit (dB)**	190.8	176.1	153	170.62	174.5	174.4	175.14	151.48

**: $FOM = DR + 10 * \log_{10}(\frac{Bandwidth\ (Hz)}{Power\ (W)})$ [3]

[a] : The paper includes VGA; [b] : multi-mode operations with logarithmic amplifier similar to logarithmic detector; [c] : The paper includes on-chip BPF; [d] : bandwidth limited by PGA.

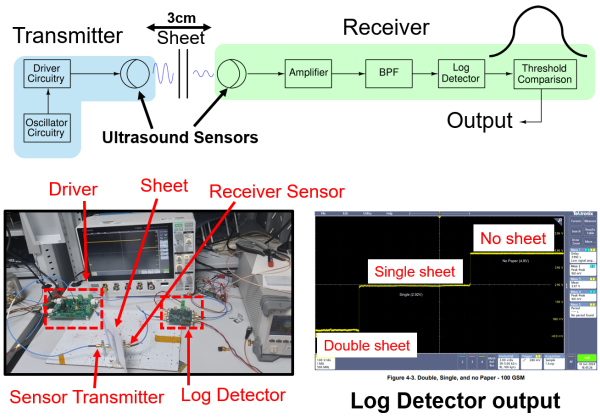

Fig. 10. Demonstration of double-sheet detection.

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