A Compact Single-Chip Four-Mode Reconfigurable CMOS Frequency Multiplier for 28/39/60/77-GHz Signal Generation

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***Abstract*—This paper presents an ultra-compact single-chip reconfigurable CMOS frequency multiplier supporting four multiplication modes (×2/×3/×4/×6) to cover the 28/39/60/77-GHz bands for joint communication and sensing (JCAS) applications. The design features a single-path reconfigurable core that utilizes dynamic conduction-angle modulation to transition between amplification and mixing operations, enabling seamless switching between frequency doubling and self-mixing tripling. Moreover, a harmonic phase-alignment technique is proposed to maximize the third-harmonic output power while concurrently enhancing common-mode rejection. Fabricated in a 65-nm CMOS, the prototype occupies a core area of only 0.25 mm². Measurements demonstrate peak output powers of -3.84, -6.71, -0.19, and -3.52 dBm for ×2, ×3, ×4, and ×6 modes, respectively. All conversion modes exhibit a harmonic rejection ratio (HRR) exceeding 20 dBc. To the authors' best knowledge, this is the first single-chip CMOS frequency multiplier to support four modes, achieving an ultra-wideband frequency coverage from 26.8 to 83.4 GHz.**

***Keywords*—reconfigurable frequency multiplier, multi-band, ultra-compact, phase-alignment technique, self-mixing, CMOS.**

I. Introduction

The rapid evolution of millimeter-wave (mm-Wave) systems toward the 6G era is driving a fundamental transition from standalone communication links to fully integrated joint communication and sensing (JCAS) architectures [1]. As illustrated in Fig. 1, emerging JCAS applications necessitate frequency-agile hardware capable of robust operation across a wide spectrum of standardized bands. Specifically, this entails seamlessly accommodating the 28/39-GHz bands for 5G FR2 [2], the 60-GHz band for short-range high-data-rate links [3], and the 77-GHz band for high-resolution automotive radar [4]. Frequency multipliers play a critical role in such architectures for generating high-frequency local oscillator (LO) signals. Conventional multi-band solutions typically rely on wideband LO chains, which suffer from significant power consumption and large area occupation. Moreover, designing a voltage-controlled oscillator (VCO) with an excessively wide tuning range inevitably compromises its phase-noise performance. To address these challenges, reconfigurable frequency multipliers have emerged as a compelling alternative, enabling multi-band coverage while significantly relaxing the tuning range requirements of the preceding VCO.

In recent years, various reconfigurable frequency multipliers have been proposed [5]-[8]. In [5], a differential pair combined with a wideband 1-bit phase shifter and a driver amplifier based on variable transmission lines is utilized to achieve the 2nd and 3rd harmonics. To further improve integration and performance, an injection-locking frequency

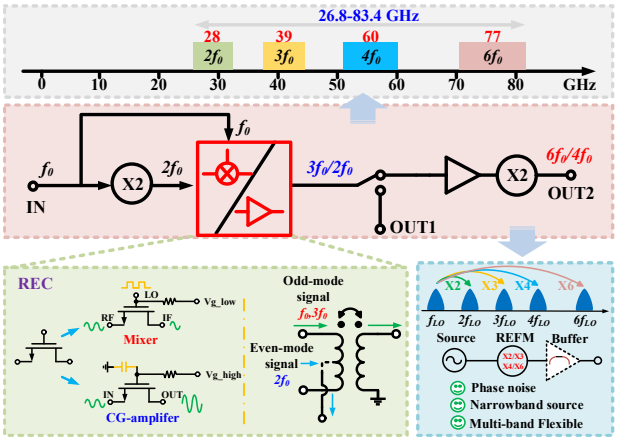

Fig. 1. Proposed compact single-chip four-mode reconfigurable CMOS frequency multiplier for 28/39/60/77-GHz signal generation.

multiplier in 55-nm CMOS was proposed in [6], employing Class-C operation and transformer-based injection networks to switch between ×2 and ×3 modes across 20.7-43.8 GHz range. Furthermore, a multi-channel active architecture utilizing Marchand baluns and power splitters has been developed to cover fragmented bands from V-band to G-band [7]. More recently, a dual-channel ×2/×3 multiplier employing shared-core broadband output networks was demonstrated in [8]. Nevertheless, existing designs still suffer from a relatively low output power and large area resulting from multi-channel or parallel-branch topologies. Additionally, a single-chip solution capable of bridging the vast frequency gap from 28 to 77 GHz remains an unresolved challenge.

In this paper, an ultra-compact quad-mode (×2/×3/×4/×6) reconfigurable CMOS frequency multiplier is proposed, achieving the first single-chip integration for 28/39/60/77-GHz signal generation. The design features a cascaded-reuse architecture centered on a single-path reconfigurable core (REC). By leveraging dynamic conduction-angle modulation, the REC enables a seamless transition between frequency doubling and self-mixing tripling, maximizing hardware utilization. A harmonic phase-alignment technique is further introduced to boost the third-harmonic output power, while the passive networks are systematically co-designed to ensure wideband performance for higher-order (×4/×6) harmonics. The fabricated prototype in 65-nm CMOS achieves a core area of only 0.25 mm² and delivers peak output powers of -3.84, -6.71, -0.19, and -3.52 dBm across the four modes. This work attains a state-of-the-art balance among wide-spectrum coverage, signal performance, and area efficiency.

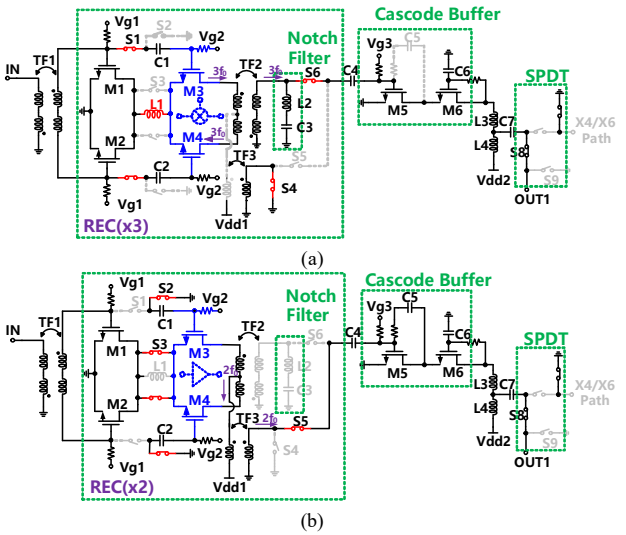

Fig. 2. Schematic of the reconfigurable core in (a) ×3 and (b) ×2 modes.

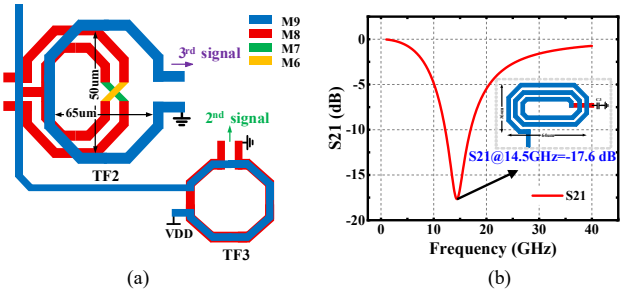

Fig. 3. (a) The EM layout of the transformer-based balun (TF2 and TF3) and (b) the layout of the LC notch filter and simulated performance.

II. Circuit Implementation

Fig. 1 presents the block diagram of the proposed four-mode reconfigurable frequency multiplier. The architecture integrates a reconfigurable core (REC) supporting ×2/×3 conversion, followed by a cascode buffer, a single-pole double-throw (SPDT) switch, and a wideband frequency doubler. Mode reconfiguration within the REC is achieved by dynamically modulating the conduction angles of the active devices and reassigning the functionality of the passive components. For high-order harmonic generation (×4/×6), the REC serves as a high-spectral-purity driver to excite the subsequent doubler stage. This cascaded-reuse strategy significantly minimizes the silicon footprint while ensuring robust performance across all four operational modes.

A. Single-Path Reconfigurable ×2/×3 Multiplier Core

In the frequency-tripling (×3) mode, as shown in Fig. 2(a), transistors M_3 and M_4 are biased in the sub-threshold region to operate as a single-balanced mixer. This topology performs a self-mixing operation between the fundamental and second-harmonic signals generated by the preceding stage (M_1 and M_2). Capacitors C_1 and C_2 function as DC-blocking elements, ensuring that the multiplier and mixer stages can be biased independently without mutual interference. Subsequently, the generated differential third-harmonic signal is converted to a single-ended output via a transformer-based balun (*TF2*) and

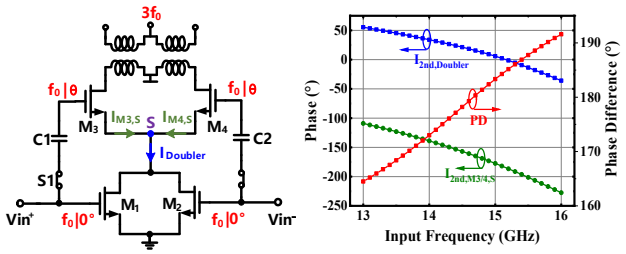

Fig. 4. (a) The topology of the conventional current-reuse self-mixing tripler. (b) Simulated 2nd harmonic current phase and phase difference.

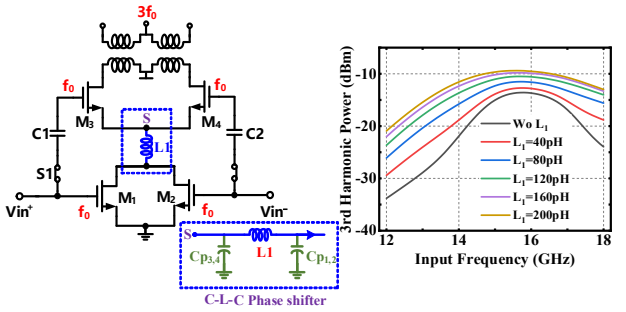

Fig. 5. (a) The proposed harmonic phase-alignment current-reuse self-mixing tripler. (b) Simulated 3nd harmonic output power with L_1.

then injected into the output amplifier. Given that the fundamental tone also propagates as an odd-mode signal, it inherently leaks through the balun. To suppress this unwanted leakage and enhance fundamental rejection, a series *L-C* resonant tank (L_2 and C_3), precisely tuned to the fundamental frequency, is strategically embedded between *TF2* and the output buffer as a notch filter.

Conversely, in the frequency-doubling (×2) mode depicted in Fig. 2(b), the gate bias voltage (V_{g2}) of M_3 and M_4 is increased from 0.6 V to 1.0 V, shifting their operation into the saturation region. In this state, M_3 and M_4 are reconfigured as a common-gate (CG) amplifier. Concurrently, C_1 and C_2 are reconfigured as decoupling capacitors for the CG amplifier. The desired second-harmonic signal, primarily generated by the push-push differential pair, is amplified by the CG stage and extracted as an even-mode signal from the center tap of the *TF2* primary coil. An auxiliary transformer, *TF3*, is employed to provide inter-stage impedance matching between the CG amplifier and the subsequent buffer. The physical layouts of the multi-functional transformers (*TF2*, *TF3*) and the *L-C* notch filter are detailed in Fig. 3.

In summary, the proposed single-path reconfigurable architecture leverages dual-functional active components to achieve a high degree of hardware sharing. This approach enables state-of-the-art area efficiency while maintaining high-performance signal generation across all modes.

B. Harmonic Phase-alignment Technique

In the proposed REC, the ×3 mode employs a current-reuse self-mixing architecture, as shown in Fig. 4(a). The generation of the third-harmonic current (I_{3nd}) primarily originates from the mixing of the fundamental (V_{1st}) and the second-harmonic (V_{2nd}) voltages. Consequently, maximizing the voltage swing

of V_{2nd} at the node S is imperative for achieving optimal ×3 conversion efficiency. Assuming the push-push frequency doubler is driven by differential fundamental signals $Acos(\omega_0 t)$ and $Acos(\omega_0 t+\pi)$, and θ denotes the relative phase difference, the total second-harmonic voltage at node S ($V_{S,2nd}$) can be derived as:

$$\begin{aligned} V_{S,2nd} &= Z_S\,(I_{M3,S} + I_{M4,S} - I_{Doubler}) \\ &= Z_S(K_{M3}cos(2\omega_0 t+2\theta)+K_{M4}cos(2\omega_0 t+2\theta) \\ &\quad - K_{M1,2}\cos(2\omega_0 t)) \end{aligned} \tag{1}$$

As indicated in (1), $V_{S,2nd}$ is determined by the vector superposition of the doubler's output current ($I_{Doubler}$) and the intrinsic nonlinear second-harmonic currents from the mixing transistors (M_3 *and* M_4). For a given node impedance Zs, the maximum amplitude of $V_{S,2nd}$ is obtained only when these current components add constructively in phase. Theoretical analysis suggests that such in-phase addition requires a specific relative phase alignment, that is, it needs to satisfy θ=-90°. However, simulated phase responses (Fig. 4(b)) reveal a critical design bottleneck, the phase difference between $I_{M3/4,S}$ and $I_{Doubler}$ approaches 180° across the target frequency band. Under this out-of-phase condition, the second-harmonic currents from the doubler and mixers arrive at node S with nearly opposite phases, leading to significant signal cancellation that severely degrades the tripling conversion power. Conventional solutions using phase shifters or couplers to restore this 90° shift are occupied a large area.

To address this issue, a novel harmonic phase-alignment technique is proposed. As shown in Fig. 5(a), a series inductor (L_1) is strategically embedded between the doubler and mixing stage. This inductor serves a dual purpose by first resonating with the complex parasitic capacitances at node S to form an equivalent C-L-C phase-shifting network, which effectively compensates for the phase misalignment. Furthermore, L_1 facilitates impedance transformation between the capacitive output of the doubler and the resistive input of the mixers, thereby optimizing common-mode power transfer at $2f_0$. As shown in Fig. 5(b), the systematic optimization of L_1 yields a substantial enhancement in the third-harmonic output power.

C. High-order ×4/×6 Signal Generation

To synthesize the higher-order harmonics (×4/×6), the preceding ×2/×3 core acts as a high-purity driver to excite a final wideband push-push doubler. Generating a flat output response across such widely separated ×4 and ×6 bands requires overcoming the inherent high-frequency gain roll-off of the active devices. To mitigate this, multi-stage passive networks are systematically co-designed.

The electromagnetic (EM) models and physical dimensions of these three critical matching networks are detailed in Fig. 6. Empowered by this broadband matching strategy, the final doubling stage achieves a peak conversion gain of 3.5 dB

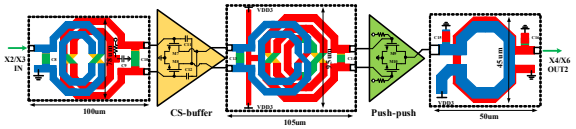

Fig. 6. Schematic of the higher-order ×4 and ×6 modes with EM model and physical size of matching networks.

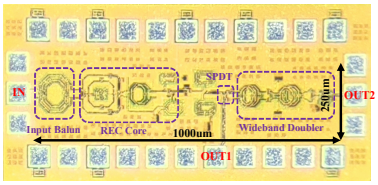

Fig. 7. Die photograph fabricated in 65-nm CMOS.

alongside an exceptionally wide 3-dB bandwidth of 54.6-84.4 GHz (44% fractional bandwidth). This extensive frequency coverage fully accommodates the spectral requirements for both ×4/×6 modes, ensuring robust, high-purity signal generation across the entire target millimeter-wave spectrum.

III. Measurement Results

The proposed fully-differential quad-mode reconfigurable frequency multiplier was fabricated in 65-nm CMOS process. The chip micrograph is shown in Fig. 7, with an active core area of only 0.25 mm × 1 mm.

The simulated and measured input and output reflection coefficients (S11 and S22) are plotted in Fig. 8. For the ×2/×3 modes, the measured S11 is below -10 dB from 14 to 16.2 GHz, while the S22 is better than -7 dB across the 36.6 to 48.3 GHz. For the ×4/×6 modes, the S11 stays below -10 dB across 14.8-16.8 GHz, and notably, the S22 is well below -10 dB over an extensive bandwidth from 50 to 90 GHz. Fig. 9 illustrates the measured conversion gain (CG) characteristics. Measurements were conducted with constant input power of -6.5 dBm for the ×2 and ×3 configurations, and -1 dBm for the ×4 and ×6 modes. The ×2 mode achieves a peak CG of -5.38 dB at 30.8 GHz with a 3-dB bandwidth of 5.2 GHz (26.8-32 GHz), ×3 reaches -9.31 dB (36.6-44.4 GHz), ×4 delivers 2.56 dB (52.4-60 GHz), and ×6 demonstrates -7.4 dB with an impressive 11.8-GHz bandwidth (71.6-83.4 GHz).

The measured output power versus input power at optimal carrier frequencies is presented in Fig. 10. The multiplier delivers peak output powers of -3.84, -6.71, -0.19, and -3.52

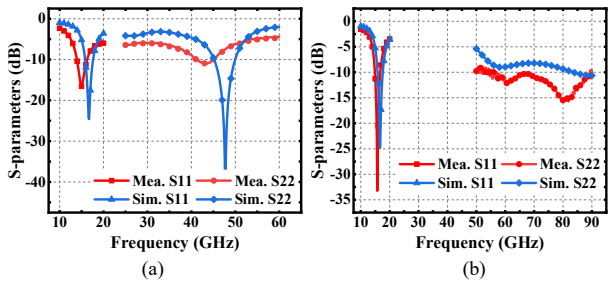

Fig. 8. Measured and simulated S-parameters. (a) ×2/×3 and (b) ×4/×6 modes.

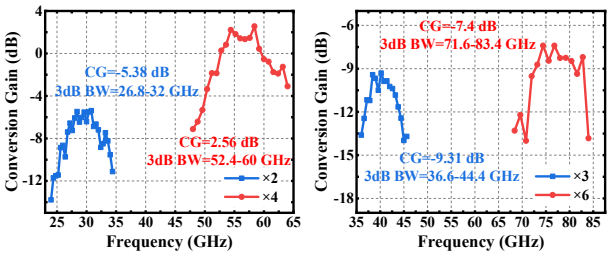

Fig. 9. Measured conversion gain. (a) ×2/×4 and (b) ×3/×6 modes.

TABLE I

PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART RECONFIGURABLE FREQUENCY MULTIPLIER

Ref.	Process	Multiplication Factor	Frequency (GHz)	CG (dB)	Output Power (dBm)	Harmonic Rejection Ratio (dBc)	Pdc (mW)	Core Area (mm^2)
IMS'19 [5]	120nm SiGe	×2/×3	19.6-25@×2 29.1-35.4@×3	N/A	5.6@×2 3.4@×3	>27 (19.6-25 GHz) >25 (29.1-35.4 GHz)	60@×2 60@×3	0.63
JSSC'22 [6]	55-nm CMOS	×2/×3	21-29.32@×2 33.9-41.4@×3	N/A	-8.8@×2 -11.6@×3	>42.89 (23-29.32 GHz) >30.4 (33.9-41.1 GHz)	12@×2 9.6@×3	0.46*
TCAI'26 [8]	40-nm CMOS	×2/×3	110-174@×2 167-254@×3	N/A	2@×2 -3.8@×3	>25 (110-174 GHz) >6 (167-254 GHz)	42@×2 57@×3	0.15*
IMS'23 [7]	40-nm CMOS	×2/×4/×8	52-66@×2 106-132@×4 211-252@×8	N/A	2@×2 2@×4 -4@×8	N/A	275	1.17*
This Work	**65-nm CMOS**	**×2/×3/×4/×6**	**26.8-32@×2** **36.6-44.4@×3** **52.4-60@×4** **71.6-83.4@×6**	**-5.38@×2** **-9.31@×3** **2.56@×4** **-7.4@×6**	**-3.84@×2** **-6.71@×3** **-0.19@×4** **-3.52@×6**	**>35 (26-30 GHz)** **>29.6 (36-42 GHz)** **>31.7 (52-60 GHz)** **>20.5 (72-82.8 GHz)**	23@×2 22@×3 70@×4 69@×6	**0.25**

*Including pads.

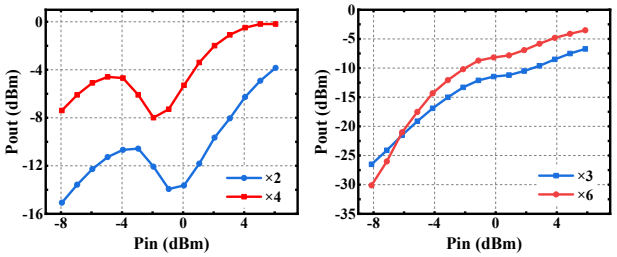

Fig. 10. Measured output power vs. input power. (a) ×2/×4 (b) ×3/×6 modes.

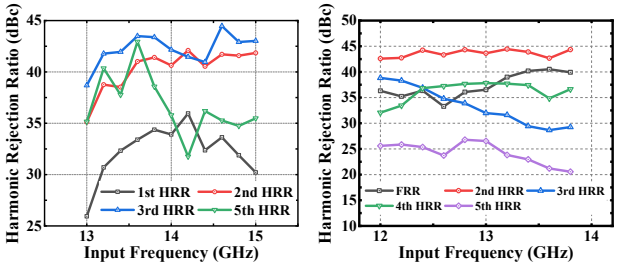

Fig. 11. Measured FRR and HRR. (a) ×4 and (b) ×6 modes.

dBm for the ×2, ×3, ×4, and ×6 modes, respectively. Finally, as plotted in Fig. 11, the harmonic rejection ratio (HRR) exceeds 20 dBc across the entire operating bandwidth for all modes, verifying exceptional spectral purity.

Table I summarizes the measured performance and benchmarks this work against state-of-the-art mm-Wave frequency multipliers. This design attains a superior balance between multi-octave frequency coverage, output power, and area efficiency. While most prior arts are constrained to dual- or triple-mode operation, this work achieves the first single-chip quad-mode reconfigurability (26.8–83.4 GHz), providing a highly integrated and versatile frequency synthesis solution for next-generation multi-standard systems.

IV. CONCLUSION

In this paper, a novel CMOS four-mode reconfigurable frequency multiplier is proposed and validated. By leveraging a single-path reconfigurable core integrated with a harmonic phase-alignment technique and a systematic broadband co-design strategy, the multiplier achieves high-performance ×2/×3/×4/×6 signal generation targeting for the 28/39/60/77-GHz bands. Measurement results demonstrate peak output powers ranging from -6.71 to -0.19 dBm, while maintaining a HRR consistently exceeding 20 dBc across all operational modes. This design attains an exceptional balance between spectral purity, wideband coverage, and area efficiency. To the authors' best knowledge, this is the first single-chip CMOS implementation supporting four distinct reconfigurable modes, providing a highly versatile frequency synthesis solution for future multi-band JCAS applications.

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