A 20kHz, 112dB SFDR, Extended-Counting ADC

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***Abstract*—This paper presents a highly-linear multi-bit incremental Delta-Sigma (I-DS) analog-to-digital converter (ADC) without the use of dynamic element matching (DEM) techniques or calibration for quantizer (QTZ) or digital-to-analog Converter (DAC). Extended Counting (EC) not only reduces the quantization noise but also suppresses the non-linearity errors of the multi-bit QTZ, while a DAC with first-order insensitivity to capacitor and reference level mismatch is employed. The design achieves 100 dB dynamic range (DR) over a 20 kHz bandwidth with FoM_{DR}=175.9 dB.**

I. Introduction

High-resolution and high-linearity Nyquist-rate ADCs are demanded in sensors and imagers, where single-shot conversion and multiplexing are required. I-DS ADCs operate on the principles of oversampling and noise shaping to achieve high resolution, and achieve Nyquist-rate conversion through periodic reset of the analog loop filter and the digital reconstruction filter [1]. State of the art (SoA) proposed various techniques to improve linearity as illustrated in Fig. 1. Some SoA use single-bit (SB) QTZ in the I-DS modulator (I-DSM) in order to achieve an intrinsically linear DAC operation [2]. However this comes with the disadvantages of reduced maximum stable amplitude (MSA), higher required oversampling ratio (OSR), and increased swings in the loop filter. MSA and OSR challenges can be remedied through recuperation phase (RP) and variable bitwidth (VBW) [3] techniques, and an FIR DAC can be employed to reduce the swings in the first integrator [3], [4]. However, the non-linear gain of the SB QTZ remains a challenge for high linearity [5]. Other SoA uses a multibit (MB) QTZ, allowing higher MSA and more aggressive loop-filter scaling to achieve higher resolution at a smaller OSR. However, the MB DAC unit-element mismatch errors needs to be addressed. Foreground calibration can be employed [6], which costs area and power especially in non-scaled CMOS and requires start-up time.

DEM techniques can be used to average and shape the DAC mismatch. DEM effectiveness is improved for lower DAC unit-element mismatch, and for larger OSR [7]. Data-weighted averaging (DWA) is a commonly used mismatch-shaping technique [8]–[10], but its effectiveness depends on signal amplitude and frequency [11]. For non-scaled CMOS, the area overhead for DWA is not to be underestimated [8]. Furthermore, DWA in I-DS ADCs is less effective compared to free-running (FR) Delta-Sigma modulators (DSMs) due to the non-uniform sample weighting in the reconstruction filter [12]. Higher-order DEM can improve efficiency [12], but the additional digital complexity imposes further challenges for non-scaled CMOS. Simple clocked averaging (CLA) was

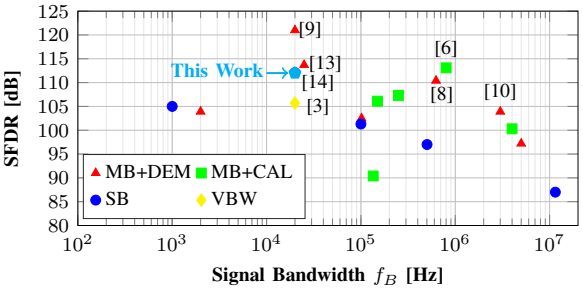

Fig. 1. SFDR of SoA incremental ADCs, grouped by DAC linearization [15].

successfully employed in [13], however the work featured an OSR = 8192 whose digital reconstruction filter implementation would be challenging in non-scaled CMOS.

An alternative is the 13-level dual DAC proposed for FR DSMs [11]. It is first-order insensitive to unit-element and reference-voltage mismatch and was called intrinsically linear [11]. Following the nomenclature of the original work, we refer to it in this manuscript as the 13-level dual DAC.

Another design challenge to be regarded is the MB QTZ nonlinearity. Mismatch in its decision thresholds leads to nonlinearity and thus harmonics which appear as increasingly prominent out-of-band (OOB) tones as they are shaped by the FR loop-filter noise transfer function (NTF) [11]. This should be addressed in the context of I-DS ADCs, as those OOB harmonics will fold back into the in-band frequency range and impact spurious-free dynamic range (SFDR) due to the lack of a brickwall decimation filter. To tackle both, DAC and QTZ nonlinearity, this work employs the highly linear MB dual DAC and it uses EC to suppress the MB QTZ nonlinearity.

II. IDS ADC with Extended Counting

The block diagram of the EC third-order I-DS ADC is shown in Fig. 2. The third-order I-DSM is based on a FR DSM prototype [11]. It operates at the original OSR = 60, at which the FR prototype achieved a thermal-noise limited in-band noise (IBN) of -102.5 dBFS. In incremental operation, this increases to -99.8 dBFS due to the noise-penalty factor from a third-order chain of integrators (CoI3) reconstruction filter [1]. Moverover, the estimated in-band quantization noise (IBQN) is only -100.6 dBFS [16] due to the inferior noise-shaping capabilities in incremental operation. With a combined IBN = -97.2 dBFS, the DSM from [11] is no longer dominated by thermal noise. Fortunately, the IBQN can be improved by employing EC in the I-DS ADC, The improvement is determined by the EC quantizer (QTZ_{EC}) resolution and the inter-stage gain (ISG); the latter is determined by the resolution

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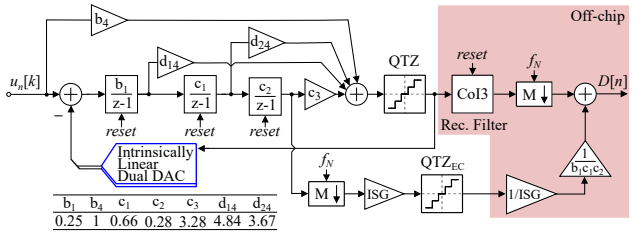

Fig. 2. Block diagram of the EC third-order I-DS ADC, featuring the highly-linear 13-level dual DAC in the feedback.

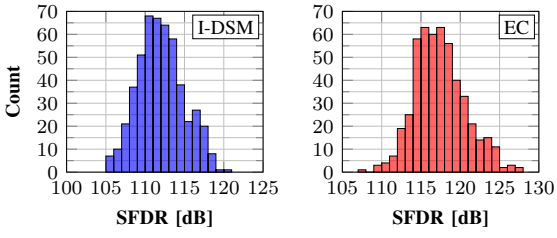

Fig. 3. Simulated SFDR at -3 dBFS input incl. QTZ threshold variation extracted from schematic. 500 Monte Carlo runs of the EC ADC from Fig. 2. OSR=60. (a) Without EC, (b) with EC.

of the first-stage QTZ, loop-filter scaling and the residual signal content in the loop filter [1]. To simplify the hardware implementation, the QTZ_{EC} is identical to the 13-level I-DSM QTZ. Using the performance prediction in [16], an ISG ≥ 20 is needed to achieve an IBQN = -110dBFS, which makes the EC I-DS ADC thermal-noise limited. The I-DSM coefficients, shown in Fig. 2, are reused from [11] with minor changes: the resonator is removed, and $b_4 = 1$ for improved transient settling after reset, and to ensure that the EC residue is dominated by quantization noise (QN) rather than signal content [1].

QTZ nonlinearity can limit the SFDR in high-resolution DSM. The QTZ nonlinearity could be prominently seen for a bandedge input signal in [11], as harmonic distortion appearing at the QTZ is shaped by the NTF; fortunately, the OOB tones are eliminated by a brickwall decimation filter in the FR Delta-Sigma (DS) ADC. In incremental ADCs, the reconstruction filter does attenuate, but not eliminate OOB components [1] and, due to decimation, the OOB tones fold into the in-band frequency range. Instead of calibrating for low-enough QTZ nonlinearity, [14] recently showed that the SB QTZ nonlinearity can be suppressed by employing EC. Consequently, we employ EC to address the MB QTZ nonlinearity.

System-level simulation is done in MATLAB. The QTZ threshold mismatch ($\sigma_{\text{QTZ}} = 7$ mV) is extracted from the original design [11]. The 13-level dual DAC mismatch has a negligible impact. Loop-filter gain errors are modeled, as a variation of b_4 impacts the SFDR improvement by altering the distribution of the extracted residue. The resulting SFDR histograms are shown in Fig. 3. Without EC, the simulated SFDR ($\mu = 112$ dB, $\sigma = 2.9$ dB) is about 6 dB worse as compared to with EC ($\mu = 117.5$ dB and $\sigma = 3.2$ dB). Even though in this Matlab simulation the boost is limited by the starting QTZ overload at the -3 dBFS input signal, and even though no further circuit non-linearities are included, this supports the possible impact of QTZ nonlinearity in high-performance I-DSM and the motivation to employ EC to suppress it.

III. Hardware Implementation

A simplified schematic of the EC I-DSM is presented in Fig. 4, which is extended from [11]. The dual-DAC reference voltages $V_{\text{ref(P,N)}}$ are generated on-chip. The first stage and the dual DAC feature cross-coupling and 4-phase operation at rate $2f_s$, denoted by the clock phases $\Phi_{1a}, \Phi_{1b}, \Phi_{2a}, \Phi_{2b}$, whereas the second stage samples the first integrator output during Φ_{2b}. This results in two successive integration cycles within one clock period t_s and enables sampling during each clock phase. The remaining loop-filter stages operate at rate f_s denoted by the clock phases Φ_1 and Φ_2. The loop-filter timing scheme is derived from the faster clock $2f_s$ [11].

For incremental operation, a periodic reset is applied to the DSM. If the reset violated the multi-rate timing scheme, e.g. due to misalignment, the early samples in each Nyquist conversion were corrupted, severely affecting the I-DS ADC performance [1]. Hence, the reset scheme shown in Fig. 4 was designed by using a single reset pulse, synchronizing it to the fast clock $2f_s$, and creating a gated reset pulse for each loop-filter stage to ensure that each stage can only produce an output after it has sampled its first valid input. The reset diagram is shown in Fig. 4: the first stage's reset (RST1) lasts until the first sampling phase Φ_{1a} elapses, then the remainder of the 4-phase operation $\Phi_{1b}, \Phi_{2a}, \Phi_{2b}$ produces the first valid output, which gets sampled by the second stage during Φ_{2b}. Afterwards, the second stage's reset (RST2) is disconnected to allow integration during Φ_1, hence producing the first valid output, which gets sampled by the third stage during Φ_1. The third stage and the adder resets follow the same principle.

The integrator operational transconductance amplifiers (OTAs) are realized using dynamically-biased pseudo-differential inverter-based amplifiers for efficiency and auto-zeroing, whereas the active adder's OTA is realized using a symmetrical OTA to allow a large output swing [11]. The QTZ is a 13-level Flash ADC employing 12 strongARM-latch comparators, and the QTZ thresholds generated from the resistive ladder are uncalibrated [11]. To relax the adder slew-rate requirements, the thresholds' range was shrunk to $(V_{\text{DD}} - V_{\text{SS}})/2$, effectively realizing a gain of 2 in the QTZ [11]. This is exploited in the EC realization: QTZ_{EC} is implemented as a copy of the I-DSM's QTZ, hence featuring a gain of 2 and realizing a portion of the ISG=20, c.f. Section II. The remaining x10 gain is explicitly realized by an amplifier implemented using a copy of the adder's symmetrical OTA. The ISG amplifier and QTZ_{EC} run every (and not only the last) clock cycle for the purpose of observing the internal state in this prototype. The QTZ and QTZ_{EC} output streams are converted to a binary bit stream using a thermo-to-binary converter. Then, they are transferred off-chip where the matched CoI3 filter (highlighted in red in Fig. 2) is implemented in MATLAB for debugging purposes.

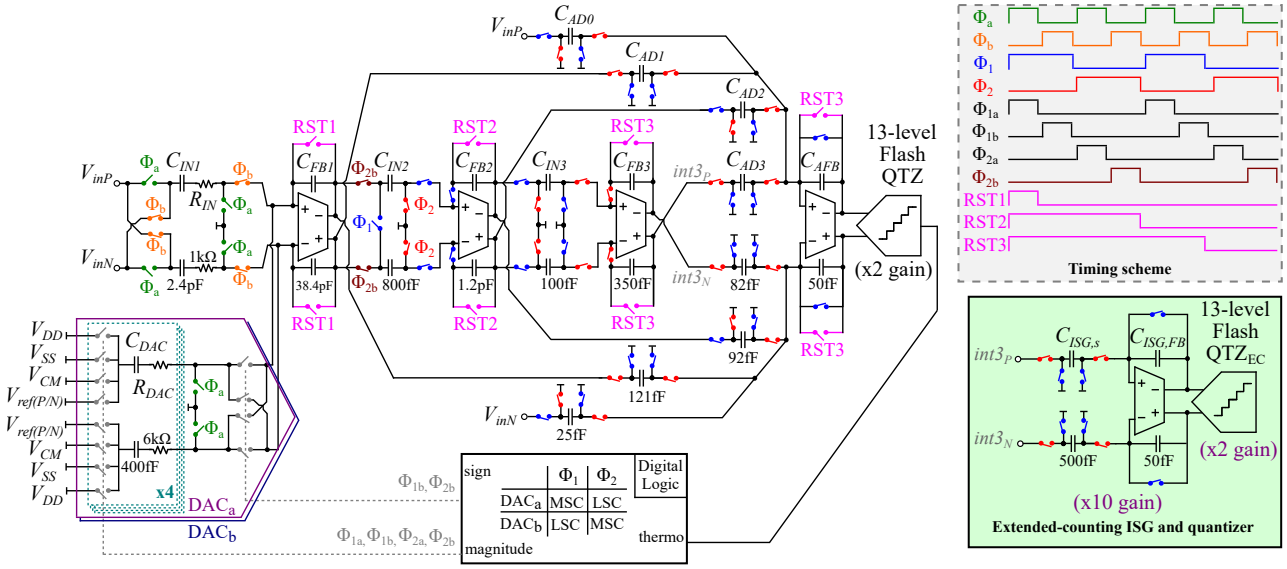

Fig. 4. Schematic of the EC third-order DT I-DS ADC employing the dual DAC. Timing scheme shows the reset scheme necessary for incremental operation.

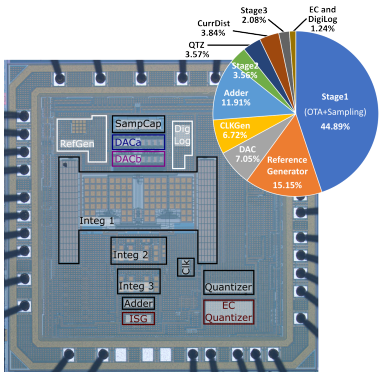

Fig. 5. Die photograph and power breakdown.

IV. Measurement Results

The design was implemented in 180 nm CMOS and a chip photo is shown in Fig. 5. The dual DAC, voltage reference generators, and the dual-DAC digital logic occupy less than 15 % of the design's total active area of 0.52mm^2. The main area contributions come from the sampling and integration capacitors; unfortunately, no high-density capacitor module was available during this prototyping process [11], leading to a rather severe area penalty.

The EC I-DS ADC runs with OSR = 60 for a signal bandwidth f_B = 20 kHz, and operates from 1.8 V. The power consumption is 514.7μW. The power breakdown is illustrated in Fig. 5, showing that the highly-linear dual-DAC and its voltage-reference generators consume less than 25% of the total power. The power consumption required for EC operation is negligible.

Fig. 6a shows the measured output spectrum of a -3 dBFS input signal at f_{in} ≈1 kHz. Thanks to EC suppressing the QTZ nonlinearity, the SFDR improves from 106.2 dB (without EC) to 112 dB with EC. Fig. 6b shows a band-edge measurement

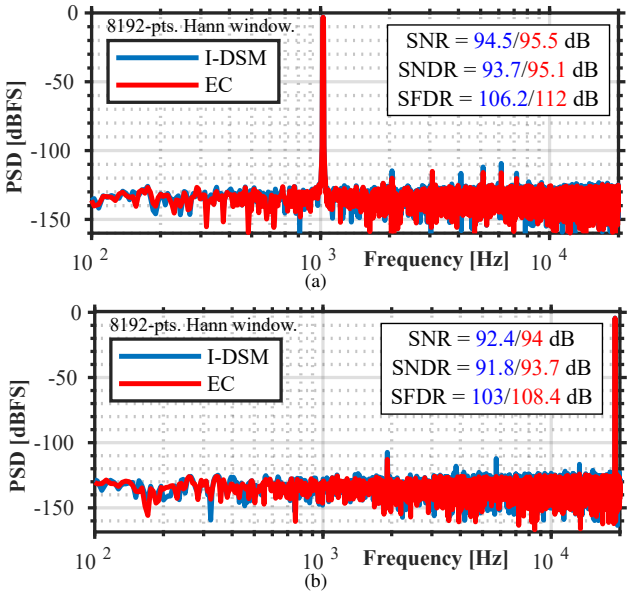

Fig. 6. Measured output spectra without (blue) and with (red) EC at -3 dBFS input. OSR= 60. (a) Deep in-band signal. (b) Band-edge signal.

at f_{in} ≈19.7 kHz, where the OOB harmonics are suppressed by EC before decimation and thus aliasing into the in-band; again, the SFDR is improved by almost 6 dB.

To further emphasize the capability of using EC to suppress QTZ nonlinearity, the measurement is repeated at a lower OSR. In this case, the QTZ nonidealities experience less suppression by the loop filter and thus dominate the achievable linearity. This is shown in Fig. 7 by operating the ADC with OSR = 45 and otherwise unchanged setup. Without EC, the SFDR degrades to 97.9 dBFS, clearly indicating that QTZ nonlinearity dominates. With EC, the SFDR improves by 10 dB. Note that at lower OSR, the dynamic loop-filter settling

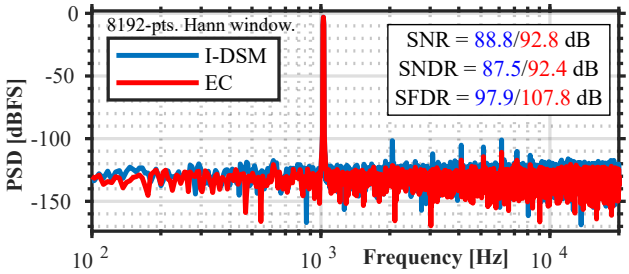

Fig. 7. Measured output spectra with (blue) and without (red) EC at -3 dBFS input. OSR=45. QTZ nonlinearity impact is stronger due to lower OSR operation.

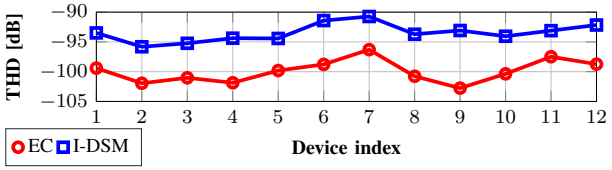

Fig. 8. Measured THD at -3 dBFS input across 12 devices, with OSR = 45.

and also signal content in the EC residue change slightly, which explains why the EC-based SFDR in Fig. 7 is slightly worse than in Fig. 6. This illustration is continued in Fig. 8, where a total of 12 devices is measured at OSR = 45, which makes them all limited by QTZ nonlinearity. By using EC, this suppresses their total harmonic distortion (THD) by 5..10 dB with a mean of 6.4 dB.

Measuring all 12 devices at the nominal OSR = 60, the SFDR is not always dominated by the QTZ nonlinearity in contrast to the shown OSR = 45. The achievable SFDR at OSR = 60 varies between 100 dB and 112 dB with EC-based improvements between 1.5 dB to 6 dB.

Fig. 9 shows the measured signal-to-noise ratio (SNR) and signal-to-noise-and-distortion ratio (SNDR) across input amplitude at the nominal OSR = 60. The 12 measured devices achieve almost identical performance of SNR=96.5 dB and SNDR=95.5 dB. The measured DR of 100 dB is consistent with the system-level IBN design, c.f. Section II.

A performance summary and a comparison to other high-linearity kHz-bandwidth SoA I-DS ADCs is given in Table I. The prototype achieves excellent linearity without DEM, calibration, or potential zoom-tracking issues. The OSR is half or less w.r.t. other SoA, thereby simplifying the complexity of digital filter implementation in non-scaled CMOS.

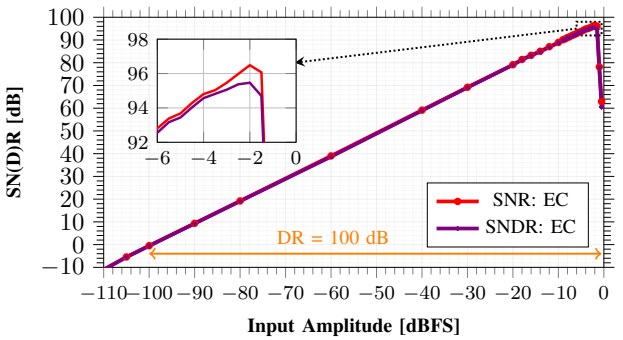

Fig. 9. Measured SNR/SNDR at OSR = 60.

Table I
COMPARISON TO SOA I-DS ADCS

	This work	L. Jie [13] ISSCC 2022	B. Wang [9] JSSC 2019	M. Mokhtar [3] ESSCIRC 2023	Z. Lu [14] TCAS1 2025
Arch.	**DT-EC**	CT-Zoom	DT-Linear-Exp.	DT-VBW-RP	CT-EC
Tech [nm]	**180**	28	65	180	55
Supply [V]	**1.8**	0.9/1.2	1.2	1.8	1.2
$f_{s,nyq}$ [kS/s]	**40**	50	40	40	40
OSR	**60**	8192	256	120	250
Power [μW]	**510**	590	550	500	188.6
SNR [dB]	**96.5**	-	-	98.2	95.4
SNDR [dB]	**95.5**	100.1	100.8	95.1	95.2
SFDR [dB]	**112**	113.7	121	105.7	112.1
DR [dB]	**100**	102.2	101.8	104	96.5
Linearization	**N/A**	CLA & DAC_{gain} cal.	DWA	N/A (VBW)	N/A (SB)
FoM_{DR} [dB]	**175.9**	178.4	177.4	180	176.7
FoM_{SNDR} [dB]	**171.4**	176.4	176.4	171.1	175.4

V. CONCLUSION

This paper presented a 112 dB SFDR I-DS ADC without DEM or calibration. DAC linearity is achieved by using a highly-linear 13-level DAC with low sensitivity to mismatch, while QTZ nonlinearity is suppressed by using EC. The I-DS ADC achieves 100 dB DR in a 20 kHz bandwidth, and FoM_{DR}=175.9 dB.

ACKNOWLEDGMENT

This work was partially funded by the German National Science Foundation DFG under grant OR 245/22-2.

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