A fractional-N DPLL using a stochastic TDC

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***Abstract*—A TDC based DPLL frequency synthesizer suitable for centralized frequency generation in antenna array systems is presented. A novel multi-mode stochastic TDC architecture is proposed. The stochastic parallel TDC structure breaks the tradeoff between increased thermal noise and reduced quantization noise inherent in series Vernier structures. Furthermore, the parallel structure results in relaxed linearity requirements of the sub-TDCs, allowing them to be designed using the available standard cell libraries. The DPLL was implemented in 22 nm FD-SOI CMOS technology and outputs a signal between 6.0 GHz to 7.1 GHz. It consumes 39.65 mW and measures a 89 fs and 166 fs jitter for integer and fractional frequency control word settings, respectively, when clocked by a 491.5 MHz reference, while the worst case reference spur measures -62 dBc.**

***Index Terms*—Phase locked loop, DPLL, stochastic TDC, antenna array systems, frequency synthesizer.**

I. Introduction

Frequency synthesis using digital phase locked loops (DPLL) in advanced CMOS technologies is attractive. Reduced voltage headroom, high reconfigurability and ease of adding new functionalities are among the factors considered when choosing a digital architecture. At the same time increased data rates in wireless communication systems have been a strong drive of stringent phase noise requirements. DPLLs with state-of-the-art jitter are thus in high demand.

DPLL architectures based on time-to-digital converters (TDC) have been losing momentum. The TDC is still very much an analogue subsystem affected by both noise and nonlinearity, and matching between delay cells is of paramount importance to reduce the PLL spur levels. Obtaining the required matching includes increasing the size of delay cells, and careful layout to balance the supply nets and account for some of the process variations. Furthermore, technology scaling has not sufficiently reduced the minimum delay of a cell so the TDC can provide the time resolution required to meet the increasing phase noise requirements. Vernier delay line TDCs [1] solve this issue by using two delay lines, one connected to the oscillator output signal (CKV) and other to the reference signal ($FREF$), the effective TDC time resolution then becomes equal to the nominal cell delay difference between the two lines. The structure of this TDC, however, does not allow for many layout options to improve matching given that each line has to be laid out in series. Since timing mismatches add up in the long delay lines, this makes linearity of the TDC a major bottleneck. Also scaling up the length of the delay lines to improve the TDC resolution results in an inherent trade-off between resolution and thermal noise as noise of many cascaded delay stages adds up, and increasing the device width to improve noise increases the power consumption.

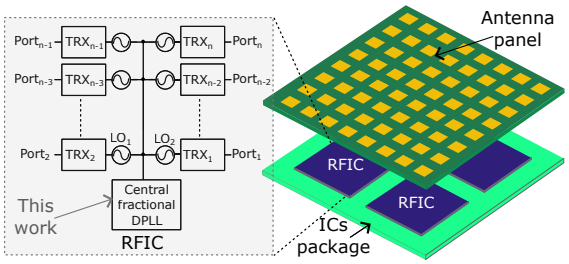

Fig. 1. An antenna array system where a central fractional-N DPLL provides reference for mm-wave LO generators.

In an antenna array system (AAS) a central synthesizer will result in significant power consumption, however, using simple local frequency multipliers performing integer frequency multiplication, the overall power saving can be significant. Similar to [2] an example for how this work can be employed in a mm-wave AAS is shown in fig.1.

In this article a fractional-N DPLL is presented benefiting from a new stochastic TDC architecture. The proposed TDC architecture effectively randomizes the non-linearity of the TDC while still maintaining low phase noise. The TDC uses a parallel structure, which reduces the effect of thermal and flicker noise originating from the delay lines. The TDC can also be configured as a series structure, allowing for an embedded frequency locked loop (FLL) operation for PLL lock acquisition. The DPLL is implemented in a 22 nm FD-SOI CMOS technology and the TDC is designed using standard cells allowing for both high performance and easy design, enabling smooth technology porting with reduced lead time.

II. Circuit Architecture and Design

A block level schematic of the DPLL test chip is shown in fig. 2. The proposed TDC is mainly designed using readily available standard cells since the linearity requirements on the parallel delay lines are relaxed. The digitally controlled oscillator (DCO) frequency range is 6.0 to 7.1 GHz while $FREF$ is generated in one of two ways, a 491.5 MHz input for testing purposes or a crystal resonator at 983.04 MHz connected to an oscillator which is internally frequency divided by two. Two memories, a high speed interface, and an SPI interface are included for testing.

A. Multi-mode stochastic TDC

The proposed TDC structure is shown in fig. 3. When used in PLL mode, multiple subTDCs (16 in this work) are operated in parallel. The subTDCs are designed using minimal number of delay cells to cover the required range under process, voltage and temperature (PVT) variations. Reduced delay line length relaxes the noise degradation issue present in Vernier TDCs. Furthermore, in contrast to Vernier architectures, since

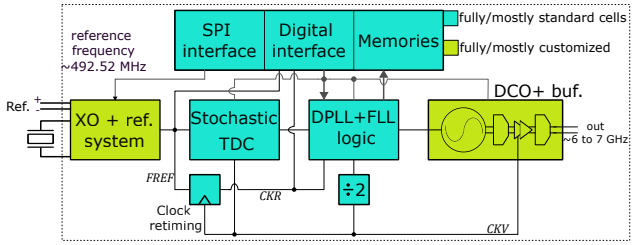

Fig. 2. Block diagram of the stochastic TDC based DPLL test chip.

all subTDCs operate in parallel the overall thermal noise level is scaled down with increased TDC resolution. For each subTDC, an $FREF_n$ signal is fed through a delay controlled by a random number generator (RNG), which reduces the effects of mismatch among subTDCs cells. The effective resolution becomes that of a subTDC delay cell divided by the number of parallel subTDCs, while randomization relaxes the mismatch issue. Another advantage of the proposed TDC is that during locking the subTDC delay lines can be configured to be in series for maximum TDC range. This allows for the TDC to be used in an FLL mode, eliminating the need for a dedicated FLL for frequency acquisition such as the high frequency counter in [3], see fig. 3.

There are two major sources of fractional spurs in a DPLL. The first and most problematic ones result from non-linearity of the TDC delay line due to PVT variations. Non-linearity of the TDC characteristic causes in-band low offset-frequency spurs as well as high offset-frequency spurs. The second source is due to the DCO clock (CKV) period not being equal to an integer number of TDC quantization steps, resulting in the phase wrap around being a fractional number of quantization steps. While this can be estimated and compensated, still due to quantization there will be a remaining periodic pattern that causes fractional PLL spurs. This is an issue even in ideal TDCs and can be mitigated by TDC resolution calibration, but that is not implemented in this work.

B. Butterfly-based shuffler

We propose a random time interleaving scheme which ensures that the reference signals to all subTDCs are spread equidistantly over at least one inverter delay time, see fig. 4. Every reference signal edge is in this way spread equidistantly to all subTDC channels, but which channel gets a certain time delay changes from one reference cycle to the next is in a random manner. It is then possible to eliminate the dead-zones and reduce spur levels, with a limited phase noise degradation. The proposed RNG uses a 4-layer butterfly shuffler that shuffles delay control inputs between subTDCs based on a pseudo-random sequence coming from a 32-bit linear feedback shift register (LFSR). Based on how many layers are operated, the randomness of the interleaving can be varied by activating different number of layers in the shuffler, allowing effects to be quantified by measurements including the no shuffling interleaved case.

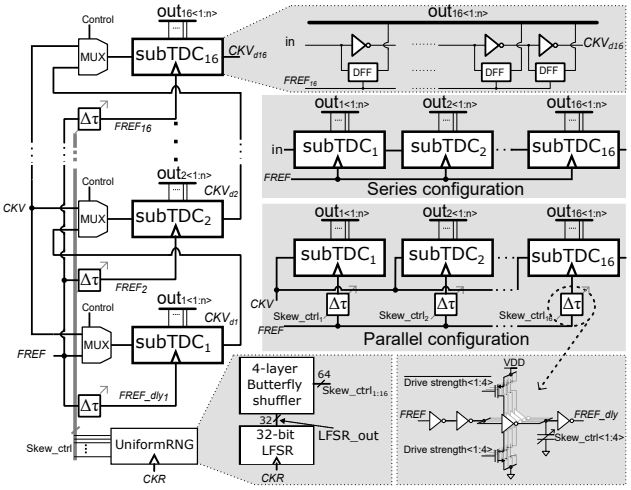

Fig. 3. Block diagram of the proposed multi-mode TDC.

C. Reference clock system

For the prototype PLL system, two multiplexed reference clock paths are available where one utilizes the latest advancements in crystal technology. A research prototype AT-cut quartz crystal with a nominal frequency of 983.04 MHz [4] used in a push-pull differential crystal oscillator (XO) [5] which is then co-integrated with the DPLL, where the frequency is divided by two. The second is an external reference clock path with a differential clock input terminated by 50 Ω on-chip.

Closer to the TDC, the time skew circuit is a digital-to-time converter (DTC). The time skew subsystem consists of 16 parallel time skew circuits, one for each subTDC. Each of these can delay an edge of the reference signal by one of 32 equidistant time delays, i.e. the delay can be $\tau_{min} + k\tau$, where k is an integer in the range 0 to 31, τ_{min} is the minimum delay and τ is a time constant. The LSB is not used thus the effective k range is 0 to 15, while τ has 16 different settings. The time skew circuit is implemented using four parallel binary weighted inverters. Digital control sets the range of the DTC. A tunable capacitor bank load is used to set the delay steps within the range, see fig. 3.

D. DCO design

The DCO core is a PMOS differential cross-coupled structure, with a two turn coil providing compact dimensions and an inductance of 340 pH with a quality factor (Q) of 15. The relatively low frequency enables use of thick oxide devices for the cross-coupled pair and fine tuning bank PMOS varactors, but the coarse tuning bank switches that carry most of the tank current to the MOM tuning capacitors use thin oxide NMOS devices for highest tank Q value. Both banks are unitary weighted and divided into rows and columns to reduce switching activity during locked state. The switches are dimensioned and biased such that they remain in the safe operating region, despite DCO negative peak voltages around -0.7 V with 0.8 V supply. Due to relatively high PLL bandwidth

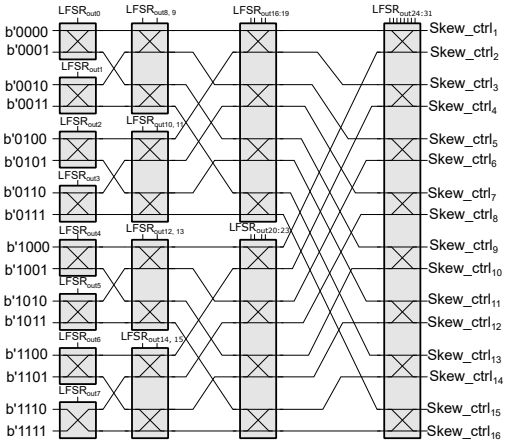

Fig. 4. Block diagram of the proposed 16-path 4-layer shuffler.

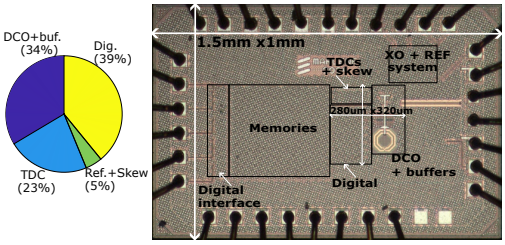

Fig. 5. Die micrograph and pie chart for the power consumption.

enabled by the low PLL in-band phase noise level and to minimize the DCO chip area no tail filtering was used.

III. Experimental Results

The proposed DPLL was implemented in a low power CMOS 22 nm FD-SOI technology. The chip size is 1.5 x 1 mm^2 and the DPLL core area is 280 x 320 um^2. The chip was wire-bonded to a PCB where the crystal was also soldered. Agilent 6700B DC power boxes were directly used to supply the DPLL subsystems resulting in supply spurs at low frequency offsets. A 491.5 MHz signal from an R&S SMA100B generator was used as an external reference. An FSWP analyser from R&S was used to measure phase noise. Multiple chips have been measured and similar results were obtained, results from one nominal chip are shown. The die micrograph together with the nominal power consumption pie chart are shown in fig. 5. The DCO consumes 16.6 mA from a 0.8 V supply and the TDC core consumes 12 mA from a 0.75 V supply, while the reference signal time skew consumes only 1.25 mA from 0.9 V. The digital part consumes 19.4 mA from a 0.8 V supply, which in addition to the DPLL part includes the consumption of the 16384 x 32 bit memories, the SPI, and the high speed digital interface. The reference buffers consume only 0.45 mA from a 1.4 V supply, and when the XO is enabled, including buffers it consumes 5.1 mA from 1.8 V or 2.1 mA from a lower 1.4 V supply.

The stand-alone XO measurements using a dedicated test buffer output show 12 fs RMS jitter integrated from 20 kHz to 10 MHz. As for the DCO, the measured 1/f^3 noise corner

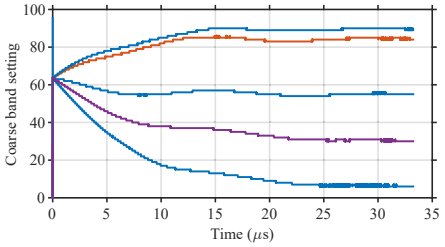

Fig. 6. Coarse bank tuning during FLL locking.

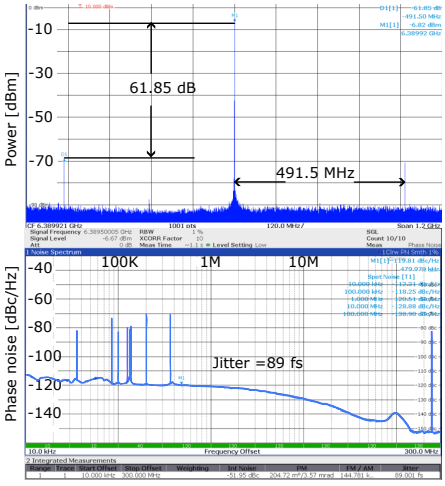

Fig. 7. Spectrum and phase noise measurements.

frequency is about 1 MHz, in line with the PLL bandwidth. The power consumption is 10.8 and 9.7 mW with corresponding FoM calculated for 10 MHz offset of -185.2 dB and -184.9 dB for lowest and highest frequencies respectively. The DCO frequency ranges from 6.0 to 7.1 GHz.

The measured coarse bank setting during FLL settling for different PLL frequency control word (FCW) values is shown in fig. 6. As can be seen in the figure the FLL settles gracefully in less than 25 μs. The spectrum and phase noise of the DPLL output for integer case FCW = 13 is shown in fig. 7. As can be seen in the figure the in-band phase noise level is $\sim$-120 dBc/Hz and the RMS jitter is 89 fs, while the reference spur is at -62 dBc.

To test the effectiveness of the stochastic TDC an FCW of 13+2^{-10} was applied and the raw phase error before subtracting from the reference phase or normalizing to the period was recorded into memories, see fig. 8. As can be seen in the figure, when the RNG is disabled the interleaving still improves the resolution, but repetitive patterns are visible in the ramp. Those patterns result in numerous low as well as high offset frequency spurs. For the stochastic case with the RNG enabled, on the other hand, the patterns are eliminated. With stochastic TDC a major source of spurs is thus eliminated and left are wrap around errors with some associated low offset frequency spurs.

An FCW of 13+2^{-2}+2^{-11} was then applied to test the TDC linearity, and the phase noise was measured for four cases, first non-random time interleaved TDC, second two shuffler

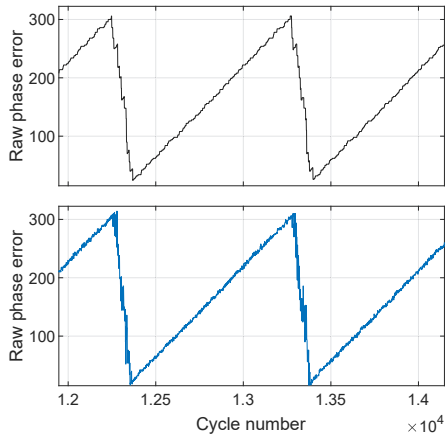

Fig. 8. Measured raw phase error when FCW is set to $13+2^{-10}$, (top) time interleaved and (bottom) stochastic TDC.

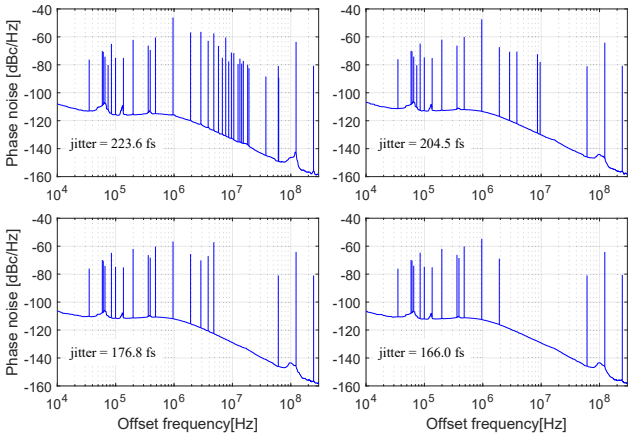

Fig. 9. Phase noise measurements with FCW=$13+2^{-2}+2^{-11}$ for (top-left) time interleaved TDCs , (top-right) stochastic two, (bottom-left) three and (bottom-right) four active layers.

layers activated, third three layers, and finally all four layers. The phase noise measurements are shown in fig. 9, where one can clearly see that most of the spurs are either reduced in amplitude or eliminated as the TDC linearity is improved by the stochastic time interleaving, and only wrap around and switched supply induced spurs are left. The worst case spur reduced from -46 dBc to -55 dBc.

A comparison to state-of-the-art DPLLs with linear phase detectors is shown in Table I. As can be seen the proposed work achieves very good performance excluding near integer case despite having power hungry test blocks included, such as the always on high-speed digital interface to memories. Furthermore, clock gating can be used to reduce the TDC power consumption to further improve the FoM. Ease of implementation, porting and reduced lead time are other benefits of this architecture.

IV. Conclusion

A novel parallel stochastic TDC architecture is presented, breaking the trade-off between circuit noise and quantization noise inherent in Vernier TDC architectures. In fact the circuit noise of the parallel TDC even reduces when the resolution is increased. A random time-interleaving method is used instead of dithering to improve TDC linearity with low in-band PLL noise penalty. Measurements show that the stochastic TDC effectively scrambles the periodic error resulting from TDC non-linearities, thus reducing both spur count and spurs levels. The TDC can also be reconfigured in series mode for use during frequency locking. A circuit has been fabricated in 22 nm FD-SOI CMOS technology, and compared to published DPLLs with linear detectors, the measurement results show state-of-the-art performance, indicating the potential of the new TDC architecture.

TABLE I
Performance comparison to DPLLs employing linear detectors

Parameter	This work	JSSC'25 [6]	TMTT'25 [7]	CICC'24 [8]	SSCL'20 [9]
Architecture	**Stochastic TDC**	Charge sharing	Reused TDC	SAR ADC	Ring osc. TDC
Tech. node [nm]	22	22	28	40	22
Reference freq. [MHz]	491.5	250	100	100	104
Freq. [GHz]	6-7.1	21-25	16.4-19.3	8-14	5.8-7.2
Area [mm^2]	0.09	0.08	0.11	0.32	-
Int. range [Hz]	10k-300M	1k-100M	1k-100M	10k-30M	10k-10M
RMS jitter [fs]	89$^\diamond$-166§	96-167	101-124	137-180	115$^\diamond$
Ref. spur [dBc]	-62$^\square$	-60	-70	57	-
Power [mW]	39.65$^\triangle$	13.81	14.83	17-21	31.1
FoM [dB] $\mathrm{dB}\left[\left(\frac{\sigma_t}{1s}\right)^2 \frac{P}{1mW}\right]$	-245, -240§	-249, -244	-248, -246	-245, -242	-243.9$^\diamond$

$^\diamond$Integer. §Excl. near integer case. $^\square$Worst case. $^\triangle$Inc. memories & high speed interface.

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