A 0.7mm x 14mm HV-CMOS ASIC for Intracerebral Electrodes Supporting 18-channel Stereo EEG Readout and Thermal Ablation Surgery

K. Badami[1], A. Sukumaran[1], T. Mavrogordatos[1], E. Azarkhish[1],
R. Cattenoz[1], J. Nagel[1], R. Ravanilla[1], J. Ruan[2], R. Kurtz[3], S. Emery[1]
[1]CSEM SA, Switzerland; [2]Aleva Neurotherapeutics, Switzerland; [3]Dixi Neurolab Inc., USA

***Abstract*—This work introduces a 0.7mm x 14mm needle-like ASIC for encapsulation within a 1.2mm diameter MEMS intracerebral electrode used for thermal ablation surgery in drug resistant epilepsy cases. The ASIC encapsulated electrode is designed for deep cerebral implantation up to 4 – 8 cm beneath the skull within the brain. The ASIC supports 18 channel high–impedance readout for stereo- electroencephalography to identify the epileptogenic–zone within the brain. Post epileptogenic–zone identification, the ASIC supports 5W of power delivery to thermally ablate the epileptogenic–zone. The ASIC is designed in 180nm HV CMOS process and the ASIC/MEMS-electrode assembly has been *in-vitro* validated for both 18-channel SEEG readout and thermal ablation.**

***Index Terms*—CMOS thermal-ablation, Epilepsy readout, High-impedance ExG readout,**

I. Introduction

Patient condition suffering from drug resistant epilepsy can be improved if the epileptogenic zone (EZ) within the brain is identified and subsequently ablated [1],[2]. Electro-corticography (ECoG) can be used to identify EZ, however, it needs a large craniotomy (see Fig. 1(a)) which can worsen the patient's morbidity [3]. Systems/ASICs with electrodes such as Utah array or Michigan probe [4]–[7] cannot be used to identify and/or ablate the EZ (Fig. 1(b),(c)), as the depth of these electrodes is sub-1cm and the required depth of EZ identification and subsequent ablation is 4 – 8cm underneath the skull [8]. Stereo-electroencephalography (SEEG) using intracerebral electrodes (Fig. 1(d)) is minimally invasive as it requires only Burr holes and enables 3D mapping of regions deep inside the brain to identify the EZ [2] and subsequently ablate it.

In the current SEEG standard of care, thin (< 1.2mm dia.) and long (typ. 20–35cm) intracerebral electrodes, shown in Fig. 2(a), are stereotactically implanted 4 – 8cm underneath the skull [8]. These electrodes are passive and have upto 18 contacts each and transmit sensitive analog SEEG signals over as many long cables to the recording station to identify EZ. Once EZ is identified, up to 5W of power is delivered to the EZ through the electrode to thermally ablate the EZ tissue [9].

ASIC integration within intracerebral electrodes as shown in Fig. 2(b)–(d) results in system-wide benefits: (1) signal digitization deep within the brain (4 – 8cm) within the brain

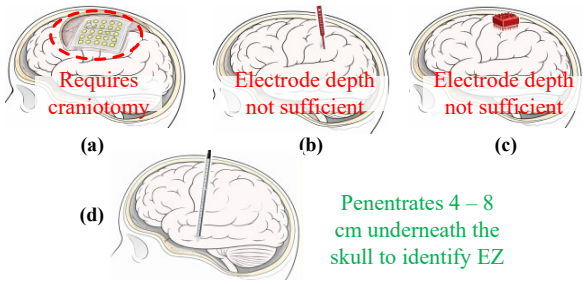

Fig. 1. (a) ECoG can be used to identify EZ but requires craniotomy (b) Utah array or (c) Michigan probe cannot be used to sense the EZ as the electrodes only support < 1cm penetration (d) Use of intracerebral electrodes to identify the EZ for drug resistant epilepsy surgeries

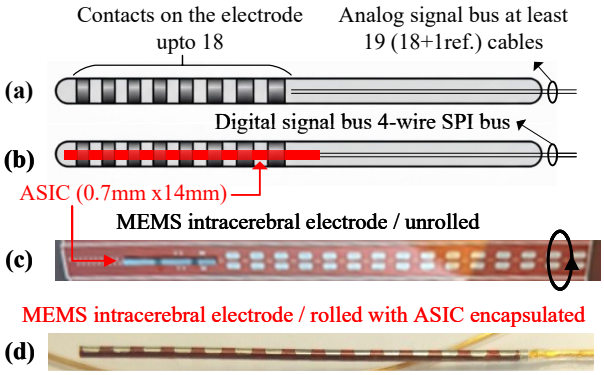

Fig. 2. (a) Schematic of passive intracerebral electrode (b) Schematic of ASIC encapsulated electrode (c) Thermo-compressive bonding of the ASIC with the electrode. The electrode is subsequently rolled around the ASIC. (d) ASIC integrated intracerebral electrode with diameter of 1.2mm

alleviates cable & motion artefacts (2) standard digital interfaces can transmit time multiplexed digitized SEEG to avoid per-channel cabling (3) ROM based electrode/contact data annotation avoids manual error prone labeling especially since upto 12 electrodes (with 18 contacts each) can be implanted for EZ identification in SEEG.

ASIC design for encapsulation within a 1.2mm intracerebral electrode for 18-channel SEEG readout while supporting 5W power delivery for thermal ablation requires several unconven-

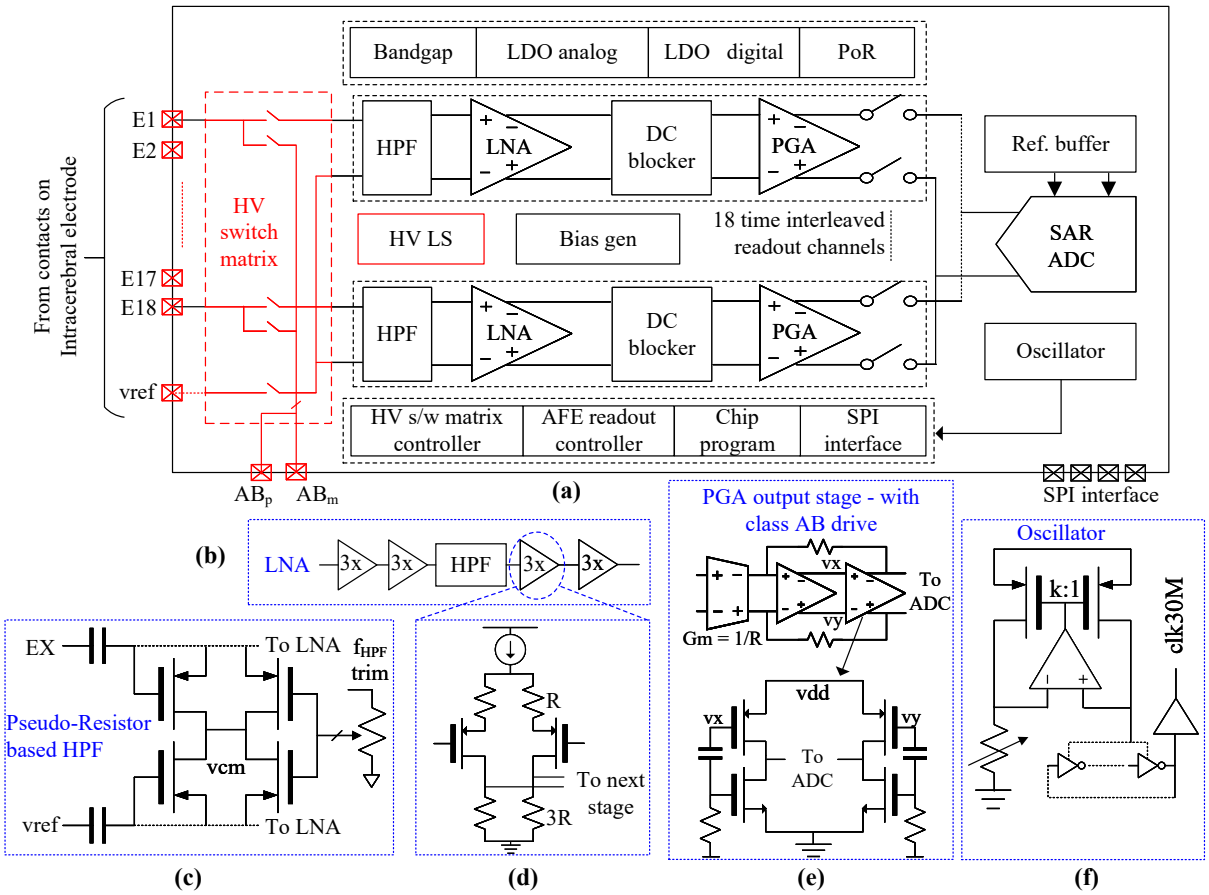

Fig. 3. (a) ASIC block-diagram depicting 18-channel SEEG readout chain for EZ identification and HV switch matrix (red) to support the thermal ablation of the EZ. (b),(c),(d) schematics for building blocks of HPF and the LNA (e) schematics of the PGA with class AB output stage (f) Schematics of the oscillator for timing and sequencing of the operations on chip.

tional design choices and is the subject of this work.

II. ASIC ARCHITECTURE AND DESIGN

This work introduces a 0.7mm × 14mm (20:1 aspect ratio) ASIC for integration within a MEMS based 1.2mm diameter intracerebral electrode and its block diagram is shown in Fig. 3(a). The ASIC width (0.7mm) is constrained by integration within 1.2mm diameter intracerebral electrode, while its length (14mm) is limited by the breakage risk resulting from unusual aspect ratio. The ASIC supports the 18-channel simultaneous SEEG readout + selectable thermal ablation of the EZ through the electrode contacts – E1–E18 as shown in Fig. 3(a). The ASIC integrates a full PMU, voltage/timing references and a digital controller for sequencing and programming its operation.

The signal flow through an SEEG readout channel is shown in Fig. 3(a). An upfront HPF is used to attenuate the electrode-drift enabling an up-to 25mHz HPF cutoff. The HPF is realized using a trimmable pseudo-resistor (PR) based passive RC as shown in Fig. 3(c). This results in a very linear HPF as the signal voltage across the PR is very small and is of the order of magnitude of the SEEG signal. The LNA provides a gain of 81× (∼38dB) in multiples of 3× (∼9.5dB) as shown in Fig. 3(b),(d). The LNA gain has been split over 4 stages to limit the passive area, effectively needing only 16R units as opposed to 82R units for single stage based gain. A degeneration resistor based amplifier (shown in Fig. 3(d) is used in the LNA as it has only two flicker noise inducing transistors, maintains robust PVT independent gain and also does not require additional circuitry for CMFB. Further this structure also offers very high input impedance in spite of a capacitive sensing interface due to absence of virtual ground at the amplifier input. Such a design choice minimizes the required area while enhancing the design robustness at the expense of power consumption. After the LNA, Gm-TIA based class-AB PGA (Fig. 3(e)) provides additional 16–22dB programmable gain to allow gain matching across the 18 channel and also drives a time multiplexed 2MSPS 10b SAR ADC. A 30MHz oscillator (Fig. 3(f)) supports timing of the ASIC.

Ablation of the EZ is supported by selectively delivering upto 5W via 64Vppkdiff / 200–500kHz sinusoids [9] between

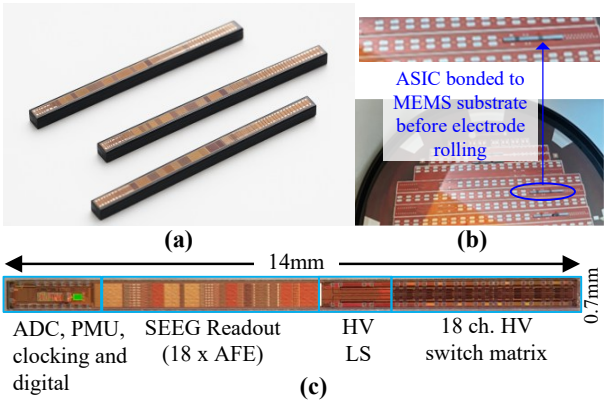

Fig. 4. (a) Die micrograph of the ASIC (b) ASIC bonding to the MEMS electrodes of different lengths (c) Different building highlighted on the ASIC

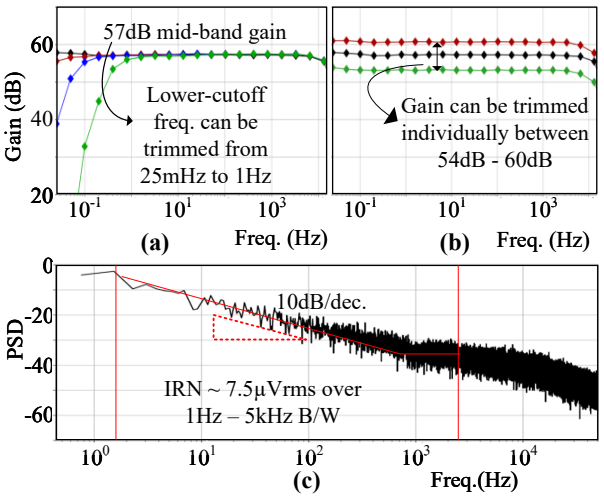

Fig. 5. Measured gain of an SEEG channel showing (a) lower cutoff trim (b) mid-band gain trim. The noise PSD shown in (c) illustrates flicker noise dominated IRN of 7.5μV$_{\text{rms}}$ over 5kHz bandwidth

ablation pads ABp/ABm shown in Fig. 3(a). The digital controller selects the power delivery location within the brain by selectively enabling electrode contacts between E1 to E18. The EZ has an estimated resistance of ∼100–200Ω when unheated and increases to >1000Ω as the tissue heats during ablation. The HV switches have been sized to have an $R_{\text{on}} < 20\Omega$ (while sustaining 64V breakdown in off state) to ensure >80% power delivery efficiency to the ablation tissue as a tradeoff between power delivery efficiency and HV switch area.

III. Measurements

The ASIC is designed in 180nm HV CMOS process and the die-micrograph is shown in Fig. 4(a) while the integration of the ASIC with the MEMS intracerebral electrodes is depicted in Fig. 4(b). ASIC building blocks are shown in the Fig. 4(c).

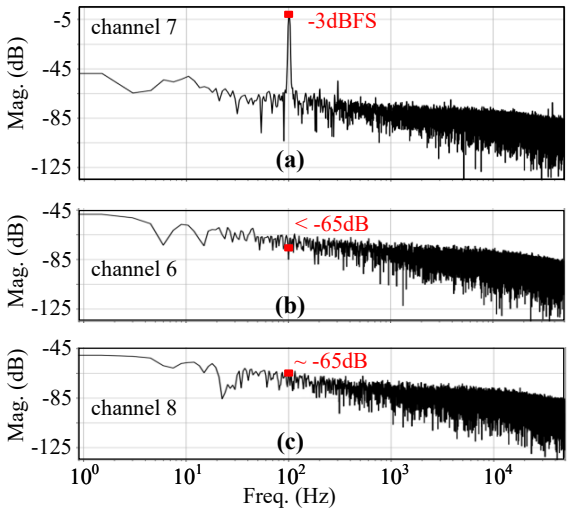

Fig. 6. Adjacent channel isolation measurements by (a) applying −3dB FS signal on channel 7 and measuring the outputs on adjacent (b) channel 6 and (c) channel 8. Measured isolation > 60dB

A. Electrical measurements

The measured signal gain from electrode input to the ADC output illustrating the trim of $f_{-3\text{dB,L}}$ from 25mHz to 1Hz and that of the mid-band gain between 54 – 60dB is shown in Fig. 5(a),(b) respectively. The noise spectral density for the complete channel is dominated by the $1/f$ noise and results in a an IRN of 7.5μV$_{\text{rms}}$ within 1Hz to 5kHz bandwidth. The noise PSD is shown in Fig. 5(c). As the ASIC width is highly constrained due to the requirement of integration within the MEMS intracerebral electrode, a very robust channel isolation is required to avoid crosstalk between adjacent channels. Channel isolation is measured by applying -3dBFS signal to channel 7 (see Fig 6(a)) while measuring its impact on adjacent channels 6 and 8. It can be seen from the measurements that robust >62dB isolation is measured on channel 6 and 8 as shown in the Fig. 6(b),(c). In-band CMRR is measured to be >75dB while offset for the 18 channels is within ±12 codes at the ADC output. Input impedance is estimated to be >1GΩ at 100Hz thanks to the pseudo-resistor based on chip HPF.

B. In-vitro measurements

Measurement setup for *in-vitro* readout based on combined ASIC electrode system is illustrated in Fig. 7(a). Gain error on simultaneous readout of all 18-channels is measured using a sinusoidal stimulus and is measured to be within ±1.2% as shown in Fig. 7(b). *in-vitro* measurements with emulated EEG signal on channel 5 and channel 1 w.r.t. to channel 3 are shown in Fig. 7(c). Measured on-resistance of HV thermal ablation switches is shown in the Fig. 8(a). Measurement setup for *in-vitro* validation of thermal ablation is illustrated in Fig. 8(b). Thermal ablation of the EZ is emulated by coagulating egg white with 5W power delivery between electrodes 2 and 3 and is illustrated in Fig. 8(c).

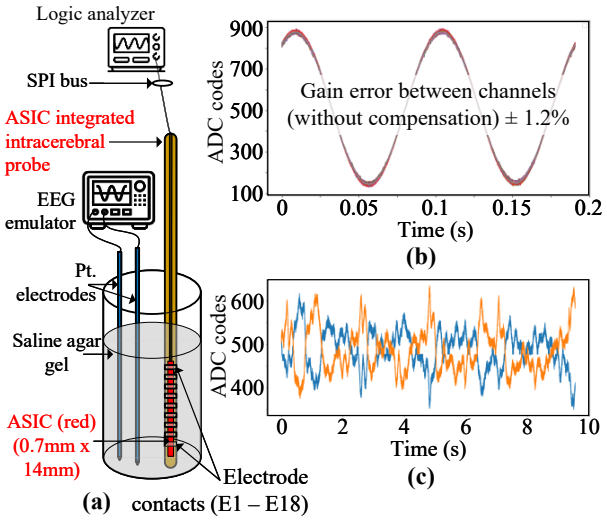

Fig. 7. (a) Scheme to show *in-vitro* meas. (b) Meas. -3dBFS sinusoidal readout on all 18 channel through a mock medium emulating conductivity of brain tissue. (c) Measured EEG signal (emulated) between channel 5/channel 3 and between channel 1/channel 3

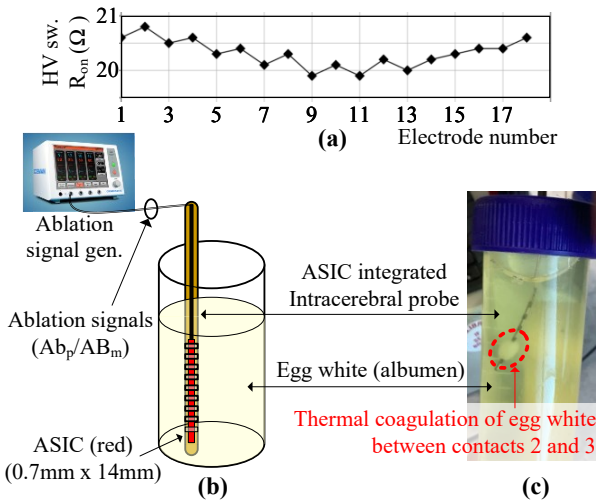

Fig. 8. (a) Measured on-resistance of the HV ablation switches. (b) Scheme to deliver up-to 5W power to ablate the identified EZ (c) *In-vitro* validation of the ablation power delivery, resulting in egg white coagulation between the selected electrodes 2/3

Comparison with state-of-the-art (SOTA) designs is shown in Table I. While most design metrics are comparable to SOTA benchmarks, the proposed ASIC prioritizes integration within an SEEG intracerebral electrode and robustness over ultra low-power optimization as these electrodes are intended for clinical bedside monitoring. Further, to the best of our knowledge, this is the first work demonstrating ASIC integration within SEEG depth electrodes, supporting multichannel SEEG readout and thermal ablation for epilepsy surgery.

TABLE I
COMPARISON OF NEURAL FRONT-END IMPLEMENTATIONS

Param.	**[4]**	**[5]**	**[7]**	**[6]**	**[10]#**	**[11]***	**This Work**
Tech.	55nm	130nm	180nm	65nm	22nm	180nm	180nm
Elec.	Michigan probe/similar			Neuralink	μECoG	Intracerebral elec.	
Z_{in} (Ω)	NA	NA	NA	92M	43M	80M	>1G
CMRR	NA	>70	>60	76	98	NA	>75
EDO (mV_{pp})	rail-to-rail	AC coup.	±60	110	160	AC coup.	rail-to-rail
THD (dB) @mV_{ppk}	−52 10	−48 10	−38 10	−44 NA	−53 2	NA NA	−54 4
IRN (μV_{rms})	7.58	10.3	9.21	6.8	3.98	10.6	7.5
BW (Hz)	1k	1k	10k	1k	500	10k	5k
P/ch (μW)	19.3	49.3	14.6	24	1.6	12	300
PEF	1640	7767	1832	1641	75	1995	4992

* Amp only. # Amp+ADC. PEF = $NEF^2 \cdot VDD$.

IV. CONCLUSION

This work demonstrates a highly integrated 0.7 mm × 14 mm HV CMOS ASIC for intracerebral electrodes, enabling combined SEEG recording and thermal ablation. Fabricated in 180 nm HV CMOS, the ASIC supports 18-channel low-noise SEEG acquisition and strong inter-channel isolation under severe geometric constraints. An integrated HV switch matrix enables selectable thermal ablation with up to 5 W delivered power. Benchtop and *in-vitro* measurements validate the system, representing, to the authors' knowledge, the first ASIC integrating SEEG readout and thermal ablation for drug-resistant epilepsy diagnosis and treatment.

REFERENCES

[1] H. Catenoix, *et al.*, "SEEG-guided thermocoagulations: A palliative treatment of nonoperable partial epilepsies," Neurology, vol. 71, no. 21, pp. 1719–1726, 2008.

[2] M. Cossu, *et al.*, "Stereo-EEG-guided radiofrequency thermocoagulation," vol. 58, Epilepsia, pp. 66–72, 2017.

[3] S. Kovac, V. N. Vakharia, C. Scott, and B. Diehl, "Invasive epilepsy surgery evaluation," *Seizure*, vol. 44, pp. 125–136, 2017.

[4] X. Yang et al., "A Highly-Integrated 1536-Channel Quad-Shank Monolithic Neural Probe in 55nm CMOS for Full-Band Raw-Signal Recording," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2024, pp. 1–2.

[5] C. M. Lopez et al., "A 966-electrode neural probe with 384 configurable channels in 0.13μm SOI CMOS," in *2016 IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, 2016, pp. 392–393.

[6] D.-Y. Yoon, *et al.*, "A 1024-Channel Simultaneous Recording Neural SoC with Stimulation and Real-Time Spike Detection," in *2021 Symposium on VLSI Circuits*, Kyoto, Japan, 2021, pp. 1–2.

[7] D. Wendler *et al.*, "A 0.0046-mm2 Two-Step Incremental Delta–Sigma Analog-to-Digital Converter Neuronal Recording Front End With 120-mVpp Offset Compensation," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 2, pp. 439-450, Feb. 2023,

[8] F. Cardinale, *et al.*, "Implantation of Stereoelectroencephalography Electrodes: A Systematic Review," *Journal of Clinical Neurophysiology*, vol. 33, no. 6, pp. 490–502, 2016.

[9] A. Vasquez, *et al.*, "Radiofrequency thermocoagulation in focal epilepsy: A retrospective cohort study," *Epilepsia Open*, vol. 10, no. 2, pp. 529–538, 2025.

[10] X. Huang *et al.*, "A 256-Channel Actively-Multiplexed μECoG Implant with Column-Parallel Incremental $\Delta\Sigma$ ADCs Employing Bulk-DACs in 22-nm FDSOI Technology," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 200–202.

[11] F. Pothof, *et al.*, "128-channel deep brain recording probe with heterogenously integrated analog CMOS readout for focal epilepsy localization," in *Proc. 18th Int. Conf. Solid-State Sens., Actuators, Microsyst. (TRANSDUCERS)*, 2015, pp. 1711–1714..