Reliability Assessment of hBN-Encapsulated TMD Devices: from FETs to Inverters

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***Abstract*—Two-dimensional (2D) semiconductors are promising channel materials for ultra-scaled logic applications. However, available prototypes suffer from severe instabilities that hinder the adoption of this technology. To overcome this, encapsulation of the channel with a hexagonal boron nitride (hBN) monolayer has been proposed. Here, we comprehensively evaluate the reliability of hBN encapsulated MoS_2 field-effect transistors (FETs) and depletion-load inverters. We choose experimental parameter ranges and variations with the aim of uncovering the physical mechanisms that govern the observed degradation. Our results provide insights that can help to improve the stability of future technologies based on 2D materials.**

***Index Terms*—2D materials, hexagonal boron nitride, encapsulation, hysteresis, bias temperature instability**

I. Introduction

As device miniaturization continues, the performance of traditional logic devices based on conventional semiconductors becomes increasingly constrained, either by the exacerbation of short-channel effects in field-effect transistors (FETs) when the channel thickness is not scaled accordingly, or by the associated mobility reduction when it is [1]. To overcome this inherent trade-off of bulk channels, two-dimensional (2D) materials that offer sizable carrier mobilities have attracted attention. Among them, transition-metal dichalcogenides (TMDs) offer suitable bandgaps and large effective masses, with molybdenum disulfide (MoS_2) being the most mature option for realizing n-channel FETs [2]. However, important limitations arise when using 2D materials. While their dangling-bond-free surfaces mitigate the mobility drop in atomic monolayer channels, the absence of covalent bonding at the oxide–channel interface leads to increased instability compared to the SiO_2/Si interface [3]. This instability typically originates from charge transfer to border traps in the gate stack and causes shifts in key device parameters (most notably the threshold voltage), thereby compromising the functionality and performance of the resulting logic circuits [4].

To mitigate the aforementioned instabilities, different gate stack concepts have been proposed to reduce charge trapping without compromising device performance. A promising approach involves the use of layered 2D dielectrics to reduce charge trap densities at the interfaces to the channel [5]. Here, hexagonal boron nitride (hBN) is the most ubiquitous; however, its low dielectric constant limits its use as the sole insulator in the gate stack in deeply scaled devices due to the expected high gate leakage [6]. However, recent studies propose the use of hBN layers to encapsulate the 2D semiconductor, thereby improving the interface quality and enhancing device stability at the expense of increased fabrication complexity [7]. To benchmark this approach, it is essential to quantify the detrimental instabilities, which can be observed in hysteresis and bias temperature instability (BTI) measurements where the gate voltage is varied, or under constant biasing, as in low-frequency noise measurements. In particular, the former are highly effective techniques for assessing device reliability [8]. However, inaccurate conclusions may be drawn if key experimental parameters are overlooked. For instance, while the time required to perform the up- and down-sweeps in hysteresis measurements is rarely reported, it has a considerable impact on the observed hysteresis [9].

In this work, a comprehensive reliability assessment of hBN-encapsulated MoS_2 FETs is presented, with hysteresis and BTI measurements providing complementary insights. Special emphasis is placed on analyzing multiple devices to capture variability in instability behavior, as well as on key measurement parameters, such as the sweep time and the drain voltage in hysteresis measurements. The analysis is extended to characterize depletion-load inverters based on these hBN-encapsulated FETs, enabling a straightforward evaluation of the reliability of this platform for highly scaled logic applications. Section II describes the device fabrication and analyzes the performance of the resulting FETs and inverters. Section III presents a comprehensive analysis of the hysteresis behavior of the fabricated devices, while Section IV focuses on BTI measurements.

II. Device Fabrication and Performance

The locally back-gated devices use a Ti/Au–Al_2O_3–(hBN)-MoS_2 gate stack and were fabricated following the approach in [10], with additional steps to enable hBN encapsulation for the encapsulated devices following the approach in [7]. Schematics of the cross-section for both devices are shown in Fig. 1a. FETs with different aspect ratios (W/L) and depletion-load inverters with varying driver-to-load ratios (W_d/W_l) were designed, as shown in the optical microscopy (OM) images in Fig. 1b and Fig. 1e, respectively.

The performance of the hBN-encapsulated FETs is summarized in Fig. 1c. The devices exhibit an excellent $I_{\mathsf{on}}/I_{\mathsf{off}}$ ratio and low gate leakage (I_{G}/A), with both metrics limited by the measurement resolution, making them well suited for low-power 2D electronics. However, other performance metrics such as the averaged subthreshold slope, SS, and the maximum current, I_{max}, show non-ideal values [11], with

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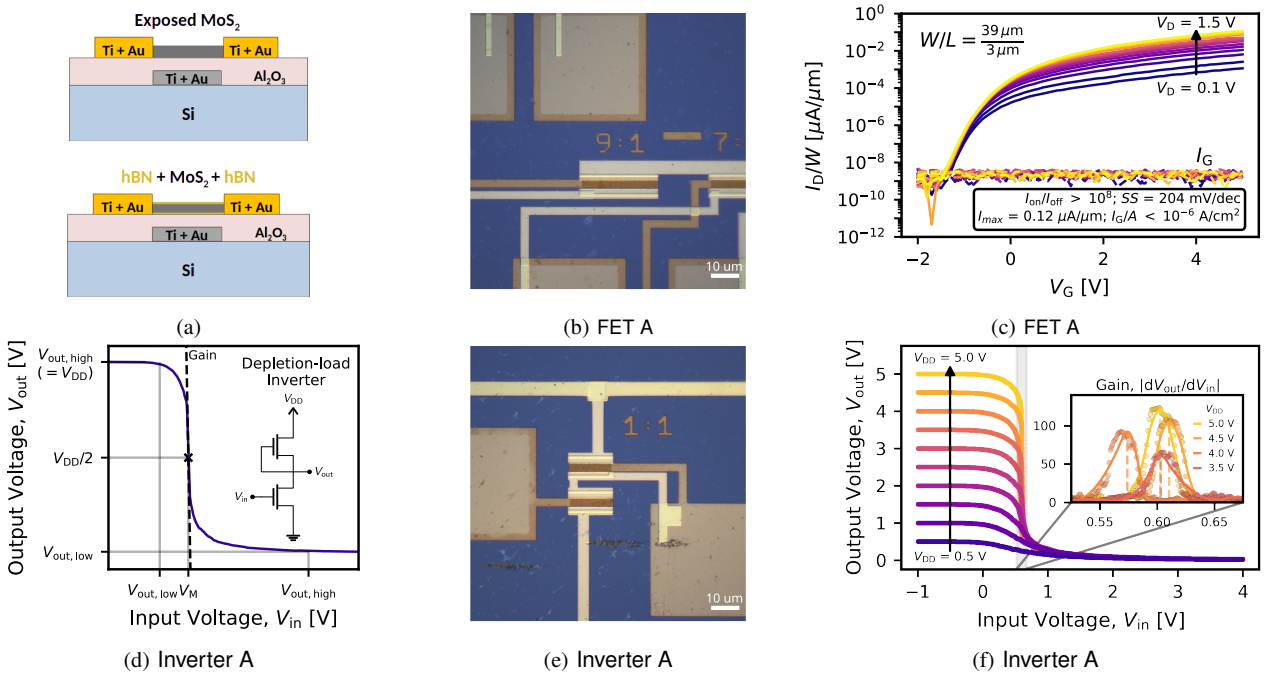


Fig. 1. (a) **Device cross-section:** Schematics of exposed (top) and hBN-encapsulated (bottom) MoS_2 FETs. (b) **FET OM:** Fabricated hBN-encapsulated FET. (c) **Performance of the fabricated FETs:** $I_{D(G)}$–V_G curves for different drain voltages and key device metrics extracted at V_D = 1.5 V. (d) **Inverter VTC:** Voltage transfer curve of a depletion-load nMOS inverter. V_M is defined as the input voltage at which the output equals $V_{DD}/2$. (e) **Inverter OM:** Fabricated hBN-encapsulated inverter. (f) **Inverter performance with V_{DD}:** Inverter VTC curves for different V_{DD} and the corresponding gain curves.

the latter likely being reduced by the contact resistances. All FET metrics were extracted at a drain voltage of 1.5 V. The schematic of a depletion-load inverter is shown in Fig. 1d, along with an experimental voltage transfer characteristic (VTC). As expected for a depletion-load design, the output high level, $V_{out,high}$, is equal to V_{DD}, whereas the output low level, $V_{out,low}$, may deviate from the ideal value of 0 V depending on the driver-to-load ratio and the threshold voltages of the transistors. The transition point between the high and low output levels, V_M, is defined for convenience as the input voltage at which the output equals half of the supply voltage, $V_{DD}/2$. In Fig. 1f, the performance of an inverter with a 1:1 driver-to-load ratio is shown for different V_{DD}. The inverter gain, defined as the magnitude of dV_{out}/dV_{in} and reflecting the steepness of the transition between high and low output levels, is plotted in the inset of this figure for higher V_{DD}, showing values approaching and even exceeding 100 depending on V_{DD}.

III. Hysteresis Characterization

Hysteresis measurements are a widely used method to benchmark the stability of FETs, as near-negligible hysteresis is a key prerequisite for reliable performance in digital applications. However, transistors based on 2D semiconductors such as MoS_2 FETs often exhibit excessive hysteresis, which can limit their practical use. Fig. 2a depicts a typical hysteresis curve in which the I_D–V_G characteristics corresponding to the up and down sweeps differ. This difference can be quantified through the hysteresis width, V_H, defined as the difference in the threshold voltage during the up and down sweeps, i.e., $V_{th,down} - V_{th,up}$[1]. Different techniques can be used to extract V_{th}; for simplicity, the constant-current (CC) criterion is adopted here. This method defines V_{th} as the gate voltage at which the drain current reaches a specified reference value, I_{th}. Typical values of I_{th} are on the order of $10^{-7}\,A \cdot W/L$ for bulk semiconductor devices, whereas lower values, around $10^{-9}\,A \cdot W/L$, are more appropriate for 2D devices and are used here. The total sweep time influences hysteresis, as shown in Fig. 2b, where $V_{th,up}$, $V_{th,down}$, and V_H are plotted versus the sweep frequency, $1/t_{sw}$, with measurements performed from high to low frequencies. For low frequencies, a drift of V_{th} toward more positive values and an increase in the hysteresis width are observed, in agreement with the behavior of n-channel FETs under positive BTI stress. However, at high frequencies, CCW hysteresis is observed, as indicated by negative values of V_H. This behavior is likely due to charge transport via mobile ions in the dielectric, as other sources of CCW hysteresis can be ruled out [9]. Besides the sweep time, the gate-voltage range, $V_{G,range} = [V_{min}, V_{max}]$, is also an important parameter, as it determines the average electric field applied to the gate stack and thus influences the extracted hysteresis, given the field dependence of most underlying physical processes. Another parameter that is often overlooked is the drain voltage, V_D. On one hand, as V_D determines the longitudinal electric field in the device, it must be small enough to avoid interface degradation due to hot-carrier effects (a phenomenon that is still not well understood

[1]Clockwise (CW) hysteresis leads to positive values of V_H in n-type FETs, whereas counter-clockwise (CCW) hysteresis to negative values.

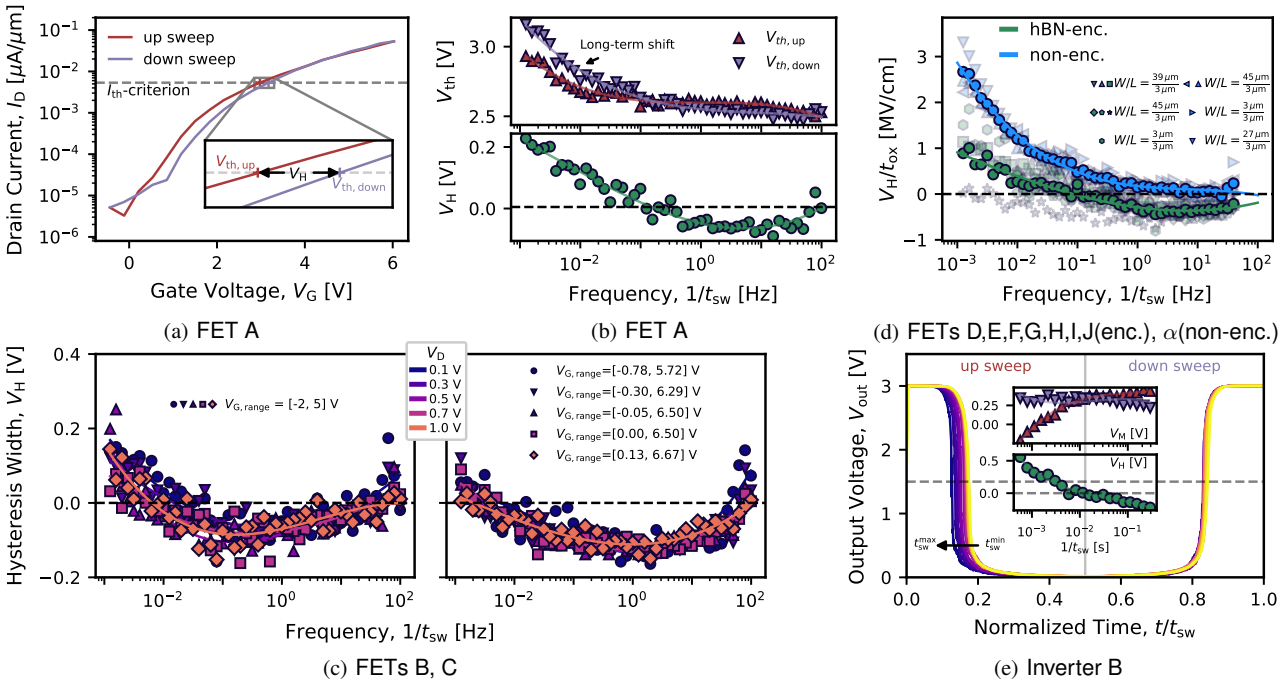
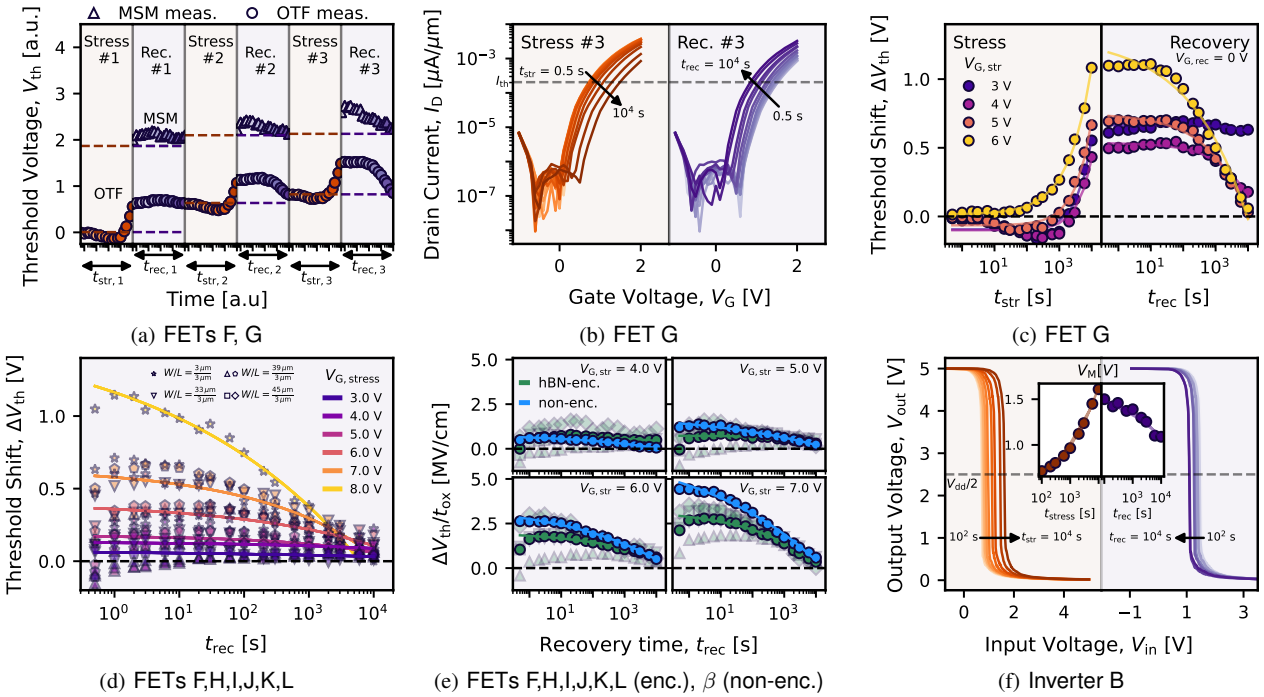


Fig. 2. (a) **Hysteresis curve**: the hysteresis width, V_H, is defined as $V_H = V_{th,down} - V_{th,up}$ evaluated at a CC criterion I_{th}. (b) **Hysteresis-$1/t_{sw}$ curves**: $V_{th,up}$, $V_{th,down}$, and V_H, are shown as a function of the sweep frequency, $1/t_{sw}$. (c) **Hysteresis for varying V_D**: The hysteresis is independent of the applied V_D. More consistent hysteresis results are obtained when using an adaptive scheme that targets the same overdrive (right), as compared to a fixed gate-voltage range (left). (d) **Hysteresis in encapsulated vs. non-encapsulated devices**: The hysteresis width in encapsulated devices is negative (counter-clockwise, CCW), whereas in non-encapsulated devices it was of a similar magnitude but positive (clockwise, CW) evaluated at V_D= 1 V. (e) **Hysteresis impact on inverter**: The hysteresis observed on an inverter shows a sizable hysteresis of V_M, approximately twice as large as on the FETs.

in 2D FETs). On the other hand, V_D may influence hysteresis measurements more subtly through its impact on the current in the on state when the hysteresis width is extracted using a CC criterion. Fig. 2c shows the impact of both $V_{G,range}$ and V_D on hysteresis. In the right plot, successive hysteresis measurements are carried out at different V_D while keeping $V_{G,range}$ constant on the same device. In contrast, in the left plot, the same procedure is repeated, but with $V_{G,range}$ adapted to account for the degradation in the previous measurements. As expected, better overlap between the different measurements is observed when the adaptive scheme is employed. In both cases, no dependence on V_D is observed, as expected. Fig. 2d provides a comparison of the hysteresis in hBN-encapsulated and non-encapsulated devices. The hysteresis is considerably reduced on the hBN-encapsulated devices, particularly for slow sweeps, while at fast sweeps a small CCW hysteresis is consistently observed on several devices. Hence, the hysteresis reduction in the hBN-encapsulated samples likely originates from an increased distance of the border traps in Al_2O_3 to the channel. The additional CCW hysteresis component may be linked to the additional fabrication steps associated with the encapsulation process.

IV. Bias Temperature Instability

Complementary to hysteresis, positive bias temperature instability (PBTI) measurements provide an additional means to assess device reliability. Since, in contrast to hysteresis, no sweep of the gate bias is involved, high biases can be applied over prolonged periods, thereby probing the long-term degradation. Fig. 3a depicts the two types of BTI experiments carried out in this work: on-the-fly (OTF) and measure-stress-measure (MSM). Both approaches employ alternating periods of stress (high positive gate bias, $V_{G,str}$) and recovery (subthreshold gate bias, $V_{G,relax}$) to analyze the degradation and subsequent recovery of the device characteristics over time. While in MSM experiments the device state is only assessed before and after the stress periods, OTF measurements monitor the device continuously throughout the entire experiment. If degradation and recovery primarily manifest as a shift in the transfer curve (as shown in Fig. 3b), V_{th} can be extracted using the CC criterion, and its difference with respect to the initial value, ΔV_{th}, can be used to monitor degradation. Fig. 3c shows an OTF PBTI measurement in which the stress bias is increased from 3 V to 6 V across successive stress–recovery periods. During the stress period, a negative shift of V_{th} is observed for times up to 10^3 s at the first three $V_{G,str}$ values. This negative contribution is in good agreement with the previously observed CCW hysteresis at high frequencies. The recovery measurements show that the induced degradation becomes increasingly recoverable as the stress voltage increases, being almost fully recoverable at the two highest voltages. Fig. 3d shows MSM results for different stress biases across devices. The average degradation at low $V_{G,str}$ is quite similar, with noticeable device-to-device variations. In Fig. 3e, a comparison of PBTI between hBN-encapsulated and non-encapsulated devices obtained through MSM measurements is presented. In



(a) FETs F, G (b) FET G (c) FET G

(d) FETs F,H,I,J,K,L (e) FETs F,H,I,J,K,L (enc.), β (non-enc.) (f) Inverter B

Fig. 3. (a) **BTI experiments**: Each point corresponds to the V_{th} extracted from an I_D–V_G at the corresponding time. The device state is only assessed during recovery in MSM measurements, whereas in OTF measurements, it is continuously monitored. (b) **Stress and recovery I_D–V_G curves**: The degradation manifests mainly as a V_{th} shift. A CC criterion, I_{th}, must be defined to extract V_{th}. (c) **OTF PBTI measurement**: An anomalous behavior (negative ΔV_{th} in PBTI for n-channel FETs) is observed at lower stress voltages and relatively short times. (d) **MSM PBTI measurements**: recovery curves after 100 s stress for six different devices, revealing high device-to-device variations. (e) **PBTI in encapsulated vs. non-encapsulated devices**: hBN encapsulation slightly improves resilience to PBTI stress, likely associated with the presence of an anomalous component. (f) **PBTI impact on inverter**: Applying a positive bias shifts the inverter transfer curve toward higher input voltages, increasing the transition point V_M.

general, the encapsulated devices exhibit greater tolerance to BTI degradation. However, this apparent robustness may be partly due to the previously observed negative contribution, resulting in an overall reduction in the measured shift. Finally, Fig. 3f shows the inverter behavior under PBTI stress and recovery periods. A shift of the inverter VTC toward more positive voltages is observed at a magnitude comparable to device-level PBTI.

V. Conclusions

The reliability of hBN-encapsulated MoS_2 devices and inverters is studied through a complementary hysteresis and PBTI analysis, with special attention to the choice of experimental parameters. The hysteresis reduction due to the hBN-encapsulation is sizable, even though the observed PBTI is similar, indicating that the hysteresis is dominated by border traps close to the interface. Moreover, encapsulated devices exhibit anomalous behavior, i.e., a negative threshold voltage shift, in both hysteresis and PBTI measurements. The origin of this anomalous behavior may be related to the additional fabrication steps involved in the encapsulation process, as none of the non-encapsulated devices show this effect. Although the negative contribution can partially compensate for the degradation induced, it is not an appropriate countermeasure, as it stems from an uncontrolled physical mechanism that may compromise device stability and requires further investigation.

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