Statistical study of HZO-based ferroelectric capacitive memories integrated in 22 nm FDSOI BEOL

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***Abstract*—This paper reports on a statistical study of the ferroelectric and capacitive memory characteristics of 7-nm thick $Hf_xZr_{1-x}O_2$ capacitors (FeCAPs) fabricated on 300 mm wafers, comparing standalone devices against integrated ones into the BEOL of a 22 nm FDSOI CMOS technology. Although remanent polarization values differ between standalone (25.7 µC/cm²) and integrated devices (8.5 µC/cm²), the Capacitive Memory Window at 0 V (CMW@0V) remains in the same range. Integrated devices, comprising 4092 FeCAPs connected in parallel, exhibit a CMW@0V of 0.083 µF/cm² (compared to 0.12 µF/cm² for 100 µm wide standalone) and a low wafer-level variation coefficient of 6.9%. Observations on spatial correlations between device performance and wafer position suggest that process-related material inhomogeneities may be responsible. Finally, we explore the analog synaptic capability of integrated FeCAPs through a multilevel programming scheme achieving up to 30 capacitance states.**

Keywords—ferroelectric, HZO, memcapacitors, 22 nm FDSOI

I. Introduction

The exponential growth of Artificial Intelligence (AI) workloads demands unprecedented energy efficiency at the edge [1]. Traditional von Neumann architectures face a "memory wall" due to costly data movement between memory and logic. In-Memory Computing (IMC) bypasses this by performing Vector-Matrix Multiplication (VMM) directly in memory. This paradigm shift required dense, low-power, CMOS-compatible non-volatile memory for synaptic weights. Among emerging NVM candidates, $Hf_xZr_{1-x}O_2$ (HZO) ferroelectric memories stand out for their proven scalability, high switching speed, and full compatibility with standard CMOS processes [2]. Conventional Ferroelectric Random Access Memory (FeRAM) read operations typically involve destructive polarization switching, necessitating a write-back after each read. This process not only degrades device endurance but is also incompatible with IMC and read-intensive AI inference tasks. To overcome these limitations, ferroelectric capacitive memories (memcapacitors) are being explored [3]. Operating the ferroelectric capacitors (FeCAP) below the coercive field indeed enables Non-Destructive Read-Out (NDRO) of capacitive states via Capacitance-Voltage curves [4], charge sensing [5] or nanosecond-scale transient current pulses [6]. Record Capacitive Memory Windows (CMW) reported so far rely on semiconductor-oxide stacks [9]. Parallelly, IMC architectures based on charge or voltage summation has been demonstrated [7], [8], addressing inherent scaling issues of memristor-based current summation. Despite these advances, most memcapacitor research remains at the device level, often using idealized standalone or RF test structures. There is thus a critical lack of statistical data regarding the performance variability at the industrial wafer scale. Crucially, the impact of integrating memcapacitors into the BEOL of advanced CMOS nodes on CMW and synaptic emulation remains unassessed.

In this paper, we report a statistical comparison of the ferroelectric switching and capacitive memory behavior of FeCAPs devices fabricated on 300 mm wafers, based on a TiN/HZO/TiN stack compatible with both FeRAM and memcapacitor applications. We contrast the performance of 300 standalone capacitors against 20 arrays of 4092 FeCAPs, fully integrated in the BEOL of a 22 nm FDSOI CMOS technology. Despite a lower remanent polarization (2Pr), we demonstrate that the integrated devices exhibit a functional CMW@0V of 0.083 µF/cm², comparable to their standalone counterparts (0.12 µF/cm²). The wafer-level uniformity remains in the same range, with variation coefficients of 6.9 % and 7.5 % for integrated and standalone FeCAPs respectively. Finally, we validate the potential of these integrated memcapacitors for analog IMC by demonstrating a multilevel capacitance programming protocol capable of achieving 30 distinct capacitance states.

II. Experiments

A. 300 mm manufacturing process flow

For this study, standalone and integrated FeCAPs were fabricated on 300 mm wafers following two parallel manufacturing process flows, as illustrated in Fig. 1. In both flows, the ferroelectric stack consists of a 7-nm-thick HZO layer deposited by ALD at 300°C, followed by a post-deposition anneal at 400°C for 1 hour. For standalone devices (Fig. 1(a)), a common bottom electrode was first realized by depositing 5 nm of Ti and 10 nm of TiN by PVD on n-doped Si wafers. CVD-deposited TiN/W top electrodes were patterned to define standalone capacitors with an area of 7852 µm² (100 µm diameter). Regarding the integrated FeCAPs, the process started above Metal 4 (M4) in the BEOL of 22 nm FDSOI [2](Fig. 1(b)). After the fabrication of a

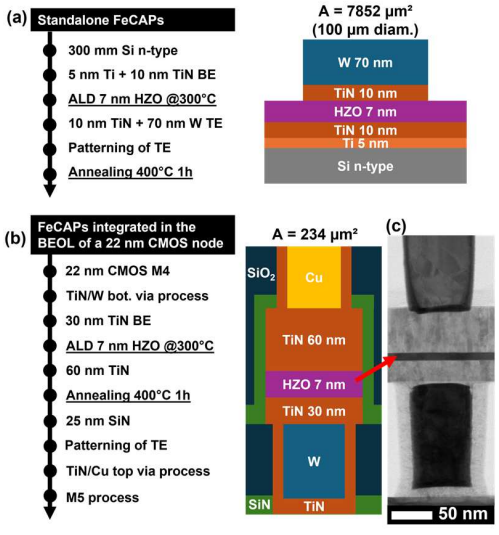

Fig. 1. Fabrication process flow on 300 mm wafers of (a) standalone FeCAPs with an area of 7852 µm² and (b) arrays of 4092 FeCAPs connected in parallel (total area = 234 µm²) integrated in the BEOL of a 22 nm CMOS FDSOI technology. (c) Cross-sectional TEM image of an individual FeCAP fabricated between M4 and M5.

TiN/W bottom via using a standard damascene process, the TiN/HZO/TiN stack was deposited by PVD and ALD, and patterned by plasma etching. Subsequent fabrication steps included the realization of a top via and Metal 5 (M5). The final integrated test structures consist of an array of 4092 FeCAPs connected in parallel, offering a total device area of 234 µm². Figure 1(c) shows a cross-sectional TEM image of one FeCAP within the array, where the HZO layer is indicated by a red arrow.

B. Ferroelectric and capacitive characteristics

A total of 300 standalone capacitors and 20 integrated devices (arrays) were tested. All electrical measurements were conducted at wafer level on a semi-automatic prober, using a Keysight B1530 for ferroelectric performance assessment and an LCR Meter for capacitance investigations.

1) Ferroelectric switching performance

Figure 2 compares the ferroelectric switching characteristics between the standalone and integrated devices. A wake-up protocol was performed using 10^4 triangular pulses of amplitude ±4 MV/cm at 100 kHz. The Polarization-Electric field (P-E) hysteresis loops (Fig. 2(a)), obtained with the Positive Up Negative Down (PUND) method at ±4 MV/cm and 10 kHz, reveal significant differences. Standalone FeCAPs exhibit a stronger ferroelectric response with a higher 2Pr after cycling, compared to the integrated devices where the loops are also shifted towards positive voltages. This behavior is analyzed further in the switching current density curves shown in Fig. 2(b). In the pristine state, standalone devices display double current peaks characteristic of antiferroelectric-like (AFE) behavior, which merge into a single sharp switching peak after cycling. This evolution suggests a field-induced reorganization of defects and stabilization of the orthorhombic phase for a more coherent ferroelectric response [10]. In contrast, the integrated FeCAPs exhibit a single, broader current density peak even in the pristine state. This peak shifts significantly during cycling while maintaining a consistent, albeit lower, magnitude. Although stress is not directly quantified here, the absence of AFE-like double switching peaks is consistent with a more stabilized orthorhombic phase induced by BEOL encapsulation.

A wake-up effect is observed in both device types, evidenced by the opening of hysteresis loops. This evolution is quantified in Fig. 2(c), where the 2Pr for standalone rises from 14 to 25.7 µC/cm² before stabilizing. Conversely, the integrated devices show a less important wake-up and a lower 2Pr value of approximately 8.5 µC/cm². This disparity in 2Pr may stem from mechanical stress induced by the electrode stack (TiN/W vs TiN/Cu) and BEOL interconnects [11]. Additionally, the asymmetry in the 2Pr loops of integrated devices may arise from their higher perimeter-to-area ratio, which could amplify sidewall etch damage and alter oxygen vacancy (VO) distribution. These defects could trap charges, leading to pinned ferroelectric domains partially switched during the wake-up phase [12]. The evolution of coercive voltages (V_C), shown in Fig. 2(d) highlights further these differences in switching behavior. Standalone FeCAPs exhibit a relatively symmetric decrease of V_C, stabilizing around 0.8 V and -1.0 V. However, integrated devices display a significant voltage shift during initial cycles, followed by progressive evolution during wake-up, eventually stabilizing at asymmetric values of approximately 0.5 V and -1.2 V.

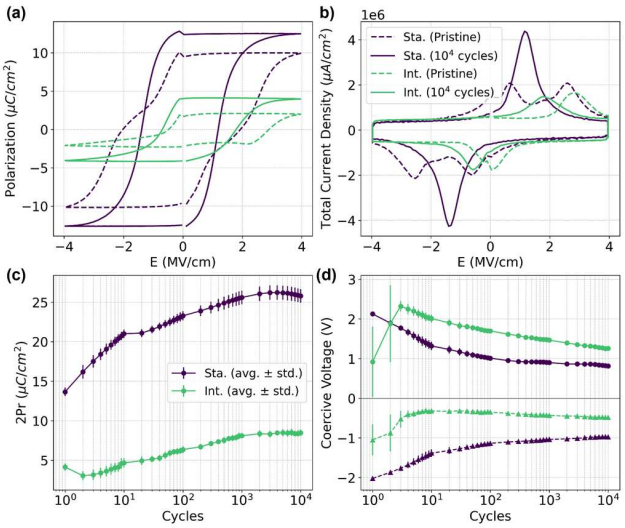

Fig. 2. Comparison of ferroelectric switching characteristics for standalone (purple) and integrated (green) FeCAPs. Data represent averages across all measured devices in the pristine state (dashed lines) and after 10^4 switching cycles (solid lines). (a) Polarization-Electric field (P-E) hysteresis loops and (b) corresponding total current density (J-E) curves. A wake-up effect is visible, evidenced by the broadening of the P-E loops and the shifting of the switching current peaks, (c) Evolution of 2Pr and (d) positive/negative coercive voltages (V_C) as a function of switching cycles, highlighting the wake-up kinetics and coercive voltage stabilization for both device types.

2) Wafer-scale ferroelectric and capacitive behavior

To assess the influence of process-induced inhomogeneities on device performance, we analyzed the spatial correlation between device position on the wafer and ferroelectric and capacitive switching variability. Figure 3(a) presents wafer maps of 2Pr values after wake-up for both device types. A wafer-scale radial inhomogeneity is visible in standalone devices. Higher 2Pr values are obtained at the center, while the highest values can be found at the bottom edge of the wafer. Figures 3(b) shows the wafer maps of the CMW@0V derived from the Capacitance-Voltage (C-V) curves of all standalone devices and integrated arrays (Fig. 3(c)). C-V measurements were conducted after wake-up, with a DC voltage sweep range of ±2.5 V and AC small signals at 10 kHz. Comparing the P-E (Fig. 3(a)) and C-V (Fig. 3(b)) wafer maps reveals a spatial anti-correlation between 2Pr and CMW@0V, specially for the standalone devices. The highest CMW@0V values are concentrated around the wafer center, where 2Pr is lowered. Conversely, the lowest CMW@0V values are found at the bottom edge of the wafer, coinciding with the highest 2Pr values. To better understand this behavior, we considered the pink-circled device. The corresponding P-E curves exhibit enhanced symmetry, facilitating ferroelectric domain reversal over the same voltage sweep range. The C-V curves (grey line in Fig. 3(c)) show the highest degree of symmetry and the largest capacitance range. Since the CMW is measured at 0 V, this symmetric polarization and C-V curves results in near-zero CMW. It was previously reported [13] that the asymmetry in C-V curves can be attributed to non-uniform VO distribution near one electrode, leading to polarity-dependent domain-wall vibration. Therefore, the variations in symmetry and range of the P-E and C-V curves

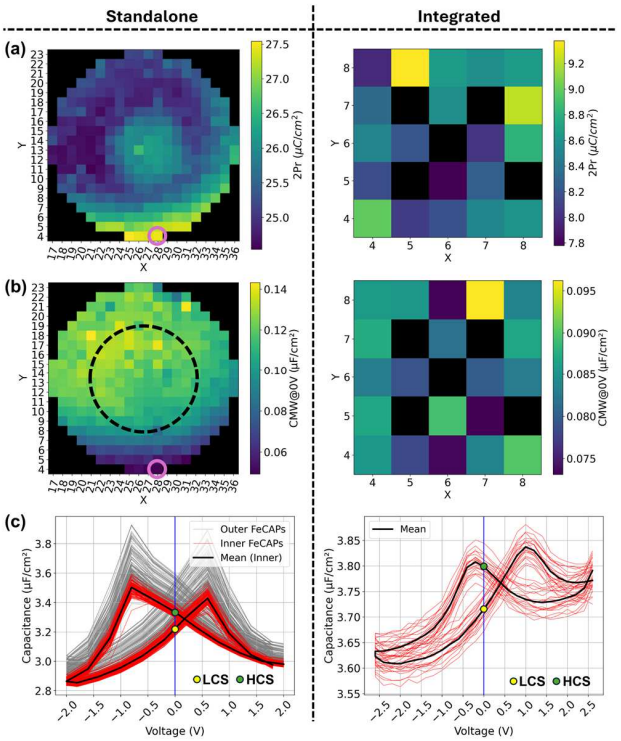

Fig. 3. Statistical distribution and capacitance characteristics of 300 standalone (left) and 20 integrated (right) FeCAPs. Black squares represent untested devices. (a) Wafer maps of 2Pr values, revealing a radial inhomogeneity in standalone devices. (b) Wafer maps of the CMW@0V, derived from the difference between the High Capacitance State (HCS) and Low Capacitance State (LCS) at 0 V in the (c) Capacitance-Voltage (C-V) butterfly loops. The thick black lines denote the mean behavior of the device ensembles. Standalone devices located outside the dashed radial boundary in (b) are plotted in grey (Outer FeCAPs) and exhibit higher peak capacitance with more symmetric loops. Devices located at the center of the wafer (Inner FeCAPs, 100 devices) are shown in red for both types of integration.

suggest the existence of wafer-level process non-uniformities (deposition, etch rate, annealing) impacting VO distribution, but also in layers thickness, number of pinned domains and stress effects in the interconnects suggested earlier.

While standalone FeCAPs P-E curves exhibit a slight negative voltage shift (Fig. 2(d)), the C-V data in Fig. 3(c) place the CMW@0V on the left of the butterfly curve, associated to a broader capacitance range in the left quadrant. For integrated FeCAPs, the shift of the V_C towards positive voltage values results in a corresponding C-V shift, with peak capacitance occurring in the positive quadrant. The opposite voltage shifts of P-E and C-V in standalone and integrated devices are consistent with different built-in fields arising from electrode/HZO interface quality and VO profiles, as shown in detailed small-signal studies of HZO capacitor [13], [14], [15]. In addition, different TiN qualities and exposure to hydrogen gas during CMOS integration may alter VO concentrations, fixed charge distributions and therefore internal electric fields [16]. Nevertheless, despite different 2Pr levels, both FeCAPs yield comparable CMW@0V. This occurs because the maximum CMW@0V is obtained when the steepest parts of the C-V branch align with 0 V, which depends not only on 2Pr but also on V_C and built-in fields.

The statistics of the Low Capacitance States (LCS), High Capacitance States (HCS), and CMW@0V of FeCAPs at the wafer center are represented in Fig. 4. Table 1 summarizes the statistical memory window performance, where the variation coefficient is calculated as mean divided by the

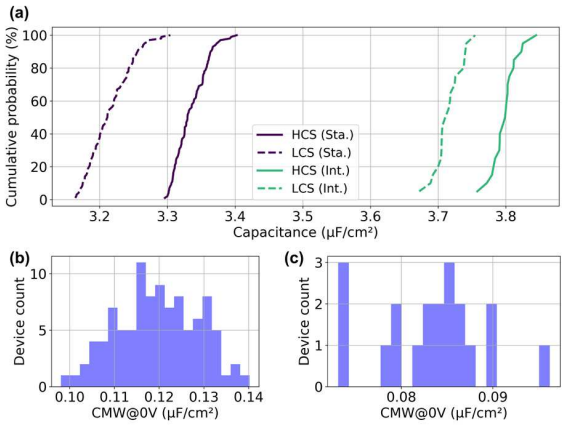

Fig. 4. Statistical distribution of capacitive states and memory window of 100 standalone FeCAPs (circled in Fig. 3(b), left) and 20 integrated FeCAP arrays. (a) Cumulative probability distributions of LCS (dotted lines) and HCS (solid lines) for standalone (purple) and integrated (green) FeCAPs. (Bottom) Histograms of the CMW@0V distribution for (b) standalone and (b) integrated devices.

TABLE 1. STATISTICAL RESULTS OF CAPACITIVE MEMORY WINDOW AT 0 V OF STANDALONE AND INTEGRATED FECAPS.

	Standalone	**Integrated**
Number of FeCAPs	100	20
Absolute CMW (pF)	9.4 ± 0.7	0.195 ± 0.013
Norm. CMW (μF/cm²)	0.12 ± 0.009	0.083 ± 0.006
CMW var. coeff. (μ/σ)	7.5 %	6.9 %
Mean CMW/LCS ratio	3.72 %	2.24 %

standard deviation of CMW@V extracted from Fig. 4(b) and 4(c). The Cumulative Distribution Function (CDF) of HCS and LCS in Fig. 4(a) shows that arrays of integrated FeCAP devices achieve higher capacitance density with tighter dispersion. The integrated structures exhibit a CMW@0V of 0.083 μF/cm² compared to 0.12 μF/cm² for standalone devices. These values are below the state-of-the-art [9], [17] achieved with semiconductor oxides (e.g. IGZO). However, our simplified TiN/HZO/TiN stack trades absolute CMW for maximal CMOS and FeRAM/memcapacitor co-integration flexibility. Regarding performance homogeneity, the coefficient of variation of integrated devices is around 6.9 %, which is lower than the 7.5 % of standalone capacitors. This variability could stem from all the sources of non-uniformity inferred in this study. It is important to note that while individual sub-micron device variability is expected to be higher than large capacitors, the parallel connection of 4092 FeCAPs effectively averages out device-to-device variations. The programing of multiple capacitance levels should now be explored to address the needs of efficient hardware neural network based on capacitive IMC architectures.

3) Multilevel capacitance programing and NDRO

Implementing analog synaptic weight storage for capacitive neural networks requires multilevel capacitance programing combined with NDRO. Therefore, we investigated the feasibility of programming and reading multiple discrete capacitance states on FeCAPS integrated on FDSOI technology. The results of a multilevel capacitance programming experiment conducted on an integrated FeCAP array are shown in Fig. 5. The incremental programming sequence detailed in Fig. 5(a) begins with a high-amplitude

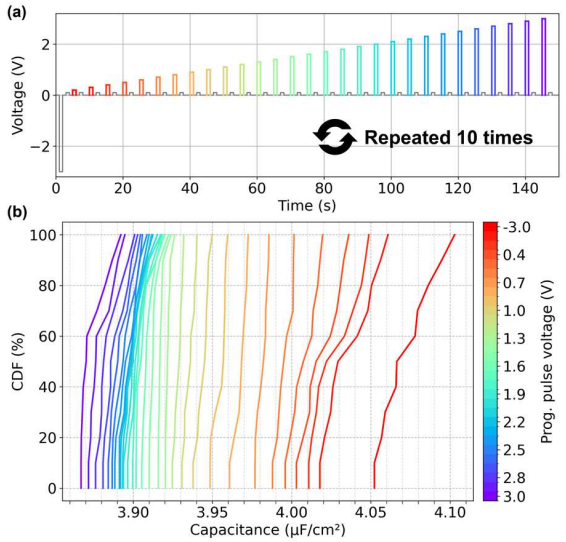

Fig. 5. Multilevel capacitance programing experiment on an integrated FeCAP array. (a) Schematic representation of the pulse sequence, starting with a high-amplitude RESET pulse at -3 V, followed by reading pulses (grey) at 0.1 V and incrementally increasing programming pulses (colored). This sequence was repeated 10 times to assess programming variability. (b) Cumulative distribution function of the 10 repetitions of multilevel programming.

negative RESET pulse of -3 V to initialize the device into a stable HCS. This is followed by a train of positive programming pulses with incrementally increasing amplitude (+0.1 V), interspersed with 0.1 V pulses to read the new capacitive state and emulate NDRO charge-domain inference. This entire sequence was repeated 10 times to assess programming variability.

As evidenced by the CDF in Fig. 5(b), distinct capacitive states are achieved with contained cycle-to-cycle variability, despite the use of an open-loop configuration (without read-write-verify feedback loop). We observe saturation and jump effects near LCS and HCS respectively, leading to local state compression, non-linear evolution and higher variability. This behavior could be attributed to variations in the dynamics of ferroelectric domain switching, leading to non-monotonic capacitance modulations in specific regions. The intermediate capacitance regime (3.92–3.98 µF/cm²) exhibits significantly lower variability and more uniform state distribution. Within this optimal window, FeCAPs demonstrate sufficient separability to support around 10 reproducible conductance states tuning. While up to 30 distinct levels can be plotted, reliable multi-bit operation would likely utilize a subset of these states and programing feedback loops to ensure adequate state distributions for IMC.

III. Conclusion

This paper reports a statistical investigation into the ferroelectric switching and capacitive memory characteristics of HZO-based FeCAPs, comparing standalone macro-devices against arrays fully integrated into the BEOL of 22 nm FDSOI technology. The integrated FeCAP arrays exhibit a capacitive memory window at 0 V of 0.083 µF/cm² (vs. 0.12 µF/cm² for standalone) with good wafer-level uniformity and low variation coefficient of 6.9 %. Finally, we demonstrated the capacitive synaptic potential of integrated devices via the programming of up to 30 capacitance states assessed by non-destructive readout. These results validate the viability of integrating HZO memcapacitors in advanced CMOS nodes for energy-efficient in-memory computing and FeRAM/memcapacitor co-integration opportunities.

Acknowledgment

This work was funded by European commission through ECSEL-IA 101007321 StorAIge project. We also acknowledge funding support from the European Research Council (consolidator grant DIVERSE: 101043854).

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