A 0.015mm^2 Fast-Startup Crystal Oscillator Using Periodically Calibrated, ΔΣ-Modulated Injection Achieving 14.5µs Startup Time for BLE Applications

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***Abstract*—This work presents a 16MHz fast-startup crystal oscillator (XO) in 65nm CMOS technology for Bluetooth Low Energy (BLE) using periodically calibrated, ΔΣ-modulated injection. It leverages the rapid wakeup demands in BLE advertising and keep-alive. The startup acceleration uses the crystal to calibrate the frequency control word of a 5-bit digitally controlled oscillator (DCO) before sleep, with ΔΣ-modulation for extra resolution. This enables accurate frequency injection upon wakeup. The circuit occupies only 0.015mm^2 in area and achieves 14.5µs startup time and 8.4nJ startup energy, outperforming prior art.**

***Keywords*—crystal oscillator (XO), fast startup, Bluetooth Low Energy (BLE), periodically calibrated injection, ΔΣ-modulation**

I. Introduction

Bluetooth Low Energy (BLE) is widely adopted as one of the backbone protocols for supporting short-range wireless connectivity in Internet of Things (IoT) applications. Such applications, like smart home appliances, wearable electronics, and location tracking tags, require periodic advertising from peripheral devices for fast device discovery and/or repetitive keep-alive signals to remain robustly addressable by the central device, as shown in Fig. 1 (a). Typical intervals for these wireless data exchanges range from 10ms-level to 10s-level (20ms to 10.24s for advertising, and 7.5ms to 4s for keep-alive [1], [2]), as a trade-off between user experience and battery life. On the circuit side, the BLE's RF transceiver can duty cycle the high-frequency crystal oscillator (HFXO), as these intervals are long enough that restarting every time would offer better energy efficiency. However, if built without dedicated startup assistance circuits, a long startup time can produce substantial wakeup latencies that offset the benefits in power saving and impact the user experience.

This work presents a ΔΣ-based frequency calibration and injection method to boost the HFXO's startup time by utilizing the information acquired during the previous operation phase. An accurate knowledge of the crystal's resonance frequency can enable optimal energization of the crystal by precisely tuning the injection frequency. Previous works that aim to reduce startup time commonly obtain this knowledge during the startup process, either by measuring it with the injection in action [3]–[5], which induces complex circuitry that comes with large area overheads, or through an injection-detection-calibration-injection sequence [6]–[8], in which the time-consuming detection and calibration limits the minimum startup latency that can be achieved. This work, on the other hand, explores the use of the BLE protocol's

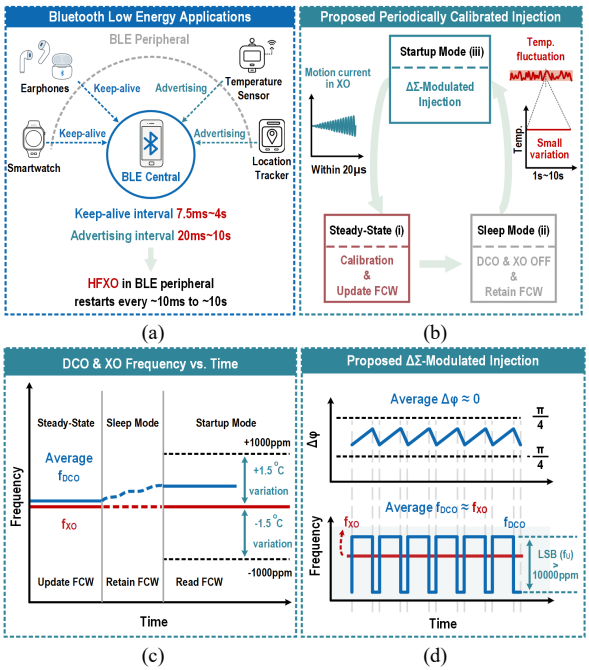

Fig. 1. The motivation (a) and an overview (b) of the proposed periodically calibrated strategy. The frequencies of DCO and XO versus time (c) and an overview of the proposed ΔΣ-modulated injection (d).

sub-10-second-level frequent wakeup demand for advertising and keep-alive to accelerate the crystal's startup process. As shown in Fig. 1 (b) and (c), before entering sleep mode, an on-chip calibration engine acquires the crystal's oscillation frequency and updates the frequency control word (FCW) registers. Upon waking up, the startup assistance circuit will use the retained FCW to inject a ΔΣ-modulated frequency signal through the on-chip digitally controlled oscillator (DCO). As shown in Fig. 1 (d), the ΔΣ modulation prevents phase error from accumulating beyond ±π/4 even when the DCO's LSB (f_U) is greater than 10,000ppm of the crystal's resonance frequency f_{XO}, which is critical for effective injection. A small temperature difference between rapid wakeup events and the ΔΣ injection technique, together, reduces the requirement for the DCO's dynamic range and temperature coefficient.

In commercial BLE products, a similar periodic calibration method has been commonly used, but only for the on-chip 32kHz RC real-time clocks (RTC), which require the HFXO to be turned on periodically at 1s [9] or upon the detection of temperature changes [10]. This work's calibration strategy can be naturally integrated with this process, reducing startup time to <16.8µs if temperature

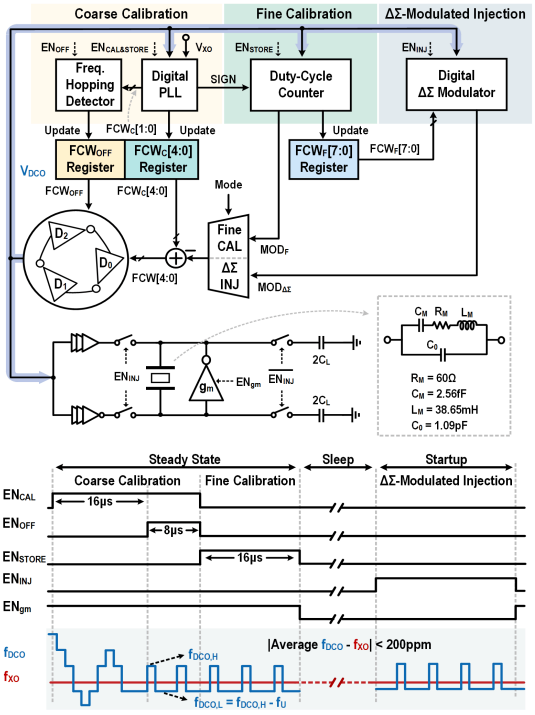

Fig. 2. Block diagram of the fast-startup HFXO and the top-level timing diagram for the DCO's output frequency and all the control signals.

changes are contained within ±1°C with only 0.015mm^2 of area overhead when implemented in a 65nm CMOS technology.

II. System-Level Implementation

Figure 2 illustrates the system-level implementation of the proposed fast-startup HFXO. The source of the injection signal is a 3-stage ring oscillator whose frequency is controlled by the 5-bit FCW[4:0] and a 1-bit offset signal FCW_{OFF}. The data used to generate FCW[4:0] is stored in two parts: an FCW_C[4:0] representing the coarse part of the digitized frequency, and an FCW_F[7:0] representing the fine part. The values of these two registers are updated after a two-step frequency calibration process before entering the sleep mode.

The first, or the coarse calibration step, uses a digital PLL (DPLL) to lock f_{DCO} to f_{XO} and updates FCW_C[4:0]. A frequency hopping detector (FHD) ensures f_{DCO} only hops between 2 values, $f_{DCO,H}$ and $f_{DCO,L}=f_{DCO,H}-f_U$, by asserting the FCW_{OFF} on demand, which is a prerequisite for moving to fine calibration. The coarse calibration allows the average value of f_{DCO} to converge to f_{XO} within ±200ppm in 24µs (16µs for DPLL to lock and 8µs for FHD to detect). During the second, or the fine calibration step, the circuit measures the ratio of $f_{DCO,L}$ in a total of 2^8=256 clock cycles (16µs) and uses the result to update FCW_F[7:0]. The two-step calibration strategy takes 40µs in total, which is identical to the time needed for an empty packet sent through a 2M PHY in BLE. The HFXO enters the sleep mode after the fine calibration concludes. Upon wakeup, the FCW[4:0] is computed by subtracting FCW_C[4:0] with $MOD_{\Delta\Sigma}$, a 1-bit correction signal generated by sending FCW_F[7:0] to a digital ΔΣ modulator. This aligns the average f_{DCO} with f_{XO}, only subject to the minor temperature-induced DCO frequency drift.

III. Circuit-Level Implementation

A. DPLL-based coarse calibration

Figure 3 shows the detailed schematic of the DPLL-based coarse calibration loop. The PFD and the TDC design are based mainly on the structure reported in [7], with the delay cells, τ_C, implemented using a 4-stage inverter chain. The delay cells are sized to ensure sufficient time range coverage over PVT corners. The TDC's output is then converted to a signed 4-bit binary format and sent through a digital LPF serving as the loop filter. The output of the digital LPF, FCW_C[4:0], is used to control the DCO unmodified, closing the loop. When the DPLL locks, the output of the DCO can be in one of the following two states.

1) In most cases, the DCO's output frequency will bounce between two adjacent values, which is desired and is compatible with the fine calibration circuit.

2) In rare cases when one of the DCO's possible output frequencies is very close to f_{XO}, the presence of noise may cause the DCO to hop between three different frequencies.

The FHD helps mitigate this situation by asserting FCW_{OFF} to downshift f_{DCO} by $f_U/3$ if it detects that the output frequency is hopping between three values. The FHD's function is realized by sampling FCW_C[1] one cycle after the rising and falling edges of FCW_C[0], respectively. If FCW_C[1:0] only takes 2 values, then all FCW_C[1] sampled after the rising edge of FCW_C[0] remain unchanged, and the same applies to those sampled after the falling edge. Hopping to a third frequency changes one of the latched values and is captured to assert FCW_{OFF}. Fig. 3 also shows the schematic of the tunable delay cells in the DCO. The delay is generated by a digitally controlled capacitor bank with C_U=7.2fF and a compound resistor (p-poly and n-poly with opposite temperature coefficients) for temperature compensation. One of the three delay cells has an extra C_U gated by FCW_{OFF}, which implements the aforementioned $f_U/3$ downshift on demand.

B. Fine calibration and ΔΣ-modulated injection

Figures 4 and 5 show the implementation of the fine calibration logic that records the ratio of $f_{DCO,L}$ in steady state, and the ΔΣ-modulated injection generator. To ensure that FCW_F[7:0] can be used to accurately recover the average frequency through ΔΣ modulation, it is critical to minimize the difference in the number of frequency transitions between fine calibration and ΔΣ recovery. This is because finite transition delays between $f_{DCO,H}$ and $f_{DCO,L}$ induce errors in the average frequency that can accumulate in time.

This work mitigates this issue by reducing the total number of frequency hops in the DCO in both fine calibration and injection. During fine calibration, frequency difference is tracked on every 8th cycle at the PFD's SIGN output using a finite-state machine. When detecting no flips in SIGN, its value in the 9th cycle is also monitored to invert MOD_F if necessary. In this way, the total number of frequency hops is capped at 32 in the 256-cycle fine calibration period while maintaining a full 8-bit resolution. In the digital ΔΣ modulator, frequency transition is limited by using an 8× slower clock, sacrificing the worst-case phase error to 0.22π during injection (simulated) as a trade-off, which is still within the π/4 boundary for startup acceleration.

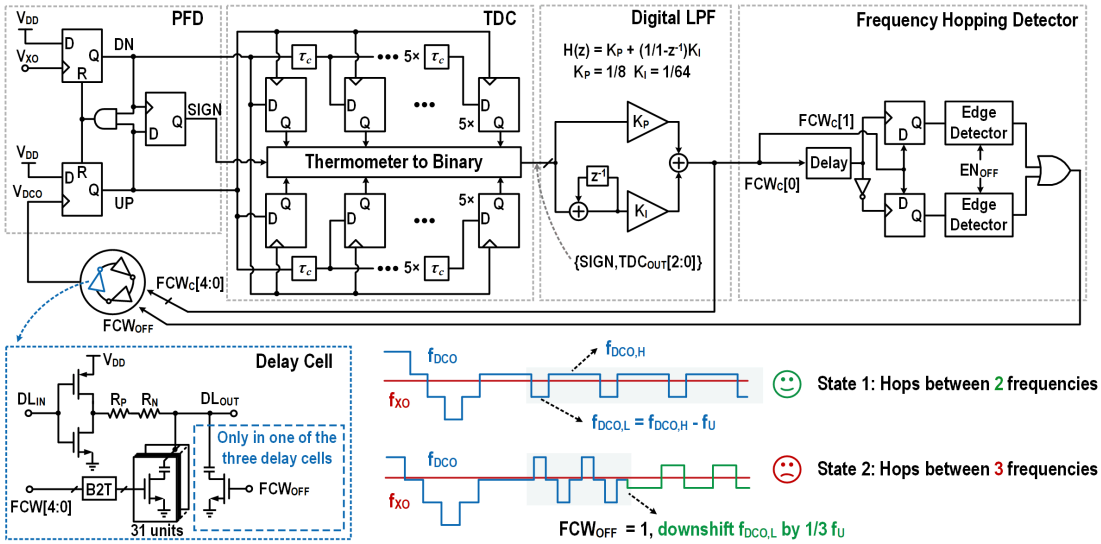

Fig. 3. The schematic of the coarse calibration circuits and the delay cell in the DCO.

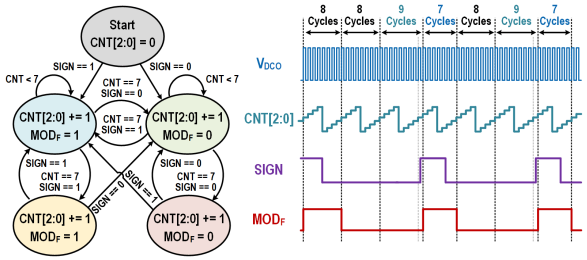

Fig. 4. State transition diagram of the fine calibration process with key waveforms.

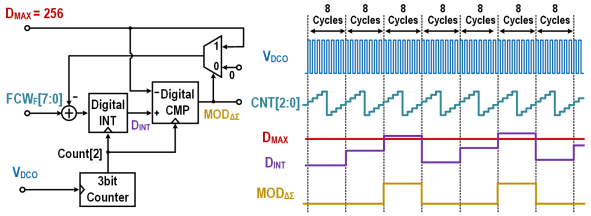

Fig. 5. Implementation of the ΔΣ-modulated injection circuits with key waveforms.

IV. Measurement Results

Fabricated in 65nm CMOS technology, the prototype fast startup HFXO circuit occupies an active area of 0.015mm^2. The annotated die photo is available as Fig. 6. Measurement results from 5 chips driving ESPON X1E0000210578 crystals are collected to evaluate the performance. Fig. 7 shows the captured transient waveform and its frequency over time from the XO's output. The average (worst) startup time is 14.5µs (15.0µs) or 232 cycles (240 cycles) at a stable 25°C. And the average (worst) startup energy is 8.4nJ (8.7nJ), including 2.4nJ (2.3nJ) spent on calibration. As shown in Fig. 8 (a), the startup time varies from 13.8µs (221 cycles) to 17.3µs (277 cycles) at constant temperatures ranging from -40°C to +85°C. And between 1.15 V and 1.25V of supply voltage, the startup time variation is within ±6.8% (Fig. 8 (b)). To evaluate degradation from abrupt temperature steps, chips slept at 25°C and woke up after thermal settling (Fig. 8 (c)). The worst-case startup is 16.8µs (269 cycles) within

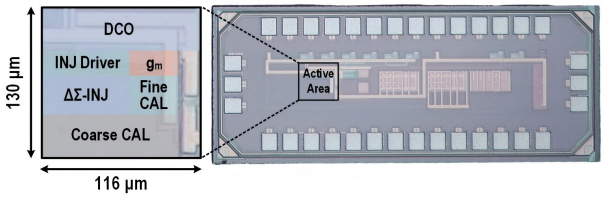

Fig. 6. Die photo, with a zoomed and annotated view of the core active circuits.

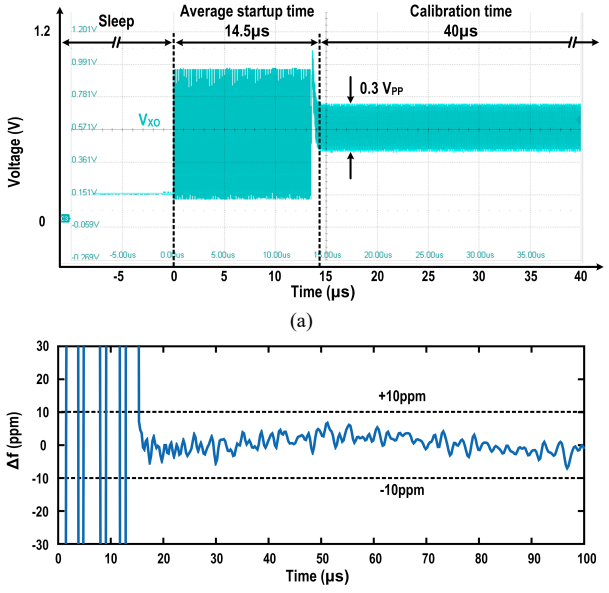

Fig. 7. Measured the time-domain waveform (a) and its frequency over time (b) at the XO's output.

±1°C steps, degrading to 22.3µs (357 cycles) at -1.5°C. The measured phase noise is -138.55dBc/Hz at 10kHz and -142.91dBc/Hz at 100kHz (Fig. 8 (d)), sufficient to meet the BLE's XO specifications in commercial products [11], [12].

Table I summarizes the performance of this fast startup HFXO using periodically calibrated ΔΣ-modulated injections and compares it with the state-of-the-art. Utilizing

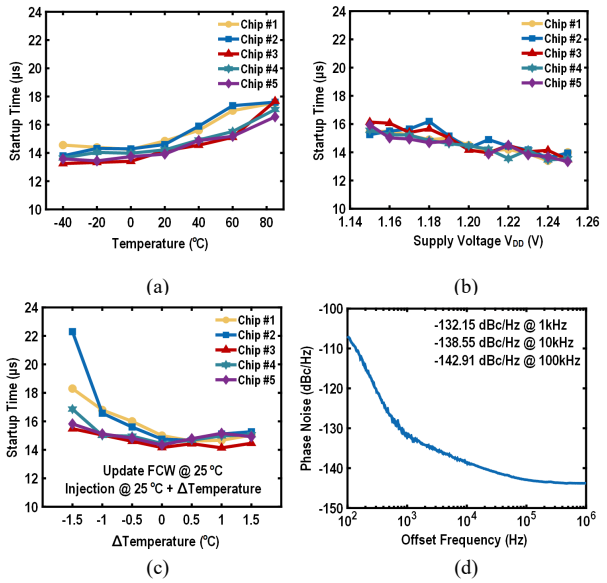

Fig. 8. Measured startup time across different temperatures (a), supply voltages (b), and temperature steps (c). And the measured phase noise at the steady state (d).

the demand for frequent wakeups in BLE applications, the proposed method reduces the total startup time to 14.5µs, which is the lowest among reported startup assistant circuits benchmarked using 16MHz crystals. In addition, the prototype circuit achieves the smallest area consumption compared to prior arts listed in Fig. 9, with its digital-intensive nature promising further area shrinking at more advanced processes.

V. Conclusion

This paper presents a fast-startup crystal oscillator using periodically calibrated, ΔΣ-modulated injection. Occupying an area of only 0.015mm^2, this design achieves a 14.5µs startup time and an 8.4nJ startup energy. These characteristics make the proposed calibrate-injection strategy a high-performing and affordable solution for fast startup HFXO in BLE applications, especially when integrated together with the existing periodic calibration for 32kHz RTC.

TABLE I. Comparison With State-of-the-art Works

	This Work	JSSC'21 [3]	JSSC'22 [4]	JSSC'24 [5]	JSSC'24 [6]	JSSC'24 [7]	VLSI'25 [8]	ISSCC'24 [13]
Technology [nm]	65	65	22	40	28	65	40	65
Supply voltage [V]	1.20	1.20	1.00	1.00	1.6/1.0	0.7	1.00	0.50
Frequency [MHz]	16	32	12	16	76.8	13.56	24	16
C_L [pF]	6	6	3.75	6	7	7	6	6
Single-ended steady-state Vpp [V]	0.30	0.13†	0.80	0.20	1.2	0.16	0.30	/
Startup time [µs]	**14.5**	7.20	340	17.5	39.6	45.8	6.90	120
Startup cycles	**232**	230	4080	280	3041	621	166	1920
Startup time over temperature	±11.3%	2.8%	±19.5%*	±4.5%	6.8%	±2.2%	±3.4%	±2.1%
Startup energy [nJ]	**8.4**	3.6	180.5	9.3	92.8	5.0	4.8	5.1
Temperature range [°C]	-40 to 85	-40 to 85	-40 to 80	-40 to 80	-20 to 85	-30 to 90	-40 to 85	-40 to 85	-40 to 85
Core area [mm²]	**0.015** (Core)	0.037# (Core)	0.070 (Core+C_L)	0.080 (Core)	2.580 (Core+C_L)	0.107# (Core)	0.119 (Core)	0.057 (Core)

† Obtained by halving the differential amplitude. * Calculated from reported data.
# Estimated from the die photos.

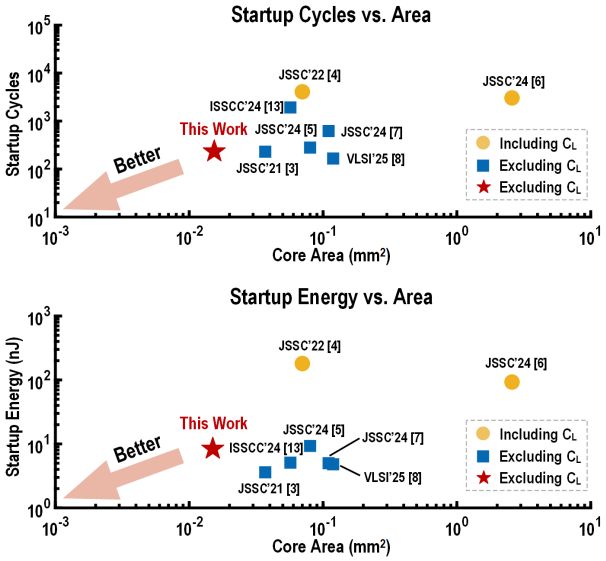

Fig. 9. Comparison with prior arts.

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