A 97.8%-Peak-Efficiency Single-Mode Three-Level Hybrid Buck-Boost Converter With Phase-Replica Adaptive Off-Time Control

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***Abstract*—This paper presents a single-mode three-level (SMTL) hybrid buck-boost converter which adopts four-phase operation to eliminate mode transitions. The average inductor current is equal to the load current by directly connecting the inductor to the output, thereby reducing the inductor DCR losses. Moreover, the continuous output current reduces the output voltage ripple and removes the right-half-plane zero. A phase-replica adaptive off-time (PRAFT) control scheme is introduced to enable precise output voltage regulation across different conversion ratios, thereby improving system stability and transient response. Fabricated in a 0.18-µm BCD process with a chip area of 2.52 mm², the SMTL converter maintains single-mode operation across the entire conversion range and achieves a peak efficiency of 97.8%. The measured response time is less than 20 µs when the load steps between 0.1 and 1 A, and the output voltage ripple is less than 0.5% of V_{OUT}.**

***Keywords*—buck-boost converter, continuous output current, phase-replica, right-half-plane zero, single-mode three-level**

I. Introduction

Modern mobile devices are usually powered by lithium-ion batteries. The voltage of a single-cell Li-ion battery ranges from 2.7 V to 4.2 V, spanning the typical regulated output voltage (e.g., 3.3 V) [1]-[2]. Buck-boost converters are therefore widely adopted to provide precise and stable output voltages across the entire battery operating range [3]. However, the growing complexity of deployment scenarios and increasingly stringent performance requirements of mobile devices impose critical demands on power converters. Specifically, buck-boost converters must achieve higher efficiency to prolong battery life, lower output voltage ripple to improve error vector magnitude (EVM), and faster transient response to support burst-mode communications such as orthogonal frequency-division multiple access (OFDMA) [4].

The conventional buck-boost converter (CBBC) operates in either four-phase (4P) or two-phase (2P) modes [5]-[6]. In 4P CBBC, mode transitions cause significant output voltage disturbance. The 2P CBBC suffers from discontinuous output current, which results in large output ripple. Moreover, the inductor current consistently exceeds the load current, resulting in unsatisfactory efficiency and power density. Additionally, the right-half-plane (RHP) zero in the CBBC topology restricts the loop bandwidth and impairs transient response performance [7].

A hybrid dual-C_F buck-or-boost (BoB) converter proposed in [8] eliminates the RHP zero in both buck and boost modes while delivering continuous output current to reduce output voltage ripple. In [9], a Li-ion-battery-voltage-profile-friendly BoB converter achieves optimized conduction losses in buck mode and unconditional RHP zero elimination. A three-level hybrid non-inverting buck-boost converter presented in [10] ensures RHP-zero-free operation and reduces inductor current based on buck-mode operation. However, all these converters rely on multi-mode operation and suffer from large output voltage disturbance during mode transitions.

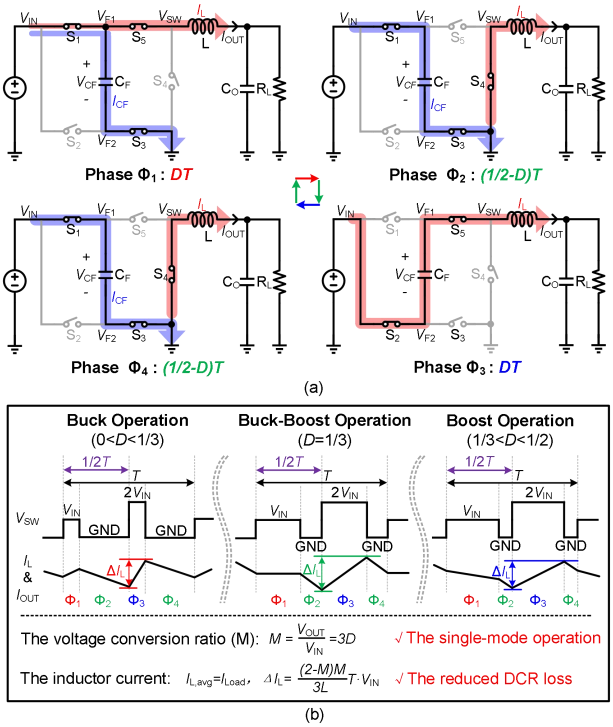

Fig. 1. The proposed SMTL buck-boost converter. (a) The operation phases. (b) The key waveform.

To eliminate mode transitions, several single-mode hybrid buck-boost topologies have been proposed. A bilaterally symmetrical hybrid buck-boost (BS-HBB) converter is introduced in [11], which improves power efficiency by reducing the inductor current and employing low-voltage CMOS switches. However, it suffers from discontinuous output current and an inherent RHP zero. In [12], a single-mode dual-path buck-boost converter (SDBBC) is proposed, achieving faster transient response and maintaining the inductor current consistently below the load current. Nevertheless, these benefits come at the cost of a larger number of power transistors and passive components.

II. The Proposed SMTL Buck-Boost Converter

A. Design Concepts and Operation Principle

To address the limitations mentioned above, a single-mode three-level (SMTL) hybrid buck-boost converter is

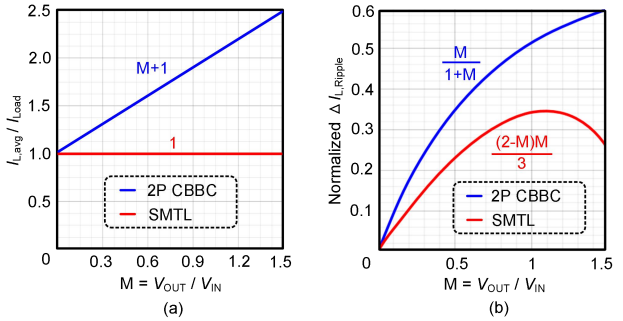

Fig. 2. (a) The comparison of average inductor current. (b) The comparison of inductor current ripple.

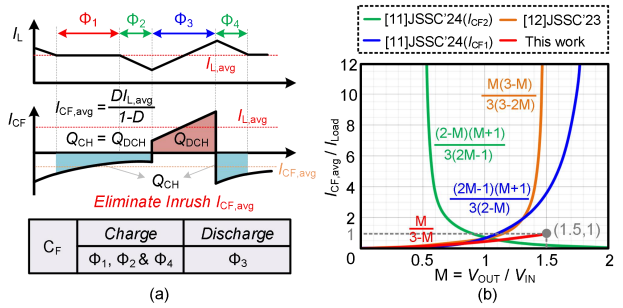

Fig. 3. (a) The waveform diagram and (b) comparison of flying capacitor current.

proposed in this work. The operating phases of SMTL converter are shown in Fig. 1(a), and the waveform of switching node V_{SW} and inductor current I_L are shown in Fig. 1(b). During Φ_1, I_L increases in buck operation, keeps constant in buck-boost operation and decreases in boost operation. In Φ_2 and Φ_4, I_L decreases, and in Φ_3, I_L increases. The duty cycle D is changed from 0 to 0.5. According to the principle of inductor volt-second balance, the voltage conversion ratio (VCR) can be expressed as

$$M = \frac{V_{OUT}}{V_{IN}} = 3D,\ (0 < D < 0.5) \tag{1}$$

Consequently, the SMTL converter enables both buck and boost operation across the full duty cycle range by using three-phase and single-mode, thus eliminating output voltage fluctuations caused by mode transitions.

B. The Inductor Current Analysis

Like the conventional buck converter, the average inductor current $I_{L,avg}$ of the proposed SMTL converter is equal to the load current I_{Load}. Fig. 2(a) shows the comparison results of the ratio of $I_{L,avg}$ to I_{Load} between the proposed SMTL and the single-mode CBBC. It is obvious that the proposed SMTL converter has a smaller inductor current DC value. It can be intuitively seen from Fig. 1(b) that the inductor current ripple $\triangle I_L$ is the largest under phase Φ_3. Under the same conditions of L, T, and V_{IN}, Fig. 2(b) demonstrates that the proposed SMTL converter significantly reduces the inductor current ripple across the entire conversion range compared with the single-mode CBBC. The DCR loss of the inductor is determined by both the DC component and the ripple of the inductor current. As a result, under the same inductor conditions, the SMTL converter exhibits lower DCR loss.

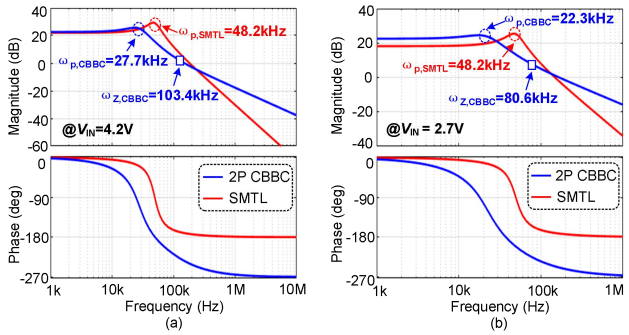

Fig. 4. The Bode plot of the SMTL converter and the 2P CBBC. (a) V_{IN} = 4.2 V. (b) V_{IN} = 2.7 V.

C. The Flying Capacitor Inrush Current

Most hybrid DC-DC converters suffer from flying capacitor inrush current issues under extreme duty cycle conditions [8]-[10]. The proposed SMTL converter effectively eliminates this issue. As shown in Fig. 3, C_F is charged during phases Φ_1, Φ_2 and Φ_4, and discharged only in Φ_3, the average discharging current is equal to $I_{L,avg}$. Since $0 < D < 0.5$, the average flying capacitor current $I_{CF,avg}$ is always less than I_{Load}. This inherent limitation of the flying capacitor current prevents large inrush currents, eliminating the need for power transistors to handle high current. Consequently, conduction losses and required silicon area are significantly reduced.

D. The Continuous Output Current

The continuity of the output current I_{OUT} significantly influences the output voltage ripple. In SMTL converter, the output current is continuous because the inductor is permanently connected to the output. This characteristic helps suppress voltage fluctuations caused by current changes across the parasitic elements (e.g., ESR and ESL) of the output capacitor. Consequently, the SMTL converter achieves a smaller output voltage ripple compared with the CBBC.

In addition, benefits from the continuous output current, the proposed SMTL converter features a faster transient response. The state-space averaging method is used to analyze the small-signal. The open-loop control-to-output transfer function G_{vd} is derived as

$$G_{vd} = \frac{V_{OUT}(s)}{D(s)}\Big|_{V_{IN}(s)=0} = \frac{3V_{IN}R_L}{s^2R_LC_OL + sL + R_L} \tag{2}$$

Fig. 4 shows the bode plots the proposed SMTL converter and the 2P CBBC under different input voltages, with V_{OUT} = 3.3 V, I_{Load} = 1 A, L = 4.7 µH, C_O = 2.2 µF and C_F = 10 µF. The SMTL converter has no RHP zero and exhibits good frequency-domain characteristics, which enhance transient response and system stability.

III. The Loop Control and Circuit Implementation

Conventional constant on-time (COT) control relies on converting a predictable inductor current ripple into an equivalent feedback voltage ripple. However, this approach fails for the proposed SMTL converter because the inductor current ripple varies across different operating modes. To

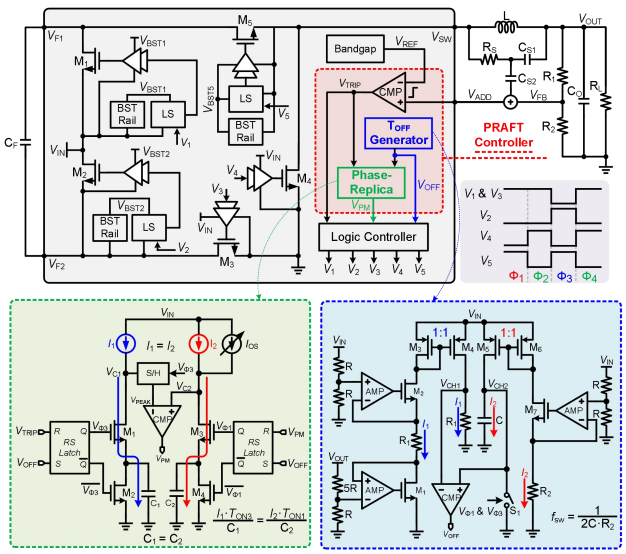

Fig. 5. The system architecture of the proposed SMTL buck-boost converter.

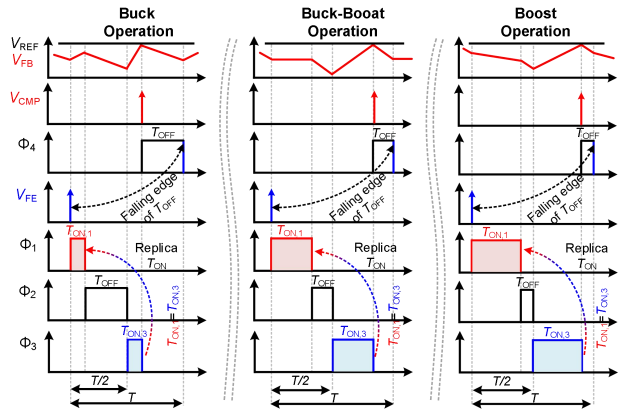

Fig. 6. The diagram of the proposed PRAFT control strategy.

address these limitations, a phase-replica adaptive off-time (PRAFT) control scheme is proposed.

The system architecture of the proposed SMTL converter is illustrated in Fig. 5. The phase-replica circuit, T_{OFF} generator, and comparator form the core of the proposed PRAFT control scheme. The phase-replica circuit mirrors and shifts the operating time of phase Φ_3 to phase Φ_1, ensuring both phases have equal durations. The T_{OFF} generator functions as a timer activated during phase Φ_2 and Φ_4, and it produces an adaptive off-time to ensure that switching frequency f_{SW} remains constant, independent of variations in V_{IN} and V_{OUT}. The logic controller generates switching signals V_1-V_5, which are processed by the level shifter, bootstrap circuit, and drivers to produce the gate drive signals for the power transistors.

Fig. 6 shows the diagram of the proposed PRAFT control strategy. During phase Φ_3, the inductor is magnetized. Once the ripple compensation signal V_{ADD} reaches the reference voltage V_{REF}, the comparator CMP outputs a high-level V_{TRIP} signal, triggering the transition to phase Φ_4. Subsequently, the adaptive T_{OFF} generator is activated and produces a high-level pulse V_{OFF} after the set T_{OFF} interval, initiating phase Φ_1. The phase-replica circuit then mirrors the duration of phase Φ_3 to phase Φ_1, ensuring equal operating times for both

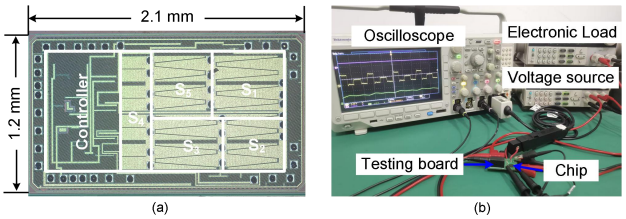

Fig. 7. (a) Chip micrograph and (b) measurement setup of the proposed SMTL converter.

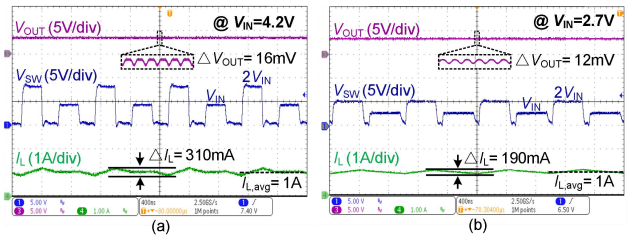

Fig. 8. The measured steady-state waveforms at different operation modes. (a) V_{IN} = 4.2 V and (b) V_{IN} = 2.7 V.

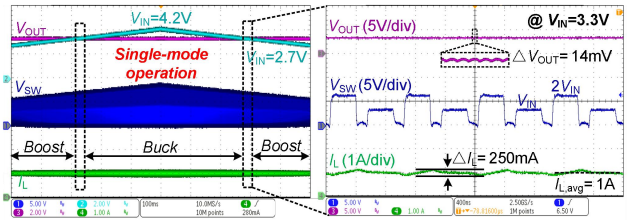

Fig. 9. The measured single-mode transition waveforms.

phases. Upon completion of this interval, a high-level pulse V_{PM} is generated to terminate phase Φ_1. As the converter enters phase Φ_2, the adaptive T_{OFF} generator starts again and outputs V_{OFF} after the T_{OFF} period, driving the system into phase Φ_3. This sequence repeats periodically, maintaining continuous cycling operation.

IV. Measurement Results

The proposed SMTL converter is fabricated with a 0.18-μm BCD process. Fig. 7 shows the chip micrograph and the measurement setup, the total chip area is 1.2×2.1 mm^2. With an input voltage V_{IN} ranging from 2.7 V to 4.2 V, the converter delivers a regulated output voltage V_{OUT} of 3.3 V.

Fig. 8 shows the steady-state waveforms of the SMTL converter. Under the buck operation (V_{IN} = 4.2 V), the inductor current ripple $\triangle I_L$ and the output voltage ripple $\triangle V_{OUT}$ are 310 mA and 16 mV, respectively. Under the boost operation (V_{IN} = 2.7 V), the corresponding ripples are 190 mA and 12 mV. In both cases, the average inductor current $I_{L,AVG}$ equals the load current.

Fig. 9 illustrates the seamless mode transition as V_{IN} varies between 2.7 V and 4.2 V. The V_{SW} waveform demonstrates a smooth transition between buck and boost operation, while the output voltage has no disturbance. When V_{IN} is approximated to 3.3 V, the measured $\triangle I_L$ and $\triangle V_{OUT}$ are 250 mA and 14 mV, respectively.

The load transient response is shown in Fig. 10. In buck operation, for a load step between 100 mA and 1 A, the

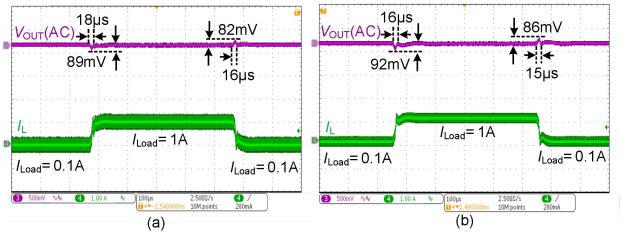

Fig. 10. The measured load transient waveforms at different operation modes. (a) V_{IN} = 4.2 V and (b) V_{IN} = 2.7 V.

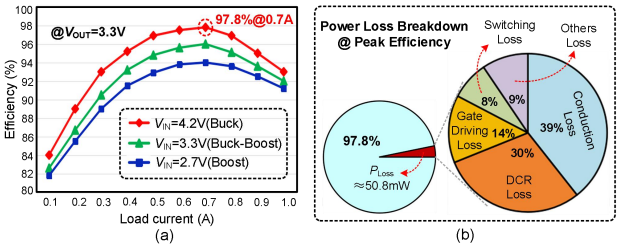

Fig. 11. (a) The measured power efficiencies. (b) The power loss breakdown.

TABLE I. COMPARISON WITH STATE-OF-THE-ARTS

	ISSCC' 24[8]	CICC' 25 [9]	JSSC' 25[10]	JSSC' 24[11]	JSSC' 23[12]	This work
Process (µm)	0.18	0.18	0.18	0.18	0.18	0.18
Topology	Dual-C_F BoB	BoB	3FLBB	BS-HBB	SDBBC	SMTL
Operation Mode	Multi-Mode	Multi-Mode	Multi-Mode	Single-Mode	Single-Mode	Single-Mode
f_{SW} (MHz)	2	1	2	1	1	1
C_F (µF)	4.7	10	10*2	10*2	10*2	10
C_{OUT} (µF)	1	10	10	10	4.7	2.2
L (µH)	1.2	2.2	2.2	4.7	4.7	4.7
Continuous I_{OUT}	Yes	No	Yes	No	No	Yes
Inrush I_{CF}	Yes	Yes	Yes	Yes	Yes	No
RHP Zero Free	Yes	Yes	Yes	No	Yes	Yes
Peak Efficiency	97.3%	98.5%	98.2%	96.9%	95.58%	97.8%

observed undershoot and overshoot voltages are 89 mV and 82 mV, with recovery times of 18 µs and 16 µs, respectively. In boost operation under the same load step, the corresponding undershoot and overshoot are 92 mV and 86 mV, with recovery times of 16 µs and 15 µs, respectively. This excellent transient response is achieved due to the elimination of the RHP zero.

The measured efficiency of the SMTL converter at V_{IN} = 2.7 V, 3.3 V, and 4.2 V under various load conditions is shown in Fig. 11(a). A peak efficiency of 97.8% is achieved in buck-boost operation at a load current of 0.7 A. Fig. 11(b) depicts the power loss breakdown at peak efficiency.

Table I summarizes the performance of the proposed SMTL converter against state-of-the-art buck-boost converters. Owing to its single-mode operation and continuous output current, the proposed converter achieves high peak efficiency, low output voltage ripple, and fast transient response.

V. CONCLUSION

In this paper, a single-mode three-level buck-boost converter is proposed suitable for mobile devices powered by single lithium-ion battery. Benefiting from the inductor connected to the output, the converter achieves lower inductor DCR loss, improved output current continuity, and elimination of the RHP zero. Moreover, by extending the charging phase of the flying capacitor, the converter mitigates the inrush current issue under extreme duty cycle. A phase-replica adaptive off-time control scheme is also introduced to achieve accurate output voltage regulation across different conversion modes.

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