A 10∼500 MHz Cryo-CMOS Noise-Canceling LNA Achieving 3.4-K Noise Temperature for Dispersive Readout of Spin Qubits

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***Abstract*— Spin qubits integrated with CMOS technology possess the potential for scalable quantum computing, while the fidelity of dispersive reflectometry readout is limited by the noise temperature of cryo-CMOS LNA. Currently, cryo-CMOS LNAs operating at 10∼500 MHz for spin qubits readout face the challenges of achieving low noise and low DC power consumption. To solve these issues, this paper presents a 28 nm cryo-CMOS 10∼500 MHz noise-canceling LNA. To minimize the Fano factor of shot noise, the input stage employs a cascode inverter with an optimized gate length of L=100 nm, which also significantly enhances the RF gain without additional DC power consumption. To boost the transconductance efficiency (g_m^2/I_D) for the thermal noise reduction, an NMOS gate width of W=400 μm with a current density of I_D/W=5∼10 μA/μm is adopted. Furthermore, a noise-canceling stage is used to suppress the channel noise current of the input stage. A Miller capacitor compensates for the phase difference between the input and noise-canceling stages, which improves the effectiveness of noise elimination at 300∼500 MHz band. Measured at 4.2 K, the LNA exhibits a peak gain of 35 dB and a noise temperature (T_e) of 3.4∼5 K within 10 to 500 MHz, while consuming 8.5 mW of DC power.**

***Keywords*— Cryogenic CMOS, low-noise amplifier (LNA), noise-canceling, spin qubit readout, quantum computing.**

I. Introduction

Quantum computing has emerged as a critical research frontier, offering the potential to surpass classical computing in fields such as factorization [1], database searching [2], and quantum simulation [3]. Among various physical qubit types, silicon-based spin qubits are uniquely positioned for large-scale scalability, leveraging their superior compatibility with silicon CMOS processes. This compatibility further enables the monolithic co-integration of qubits and their associated interface circuits within the cryogenic temperature range from 20 mK to 4 K. Dispersive reflectometry for spin-qubit readout typically operates in the 10∼500 MHz frequency range. However, the readout fidelity of spin qubits is strictly limited by the noise temperature of the LNA, as illustrated in Fig. 1.

Previously, cryogenic LNAs have been predominantly implemented using InP HEMT or SiGe HBT technologies, exploiting their superior carrier mobility and ultra-low noise at 4.2 K. A 0.1∼8.8 GHz SiGe BiCMOS LNA [4] achieves a min. T_e=4.0 K at 3.5 GHz, but presenting a T_e=5∼8 K within 10∼500 MHz. A 0.1∼3 GHz SiGe HBT LNA [5] achieves a min. T_e=4.0 K at 1 GHz, but T_e=5∼14 K within 10∼500 MHz. In recent years, cryo-CMOS LNAs [6]–[12] operating within ∼3 GHz widely adopt the noise-canceling technology [13]. A 160-nm CMOS 0.1∼0.5 GHz LNA [7] achieves a T_e of

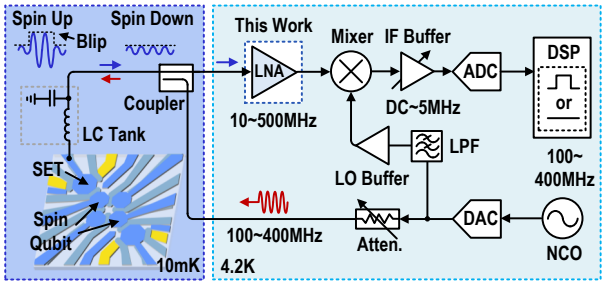


Fig. 1. Schematic of dispersive reflectometry for silicon spin qubits.

7∼36.6 K, while consuming a high DC power of 54.9 mW. The 22 nm FinFET 0.1∼0.6 GHz LNA only consumes 1.4 mW of DC power, but presents a high T_e of 44.4 K [6]. A 0.01∼3 GHz noise-canceling LNA achieves a min. T_e=2.2 K at 1.8 GHz, but its noise within 10∼500 MHz is only T_e=41.6∼60.7 K [9]. Another noise-canceling cryo-CMOS LNA reports a min. T_e of 6.9 K at 0.6 GHz [10] with P_{DC}=8.6 mW. Alternatively, utilizing the passive gain of the switched capacitor, a Cryo-CMOS receiver for spin qubit readout [14] achieves T_{noise} of 15 K at 1.2 GHz.

So far, the cryogenic LNAs within 10∼500 MHz still present unsatisfactory noise performance for the dispersive readout of spin qubits. This work presents a 28 nm cryo-CMOS LNA at 4.2 K, achieving a noise temperature below 5 K within 10∼500 MHz. For the higher transconductance efficiency, the input stage of LNA features an optimized device sizing and current density to suppress shot noise. Noise-canceling technology is also implemented for further channel noise reduction of the input stage. The cascode inverting configuration significantly enhances the RF gain. Furthermore, the LNA features an ultra-compact core area of only 0.012 mm^2, making it highly suitable for large-scale quantum integration.

II. Architecture of Noise-Canceling LNA

Fig. 2 illustrates the schematic of the proposed cryo-CMOS LNA, featuring a cascode inverting input stage designed to concurrently achieve high transconductance efficiency and substantial RF gain. To mitigate the noise contributions of the input stage, a noise-canceling (NC) stage employing a similar cascode inverting topology is integrated to suppress the channel noise components, $\overline{i_p^2}$ and $\overline{i_n^2}$, originating from the input transistors M_1 and M_4. Both the input and NC stages

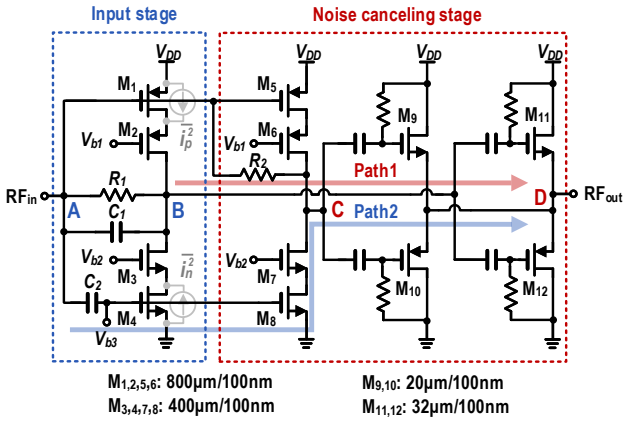
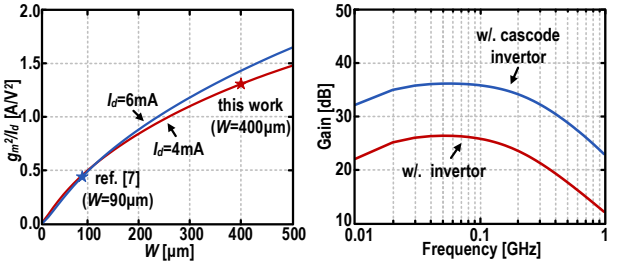


Fig. 2. Schematic of the proposed cryo-CMOS noise-canceling LNA.



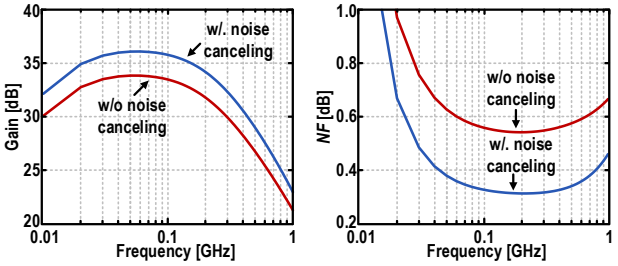
(a) (b)

Fig. 3. Simulation results: (a) Transconductance efficiency g_m^2/I_d of M_4 MOSFET, (b) Overall RF gain of LNA with cascode inverter at 300 K.

are coupled to a self-biased complementary source-follower output stage, which performs signal summation and noise cancellation.

A. Input Stage with Cascode Inverter for High g_m^2/I_d

The input stage employs a cascode inverting configuration, comprising pMOSFETs $M_{1,2}$ ($W/L = 800\,\mu$m$/100$ nm) and nMOSFETs $M_{3,4}$ ($W/L = 400\,\mu$m$/100$ nm). By adopting a 100 nm channel length, the impact of quasi-ballistic carrier transport is minimized, thereby suppressing the Fano factor of shot noise [15] and boosting the intrinsic gain via increased output impedance. To balance the trade-offs between transconductance (g_m), shot noise, and thermal noise, the nMOSFETs are biased at a current density of $5\sim10\,\mu$A$/\mu$m. As g_m^2/I_d serves as a critical figure of merit for noise performance [16], high transconductance efficiency is essential for achieving low noise temperature. By strategically increasing the device width W while reducing the current density I_d/W, this design achieves a 2.9× improvement in g_m^2/I_d compared to [9] in Fig. 3a. Consequently, both shot and thermal noise components are significantly suppressed through the optimization of device sizing and bias current conditions. Furthermore, as illustrated in Fig. 3b, the implementation of the cascode inverting topology substantially enhances the RF voltage gain without increasing DC power consumption relative to the conventional inverter-based design.



(a) (b)

Fig. 4. Simulated LNA performance at 300 K: (a) RF gain, (b) Noise figure.

B. Noise-canceling Stage with Miller Phase Compensation

The noise-canceling stage is a similar cascode inverting topology composed of the same size pMOSFETs $M_{5,6}$ and nMOSFETs $M_{7,8}$ for eliminating channel noise of the input stage. The noise current of the transistors $M_{1,4}$ flows toward its gate through the feedback resistor R_1, creating in-phase noise voltage and out-of-phase signal voltage between nodes A and B, respectively. The in-phase noise and out-of-phase signal voltage at node B follow path1 through the source follower $M_{11,12}$. On the other hand, the noise and signal voltages at node A follow path2 and are further amplified and inverted through the auxiliary transistors $M_{5,6,7,8}$ and then appear at node C through the source follower $M_{9,10}$. The output stage is the parallel connection of self-biased complementary source-followers for combining both the in-phase amplified signals and out-of-phase noise signals at node D and 50-Ω output impedance matching. As a result, the noise voltage is canceled due to the opposite polarity, while the signal voltage is added up.

At high frequencies, the parasitic capacitances (C_{gs}) of the transistors introduce a pole at the input node, which leads to a frequency-dependent phase offset of the noise between nodes A and B. To address this, a Miller capacitor C_1 is incorporated between nodes A and B to introduce a zero, which provides a phase-lead effect. By precisely optimizing the capacitance of C_1, the phase-lead effect can effectively compensate for the phase lag induced by the parasitic capacitances, ensuring noise cancellation across an extended bandwidth. At the $300 \sim 500$ MHz band, the average phase difference of the inverting noise voltage has been improved from 152 deg. to 175 deg., thereby approaching ideal noise cancellation conditions. Fig. 4 shows the 300 K simulated results of the gain and noise figure of the proposed LNA with and without the noise-canceling. The gain and noise figure can be improved by 2.3 dB and 0.22 dB, respectively at 0.2 GHz, compared to those without the noise-canceling.

III. Measured Results

The proposed LNA is fabricated using a standard 28 nm bulk CMOS process, occupying a core area of only 0.012

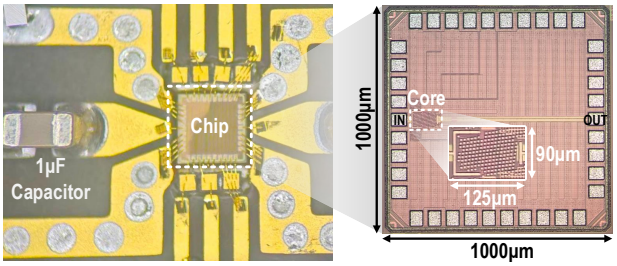


Fig. 5. Photos of fabricated 28 nm CMOS chip and chip packaging.

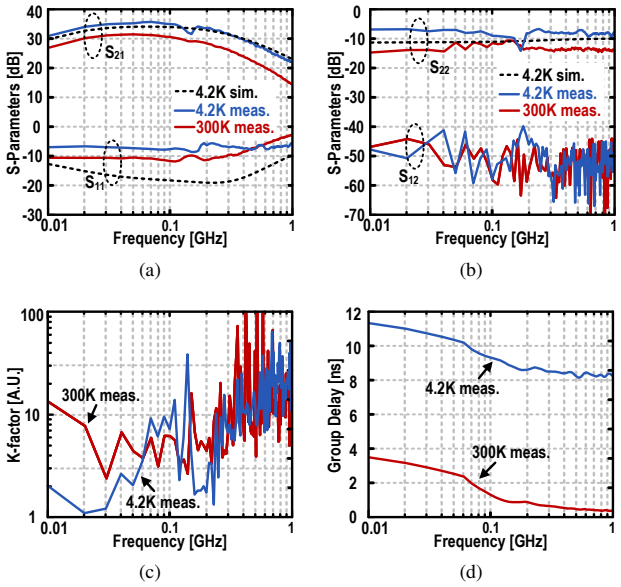


Fig. 6. Measurement results: (a) and (b) S parameters, (c) stability factor K, (d) group delay.

mm^2. The chip microphotograph and the chip packaging are illustrated in Fig. 5. Firstly, the S-parameters measured via a vector network analyzer at both room temperature (300 K) and cryogenic temperature (4.2 K) are compared in Fig. 6a and Fig. 6b. At 300 K, the LNA exhibits a gain (S_{21}) of 22∼31 dB with a bandwidth from 0.01 to 0.5 GHz. The input (S_{11}) and output (S_{22}) return losses are measured within -11.2∼-8.0 dB and -14.5∼-10.2 dB, respectively. Upon cooling to 4.2 K, the LNA performance improves significantly. Due to the increased g_m of the transistors, the gain of the LNA effectively enhances, yielding a S_{21} of 28∼35 dB with a bandwidth of 0.01∼0.5 GHz. Furthermore, the 4.2 K measurement shows the average S_{11} and S_{22} reaching down to -8.6 dB and -9.2 dB, respectively, while the reverse isolation (S_{12}) remains robustly below -40 dB across the operational band. The stability factor (K-factor) provided in Fig. 6c confirms that the LNA remains unconditionally stable (K >1) at both temperature states. Additionally, the group delay characteristics at both 300 K and 4.2 K are as shown in Fig. 6d.

Secondly, the noise performance is evaluated using a Ceyear 3986E NFA at 300 K and the hot-cold method with a

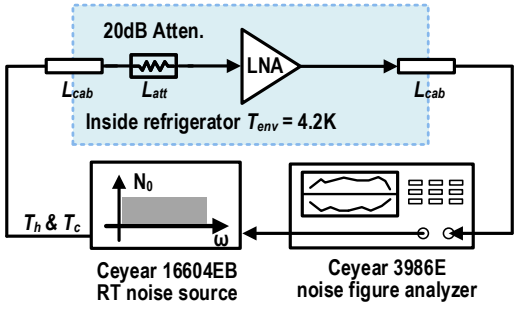


Fig. 7. Measurement setup of noise temperature using cold attenuator at 4.2 K.

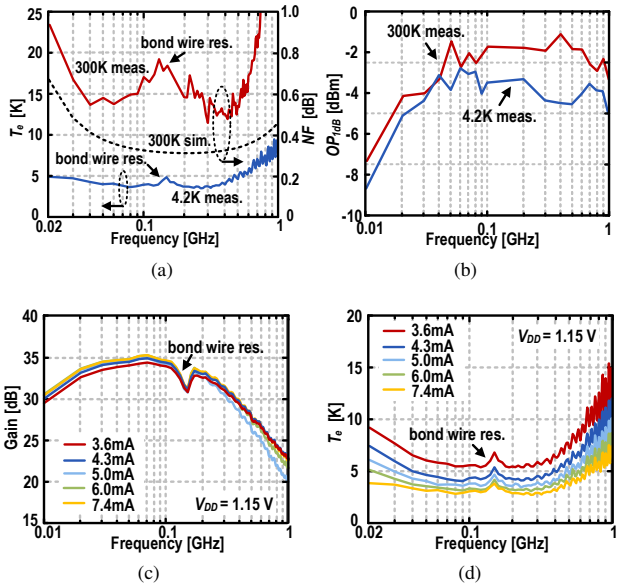


Fig. 8. Measurement results: (a) Noise T_e and NF, (b) output 1-dB comp. point (OP_{1dB}), (c) RF gain, and (d) noise temperature varying bias current.

20 dB cold attenuator [17] at 4.2 K, as detailed in Fig. 7. At 300 K, the LNA achieves a min. noise figure (NF) of 0.5 dB at 0.3 GHz. After rigorous calibration of cable and attenuator losses and noise at 4.2 K, the LNA demonstrates a noise temperature (T_e) of 3.4∼5 K within the 0.01 to 0.5 GHz bandwidth, with a min. T_e of 3.4 K at 0.2 GHz (Fig. 8a). The dips in noise at ∼150 MHz in Fig. 8 are caused by the resonance of the chip bonding wires. This issue can be resolved in the future through redesigning the packaging. The measured output 1-dB compression point (OP_{1dB}) across frequency is depicted in Fig. 8b, validating that the linearity is sufficient for amplifying weak reflected blip signals in spin qubit readout chains. To investigate the dependence of gain and T_e on DC power, the LNA is characterized under varying bias currents with a fixed V_{DD} = 1.15 V. As illustrated in Fig. 8c and Fig. 8d, reducing the current from 7.4 to 3.6 mA results in a gain reduction of ∼1.1 dB and a T_e increase of ∼3.3 K.

Table 1. Performance comparison with the state-of-the-arts.

Ref.	This work	JSSC 2018 [7]	TCAS II 2025 [8]	TMTT 2024 [9]	TCAS II 2024 [10]	RFIC 2024 [11]	TMTT 2024 [4]	IMS 2021 [5]
Architecture	Cascode inverting input+ Noise-canceling	Noise-canceling	Cascode inverting input+Current reuse+ SBB	Noise-canceling+ Current reuse+ SFBB	Noise-canceling+ Current reuse+ SFBB	Cascode inverting input+Current reuse+ SBB	Common-source+ resistive feedback	Source degeneration
Meas. Temp. [K]	4.2	4.0	4.0	4.0	4.0	4.0	3.6	15.0
Frequency [GHz]	0.01∼0.5	0.1∼0.5	0.2∼3.2	0.01∼3	0.01∼2.6	0.01∼2.2	0.1∼8.8	0.1∼3
Gain† [dB]	28∼35	54∼57	41∼43.4	27∼29	30∼31	43.2∼46.7	32∼34	27∼32
Noise Temp.† [K]	3.4∼5	7.0∼36.6	26.6∼67.4	41.6∼60.7	17.7∼35	12∼30.4	5.0∼8.0	5.0∼14.0
Min. Noise Temp. [K]	3.4 at 0.2 GHz	7.0 at 0.5 GHz	26.6 at 0.4 GHz	2.2 at 1.8 GHz	6.7 at 0.6 GHz	9.2 at 0.6 GHz	4.0 at 3.5 GHz	4.0 at 1 GHz
P_{DC} [mW]	8.5	54.9	7.6	19.4	8.6	5.8	8.2	1.0
Core Area [mm^2]	0.012	0.115	0.3	0.018	0.117	0.17	0.017	0.038
Technology	28nm CMOS	160nm CMOS	28nm CMOS	40nm CMOS	40nm CMOS	28nm CMOS	SiGe BiCMOS	SiGe HBT

† within 0.01∼0.5 GHz.

IV. Conclusion

This paper presents a 28 nm cryo-CMOS LNA for spin qubit dispersive readout. To suppress channel noise while improving the RF gain at 4.2 K, a noise-canceling technology utilizing a cascode inverting-based input stage is validated. Table 1 benchmarks the performance comparison with the published cryogenic SiGe and CMOS LNAs. To the author's knowledge, the proposed cryo-CMOS LNA achieves the lowest noise temperature within 10∼500 MHz at 4.2 K, while maintaining a low DC power dissipation of 8.5 mW. Instead of relying on SiGe technology, this work provides a critical integrated building block for high-fidelity reflectometry of the future large-scale silicon spin qubit array.

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