A Bidirectional Neural Interface SoC with 128-Ch HDR Artifact-Resilient Recording, Real-Time Artifact Removal and Spike Sorting

Xiongfei Jiang*, Yuntao Han*, Minghui Cui, Dongxu Guo, Yihan Pan, Mehmet Taskiran, Alfredo Gonzalez Sulser, Themis Prodromakis, Shiwei Wang
(*Equally contributed authors) School of Engineering, University of Edinburgh, UK

***Abstract*—This paper presents a bidirectional neural interface SoC that incorporates 128 high dynamic range (HDR) AFEs, 4 neurostimulators, and an on-chip digital processor for stimulation artifact removal and spike sorting. The chip enables artifact-free recording thanks to the HDR channels tolerating stimulation artifacts up to 300mV_{pp}, and effective artifact removal on chip. A spike sorting processor is further integrated to analyze recorded data in real time and reduce the output data rate. The chip achieves accurate spike sorting even when large stimulation artifacts are present, demonstrating strong potential for reliable bidirectional interfacing in high-density electrophysiology and neuro-prosthesis applications.**

Keywords—*Bidirectional Neural Interface, Artifact-Tolerant Recording, Artifact Removal, Spike Sorting.*

I. Introduction

Modern neuropathology research and neurological disorders therapy require artifact-resilient bidirectional neural interfaces that allow real-time neuronal recording and neuromodulation. Unlike conventional IA+ADC recording architectures (e.g. [1] as shown in Fig. 1 left) that require artifact blanking during stimulation, direct digitization architectures based on continuous-time Delta-Sigma modulators (CTDSM) can achieve high dynamic range (HDR) to accommodate large stimulation artifacts, and thus allowing undisrupted recording [2]. However, their scalability for high-density applications is limited by the increased data rate due to higher bit resolution, as shown in Fig. 1 right. As the number of electrodes grow continuously [1], scalable on-chip neural signal processing is required to compress the data for wireless operation and reduce latency in data analysis, allowing real-time responses to neuronal events [3, 4].

To meet the above requirements, this work presents a bidirectional neural interface SoC that incorporates 128 CTDSM-based HDR AFEs and four neurostimulators. Assisted by an on-chip digital processor, the proposed chip can address stimulation artifacts, compress and analyze the neural signals in real time, achieving true bidirectional interfacing of high-density neurons with optimized scalability.

II. Artifact-Resilient Bidirectional Neural Interface SoC

Fig. 2 shows the architecture of the proposed SoC. It operates with a 2.56MHz primary clock frequency. An on-chip UART module is used for configuration. It has 128 HDR

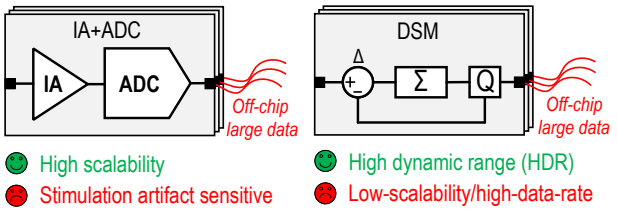

Fig. 1: Prior neural interface architectures: IA+ADC (left), HDR DSM (right).

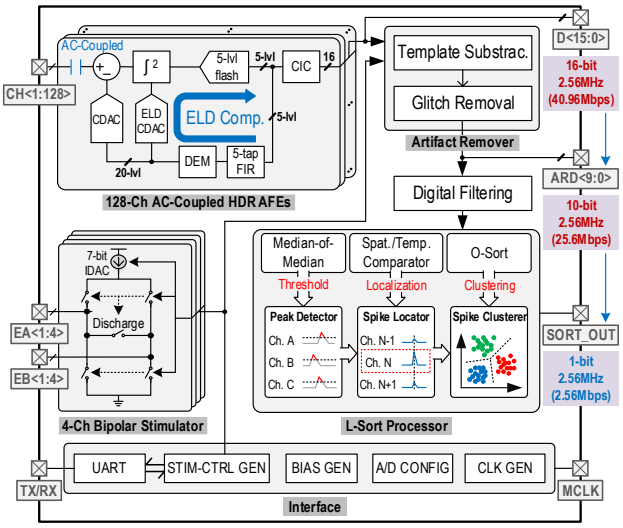

Fig. 2: System architecture of the proposed neural interface SoC.

AFEs that digitize the input neural signals in the bandwidth of 1Hz to 10kHz. The raw data rate after CIC decimation (16-bit resolution and 20kS/s sample rate) and serialization is 40.96Mbps. An artifact remover is embedded to eliminate the stimulation artifacts induced when the four on-chip stimulators are activated, reducing the output data to 25.6Mbps (10 bits per channel). A localization-based spike sorting (L-Sort) [5] processor is integrated to sort the recorded spikes, further reducing the data rate to only 2.56Mbps.

The architecture of the AFE is shown in Fig. 3. It is based on an AC-coupled 2^{nd}-order CTDSM using FIR feedback, employing an oversampling rate (OSR) of 128. The integrator

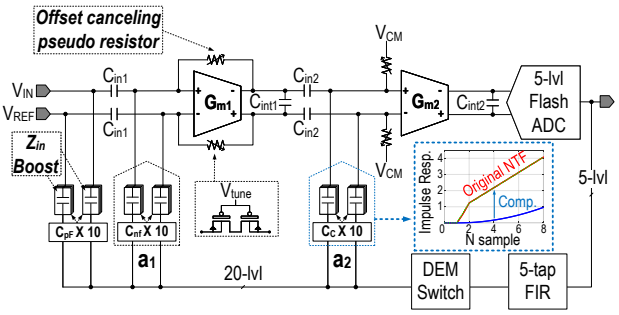

Fig. 3: Architecture of the AC-coupled HDR AFE.

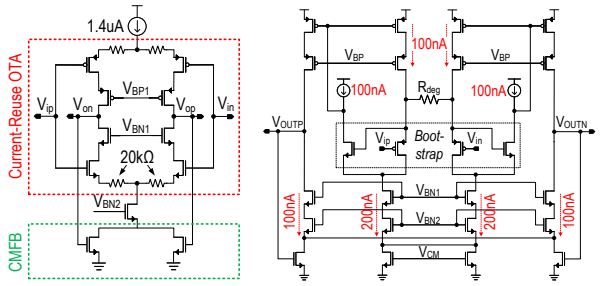

Fig. 4: Schematic of G_{m1} (left), and G_{m2} (right).

output is sampled by a 5-level flash ADC, whose output is filtered by a 5-tap FIR filter, resulting in 20-level feedback through the CDACs (C_{nf} for main feedback and C_{pf} for Z_{in} boosting). The multi-level feedback presents close replicas of the input signal and thus improves the modulator linearity as well as Z_{in} [2]. To compensate for the excess loop delay (ELD) caused by the 5-tap FIR filter, CDAC marked by C_c is used to implement the derived ELD compensation coefficients, achieving good stability by recovering the system impulse response to the original NTF [2].

III. Circuit Implementation

G_{m1} adopts a source degenerated inverter-based OTA topology to achieve better energy efficiency and linearity, as shown in Fig. 4 left; The schematic of G_{m2} is shown in Fig. 4 right, which is based on a flip voltage follower with input parasitic capacitance neutralization [6], allowing precise ELD compensation coupled at the G_{m2} input through CDAC C_c. To improve current efficiency, Both of the OTAs exploit tail transistors that are biased in the triode-region to achieve common-mode feedback (CMFB).

To mitigate non-linearity contributed by components' mismatch, two capacitors are used to implement the 5-level CDAC feedback by using V_{CM} as an extra reference, a dynamic element matching (DEM) switching scheme is proposed to shuffle the references (VCM/VDD/VSS) applied to each element (e.g., $C_{nf} < 1, 2 >$ as shown in Fig. 5) from sample to sample when the flash ADC generates outputs of ±1. The method significantly reduces the non-linearity caused by the mismatch between $C_{nf} < 1, 2 >$ with low area and power overhead.

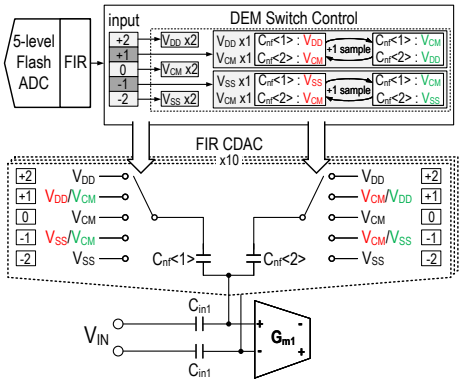

Fig. 5: Schematic of the feedback FIR CDAC C_{nf} and the DEM switching logic. The FIR CDAC C_{nf} and C_c use an identical implementation.

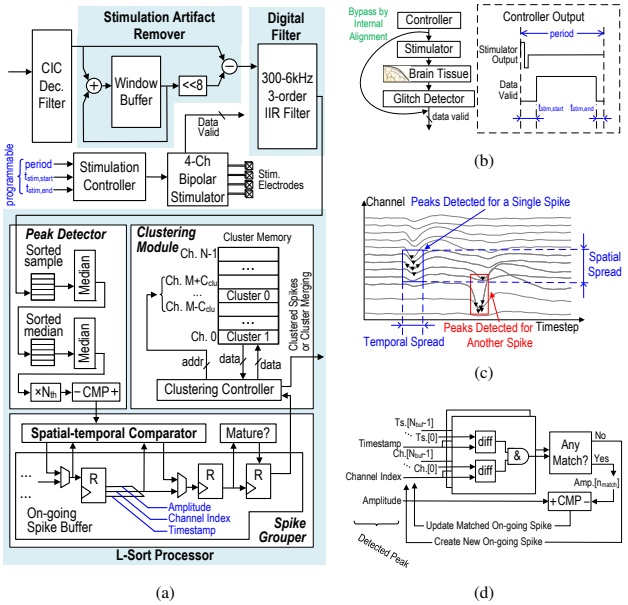

Fig. 6: Digital core design. (a) Architecture of the on-chip stimulation artifact remover and L-Sort spike sorter, (b) Stimulation controller and glitch removal, (c) spike grouping scheme, (d) spatial-temporal comparator.

The architecture of the on-chip digital processor is shown in Fig. 6. The artifact remover is enabled when the stimulator is activated. It uses a window buffer to accumulate 256 periodic artifact windows, which are averaged to derive an artifact template. The template is then subtracted from the channel outputs to cancel artifacts. To remove the residual artifact glitches, a 'data valid' signal generated by the stimulation controller and aligned with the stimulation period is used to exclude samples with artifact glitches. The data is then filtered by a 3^{rd}-order IIR filter to remove LFP and then sent to the spike sorter. The peak detection threshold is determined by a median-of-median calculator. Since multiple spatial-temporally adjacent peaks may be detected for a single spike, a spike grouper with spatial-temporal comparator and an on-

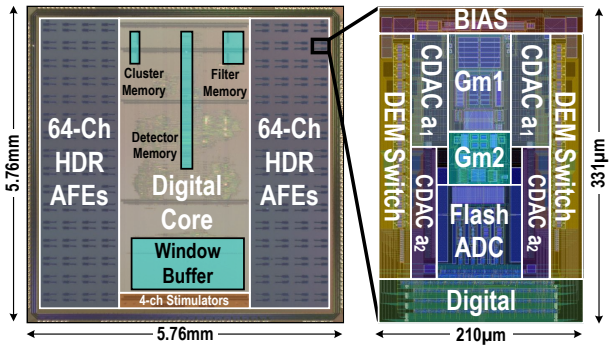

Fig. 7: Chip micrograph with dimension.

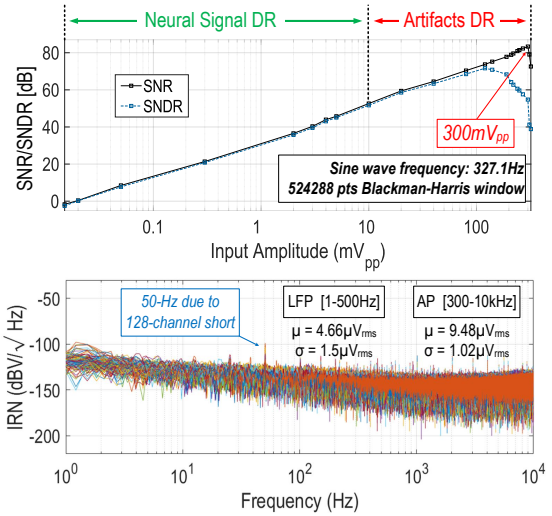

Fig. 8: Measured SNR/SNDR versus input amplitude of the AFE (top), Measured IRN of the 128-channel AFE (bottom).

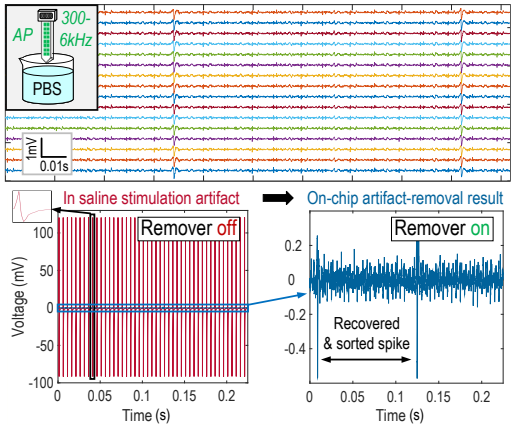

Fig. 9: Chip in saline spike recording results (top). Measured effectiveness of the on-chip artifact remover against in saline stimulation artifact (bottom).

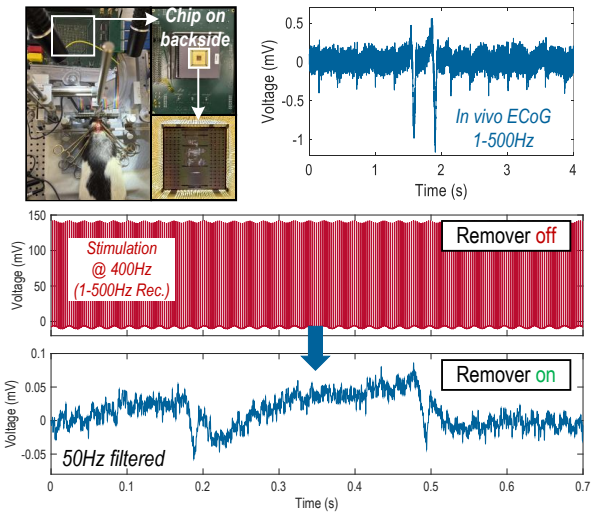

Fig. 10: Chip *in vivo* ECoG recording results (top). Measured effectiveness of the on-chip artifact remover against *in vivo* stimulation artifact (bottom).

going spike buffer is implemented to find the peak amplitude within a spatial/temporal spread. The peak in the buffer is considered to be mature as a detected spike when no spatially adjacent peak has been detected for 30 timesteps. The spike clusterer implements an O-Sort algorithm but only searches within several adjacent channels like [3]. This L-Sort processor requires less memory since no temporal feature is utilized and previous samples are no longer retained, as illustrated in [5].

IV. Measurement Results

The micrograph of the SoC fabricated in 180nm technology is shown in Fig. 7. The AFE and digital processor are supplied by 1.8V, while the stimulator is supplied by 3.3V. Fig. 8 top shows the measured input range of the AFE, demonstrating a total $300\mathrm{mV_{pp}}$ artifact tolerance range. Fig. 8 bottom shows the measured average 128-channel LFP/AP band IRN of 4.66μVrms/9.48μVrms, leading to a DR of 81dB.

The measured on-chip stimulator can generate an 8 bits current output from -3.81mA to 3.81mA. To validate the neural recording and artifact removal capability of the chip, biological experiments are performed. Fig. 9 top shows the multi-channel in saline spike recording results, demonstrating the neuronal recording capability of the chip. Fig. 9 bottom shows the resilience of the on-chip artifact remover against real stimulation artifacts (>$200\mathrm{mV_{pp}}$) present in saline, successfully recovering the pre-recorded spikes from the artifacts. Due to neural probe failure, ECoG electrodes are used for *in vivo* measurement. Fig. 10 top shows the setup of the *in vivo* test and its ECoG recording results; bottom shows the neural events recovered from $150\mathrm{mV_{pp}}$ *in vivo* stimulation artifacts.

Fig. 11 (a) shows the localization results of 7 neurons in set 1 [10]; it validated those locations detected by the chip are spatially close to the ground truth calculated by an offline center-of-mass algorithm. Fig. 11 (b) shows the setup for testing the full analog-to-sorted-spike signal chain with an MEArec-generated data [11]; the four neurons, each with 3-ch spatial spread, have been successfully sorted, whose firing intervals match the replay repeating period. Fig. 11 (c) shows

TABLE I: Comparison with state-of-the-art multi-channel neural interface/processor ICs.

		This Work	VLSI23 [7]	VLSI24 [1]	JSSC25 [2]	ISSCC25 [8]	VLSI25 [9]	ISSCC25 [4]
System	Technology (nm)	180	130	55	180	65	28	40
	Supply (V)	1.8/3.3	1.5/±2.5	1.2	1.8	0.45/1/2.5	0.46	0.72
	chip area (mm^2)	33.2	144	15.7	4.8	0.82[a]	0.27[a]	1.68
	Power	55.6mW	38.8mW	29.7mW	5.39μW/Ch	1.6μW/Ch	2.37μW/Ch	0.074μW/Ch
Neural Recording	# of channel	128	256/1024	1536	32	64	-	-
	Neural Signal	LFP+AP	ECoG	LFP+AP	ECoG	AP		
	Input Couple	AC	DC	AC	DC	DC		
	Bandwidth (Hz)	1-10k	10-4k	0.5-10k	1-500	300-7k		
	IRN (μV_{rms})	4.7 (1-500Hz) 6.6 (300-6kHz) 9.5 (300-10kHz)	4.3/8.7 (10-4kHz)	7.6 (0.5-1kHz) 6 (300-10kHz)	3.7 (1-500Hz)	5.5 (300-7kHz)		
	Input Range (mV_{pp})	300	< 2.1[b]	10	222	-		
	DR	81	< 44.7[c]	55.4[c]	83	-		
	Artifact Removal	Yes	No	No	No	No		
Stim.	# of channel	4	16384	-	2	4	-	-
	Current Res.	8 bits	3 bits		7 bits	8 bits		
Spike Sort.	Feature	Spatial	-	-	-	Temporal	Template	Spatial
	# of channel	128				64	128	1024
	Accuracy (%)	97.2				94.58	93.3	99.7
	Accuracy drop w/ artifact (%@mV_{pp})	<0.1@∼300				0.3-0.7@∼0.1	-	-

[a]Core only [b]Estimated by using core supply and minimum AFE gain [c]Estimated based on input range and IRN

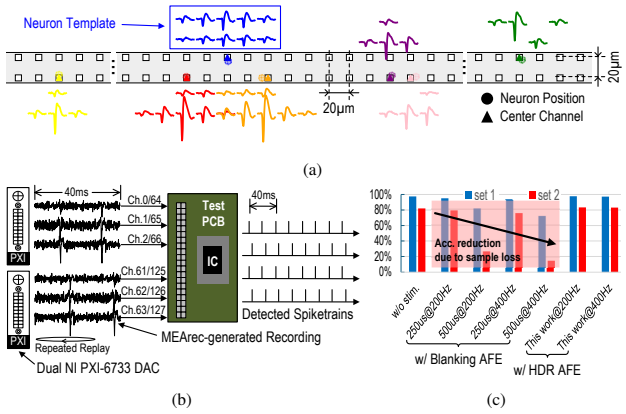

Fig. 11: Spike sorting results. (a) Spike localization result, (b) on-chip analog-to-sorted-spikes testing setup, (c) sorting accuracy degradation with $300mV_{pp}$ stimulation artifact.

the accuracy degradation for spike sorting by adding measured in-saline artifacts with different stimulation periods/durations to the data. The accuracy drops significantly in conventional blanking AFEs due to sample loss, while the proposed chip shows negligible (<0.1%) accuracy reduction.

V. Summary and Comparison with State-of-the-Art

This work presents a bi-directional neural interface SoC with 128 HDR AFEs, four bipolar stimulators, and on-chip digital processors. The chip achieves a $300mV_{pp}$ stimulation artifact resilience enabled by the HDR AFE and the on-chip artifact remover, and achieves a low 2.56Mbps output data rate allowed by the on-chip spike sorter. TABLE I includes the chip details and compares this work with state-of-the-art multi-channel neural interface/processor ICs, indicating that it is the only one that integrates real-time high-accuracy spike sorting with HDR AFEs and effective stimulation artifact removal.

VI. Acknowledgement

This work was supported by the EPSRC program FORTE, under Grant EP/R024642/1; the RAEng Chair in Emerging Technologies, under Grant CiET1819/2/93.

References

[1] X. Yang *et al.*, "A highly-integrated 1536-channel quad-shank monolithic neural probe in 55nm cmos for full-band raw-signal recording," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2024, pp. 1–2.

[2] X. Jiang *et al.*, "A bi-directional neural interface chip with 32-channel 83-db dr ctdsm-based recording using firdac with pre-emptive eld compensation," *IEEE Journal of Solid-State Circuits*, pp. 1–14, 2025.

[3] Y. Chen *et al.*, "A 384-channel online-spike-sorting ic using unsupervised geo-osort clustering and achieving 0.0013mm2/ch and 1.78μW/ch," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 486–488.

[4] A. Akhoundi *et al.*, "15.2 a 1024-channel 0.00029mm2/ch 74nw/ch online spatial spike-sorting chip with event-driven spike detection and self-organizing map clustering," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 268–270.

[5] Y. Han *et al.*, "L-sort: On-chip spike sorting with efficient median-of-median detection and localization-based clustering," *IEEE Open Journal of Circuits and Systems*, vol. 6, pp. 205–216, 2025.

[6] S. Wang *et al.*, "A compact chopper stabilized $\delta - \delta\sigma$ neural readout ic with input impedance boosting," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 67–78, 2021.

[7] N. Zeng *et al.*, "A wireless, mechanically flexible, 25μm-thick, 65,536-channel subdural surface recording and stimulating microelectrode array with integrated antennas," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2023, pp. 1–2.

[8] Y. Huang *et al.*, "15.4 a neuroprosthetic soc with sensory feedback featuring frequency-splitting-based wireless power transfer with 200mb/s 0.67pj/b backscatter data uplink and unsupervised multi-class spike sorting," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 272–274.

[9] Z. Wen *et al.*, "A 28nm online spike sorting processor based on multi-channel template matching," in *2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2025, pp. 1–3.

[10] N. Steinmetz. (2016, Feb.) Sorting comparison results. [Online]. Available: http://phy.cortexlab.net/data/sortingComparison/

[11] A. P. Buccino *et al.*, "Mearec: A fast and customizable testbench simulator for ground-truth extracellular spiking activity," *Neuroinformatics*, vol. 19, no. 2, pp. 185–204, 2020. [Online]. Available: https://link.springer.com/article/10.1007/s12021-020-09467-7