aF-Resolution On-Chip Characterization of Sub-fF Non-Volatile Capacitance in Nanoscale FeFET

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***Abstract*—The gate-to-source/drain non-volatile capacitance (nvCAP) of FeFET devices remains insufficiently characterized due to the difficulty of accurate sub-fF capacitance measurements off-chip. As nvCAP based charge-domain compute paradigm has shown the promise of boosting energy efficiency, the experimental characterization is desired to validate the scaling trend for the nvCAP as further guidance. To enable aF-resolution, a custom on-chip capacitance-to-voltage converter measurement (CVCM) circuit is designed and taped-out on GlobalFoundries 28nm FeFET platform. In this work, the gate-to-source/drain capacitance of FeFET devices is experimentally investigated across three scaled geometries ($1\,\mu\text{m}\times1\,\mu\text{m}$, $500\,\text{nm}\times500\,\text{nm}$, and $200\,\text{nm}\times200\,\text{nm}$) with MOSCAP-assisted calibration. The C-V characteristics are extracted separately under programmed and erased states by sweeping the gate voltage from $-0.5\,\text{V}$ to $1\,\text{V}$. The results reveal a systematic reduction in capacitance on/off ratio with device scaling, from $12.1\times$ at $1\,\mu\text{m}\times1\,\mu\text{m}$ to $3\times$ at $200\,\text{nm}\times200\,\text{nm}$. TCAD simulations further corroborate the experimental results and confirm the observed scaling behavior.**

***Index Terms*—C–V characterization, capacitance measurement circuit, device scaling, ferroelectric field-effect transistor (FeFET), non-volatile capacitor (nvCAP), TCAD simulation**

I. Introduction

Ferroelectric devices are increasingly explored for data-intensive edge AI accelerators, such as compute-in-memory (CIM) and content-addressable-memory (CAM), due to their non-volatility and low programming energy. Representative implementations include FeFET [1], FeRAM [2], and non-volatile capacitor (nvCAP) [3] [4] [5]. Among these, nvCAP-based architectures are particularly attractive due to their dynamic power-only and non-destructive read operation with small read voltages, as shown in Fig. 1.

However, the scalability of nvCAP-based circuits is fundamentally constrained by the lack of accurate experimental capacitance characterization at deeply scaled dimensions. In particular, the capacitance on/off ratio, defined as the ratio between the high-capacitance state (C_{HCS}) and the low-capacitance state (C_{LCS}), remains poorly understood at small scales, despite its critical impact on system performance, power, and area. Existing experimental results [6] [7] are largely restricted to tens to hundreds of μm devices due to the off-chip probing constraints, while nanoscale behavior is typically inferred through modeling and extrapolation. Direct measurement of sub-μm nvCAP capacitance is particularly challenging, as measurement accuracy at the aF scale is severely limited by parasitic capacitances and instrumentation resolution. Quasi-static C–V measurements are dominated by pad parasitics [8] as shown in Fig.2(a), and LCR-based techniques are fundamentally limited to the fF range [9] as shown in Fig.2(b). RF C–V methods based on S-parameter extraction alleviate parasitic effects through de-embedding, but require complex calibration procedures and dedicated structures [10], which significantly increase measurement overhead for nanoscale device-level C–V characterization as Fig.2(c). On-chip charge-based capacitance measurement (CBCM) [11] removes external parasitics, yet its bias range is determined by the supply rail of the charging transistors, precluding continuous gate-voltage sweeping required for full-range C–V extraction as Fig.2(d). As a result, a direct and accurate experimental approach for nanoscale nvCAP capacitance characterization is still lacking.

In this work, we present an on-chip capacitance-to-voltage converter measurement (CVCM) methodology [12] with MOSCAP-assisted calibration for direct aF-level characterization of nvCAP devices as Fig.2(e). The gate capacitance of FeFET devices is measured across scaled geometries from $1\ \mu\text{m}\times1\ \mu\text{m}$ down to $200\ \text{nm}\times200\ \text{nm}$. C–V characteristics of foundry FeFET configured in the nvCAP mode are successfully extracted under small-signal excitation following program/erase pulsing operations. The results reveal a systematic reduction in capacitance on/off ratio with device scaling, providing the first direct experimental evidence of nvCAP scaling behavior in the sub-fF regime and offering design guidance for nvCAP-based circuits. The rest of this paper is organized as follows: Section II introduces the operating principle of nvCAP and the physical origin of the capacitance on/off ratio. Section III presents the proposed on-chip CVCM circuit and the MOSCAP-assisted calibration scheme. Section IV demonstrates the measurement results across three scaled device geometries, and TCAD simulations have also been performed to further support the experimental results.

II. Fundamentals of nvCAP Operation

The nvCAP typically utilizes either Metal-Ferroelectric-Metal (MFM) or Metal-Ferroelectric-Semiconductor (MFS) stacks, as shown in Fig. 3(a). This paper characterizes an MFS-type nvCAP on the GlobalFoundries 28nm FeFET platform. The capacitance on/off ratio ($C_{\text{HCS}}/C_{\text{LCS}}$) is fundamentally

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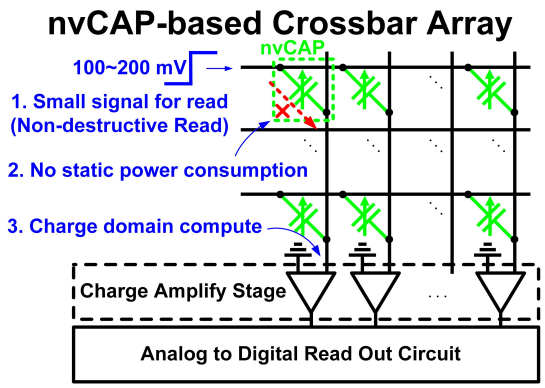

Fig. 1. nvCAP-based crossbar array for small-signal charge-domain compute-in-memory.

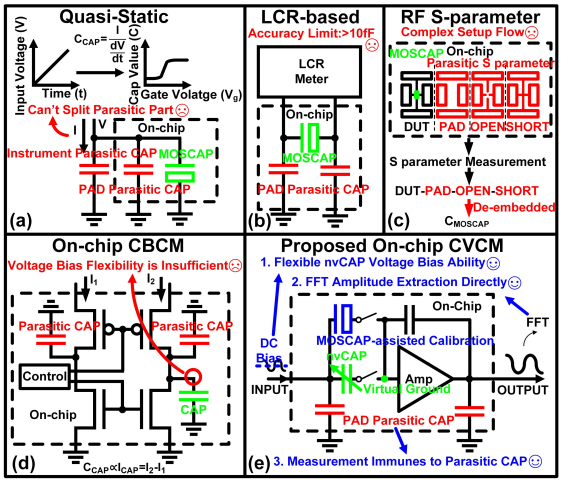

Fig. 2. Comparison of C–V measurement techniques: (a) Quasi-Static, (b) LCR-based, (c) RF S-parameter, (d) on-chip CBCM, and (e) proposed on-chip CVCM.

governed by the geometric ratio of the total gate area to the parasitic overlap area [7] (Fig. 3(b)). Physically, this is achieved through dipole-induced threshold (V_{th}) shifts: in the programmed state (low V_{th}), a gate bias forms an inversion layer to enable C_{HCS} via gate-to-channel coupling. In the erased state (high V_{th}), the depletion in the channel restricts the capacitance to the overlap regions, resulting in C_{LCS} (Fig. 3(c)). nvCAPs in a capacitive crossbar array enable charge-domain compute with non-destructive small input voltage (e.g., 100 mV), where charge transfer is assisted by the peripheral circuit (e.g. operational amplifier). In such a scheme, only dynamic power is consumed by eliminating the excessive static power that typically dominates the resistive crossbar array.

III. aF-Resolution Cap Measurement Circuit

A. The Proposed CVCM Test Structure

To enable accurate measurement of nanoscale nvCAP devices in the aF regime, we propose an on-chip CVCM test structure that effectively avoids the pad connection parasitics. As illustrated in Fig. 4(a), the circuit adopts a two-stage

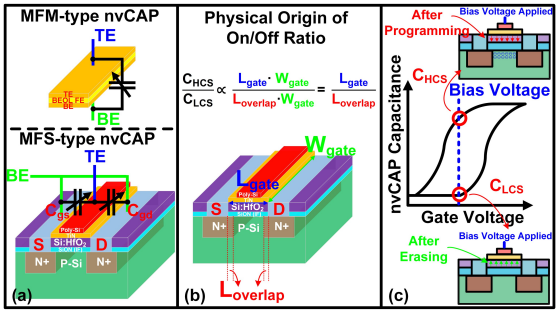

Fig. 3. (a) Device structures of MFM- and MFS-type nvCAP. (b) Physical origin of C_{HCS} and C_{LCS} in FeFET (nvCAP mode) that is governed by gate-to-overlap area ratio. (c) C–V characteristics for MFS nvCAP under program and erase conditions.

amplification. In the first stage, the target nvCAP C_{nvCAP} is configured with a known feedback capacitor C_f, forming a capacitive sensing amplifier stage. The adjustable high-value feedback resistor is also used to provide the stable DC bias point. Under fixed small-signal input excitation, the output voltage of the first stage $v_{out,1}$ is proportional to the capacitance ratio, given by (1):

$$v_{out,1} = v_{in} \cdot \frac{C_{nvCAP}}{C_f} \tag{1}$$

This first stage directly encodes the nvCAP capacitance as a voltage ratio, with C_f configurable between 5 fF and 10 fF ($\pm 10\%$ process variation) to balance measurement sensitivity and output swing range. However, due to the minimum realizable on-chip capacitor size, C_f cannot be arbitrarily reduced, which limits the achievable signal amplitude. To address this limitation, a second-stage amplifier ($A_{v2} = 1$ or 10) is introduced to further amplify the signal and provide sufficient output drive capability for external readout after the chip is packaged. The overall output $v_{out,2}$ is expressed as (2):

$$v_{out,2} = A_{v2} \cdot v_{out,1} \tag{2}$$

This two-stage architecture enables reliable extraction of aF-level capacitance variations while maintaining robustness against parasitic effects. Due to the virtual-ground operation of the first-stage amplifier, parasitic capacitance to real-ground has negligible impact on the feedback loop and therefore minimally affects the extracted nvCAP capacitance. In addition, on-chip MOMCAP are integrated for functionality verification, while MOSCAP serves as the calibration reference. Although the CVCM circuit achieves aF-resolution, the extracted C–V characteristics are subject to two sources of systematic error: (1) a gain error arising from finite open-loop gain and process mismatch in the feedback path, and (2) an offset error caused by the voltage-dependent pass-gate resistance and device mismatch. Since both contributions are captured in the deviation between the measured and PDK MOSCAP C–V curves, a gain and offset correction factor is derived and applied to the raw data from the nvCAP measurement, and

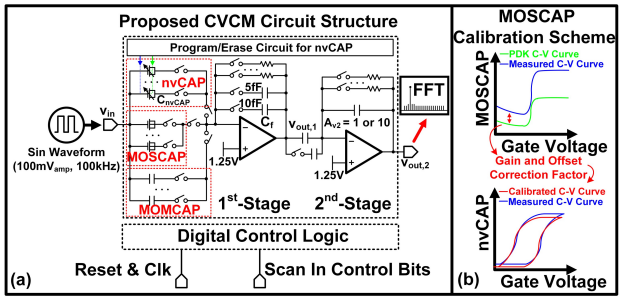

Fig. 4. (a) Proposed CVCM circuit structure. (b) MOSCAP-assisted calibration scheme.

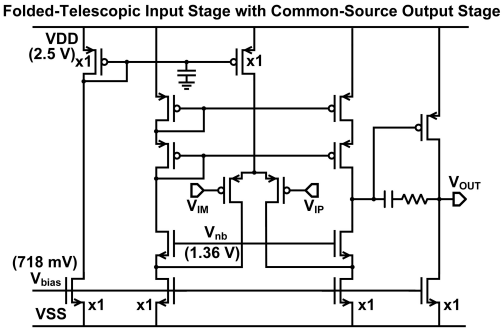

Fig. 5. Schematic of the proposed two-stage amplifier: folded-telescopic input stage with common-source output stage.

such MOSCAP-assisted calibration scheme as illustrated in Fig. 4(b).

B. Two-stage Amplifier Design

To achieve high measurement resolution, a two-stage amplifier is designed using 2.5 V I/O transistors, comprising a folded-telescopic input stage for low input-referred noise and high open-loop gain, followed by a common-source output stage for additional gain and off-chip drive capability (Fig. 5). Long-channel devices and large bias currents are adopted to suppress flicker and thermal noise. Three external bias voltages (V_{bias}, V_{nb}, V_{IP}) are supplied via off-chip references. Under a 2.5 V supply, the amplifier achieves 96.6 dB DC gain, 1.88 MHz unity-gain bandwidth, with a total power consumption of 260.8 μW per amplifier.

IV. Measurement Results and Discussions

A. Measurement Setup

The nvCAP C–V characteristics are measured using a Keysight 81160A source generator to supply a sinusoidal excitation of 100 mV amplitude at 100 kHz, with the DC bias swept from 0.75 V to 2.25 V to scan the nvCAP gate voltage bias over a -0.5 V to 1 V range relative to the 1.25 V virtual-ground. The output is captured by a Keysight MSOS804A oscilloscope, where FFT with a Flat Top window is applied to extract the 100 kHz signal amplitude with high accuracy. Prior to each C–V sweep, program and erase pulses of $\pm$(3.5–3.9) V are applied between gate and bulk to set the two ferroelectric polarization states, as shown in Fig. 4(a).

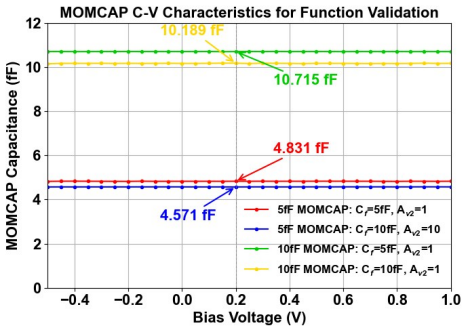

Fig. 6. Measured C–V characteristics of on-chip MOMCAP (5 fF and 10 fF) using different C_f and A_{v2} configurations.

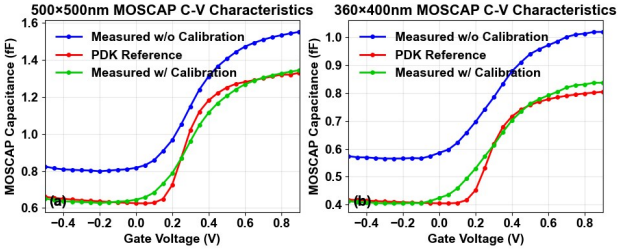

Fig. 7. (a) Measured vs. PDK C–V curves for 500 nm $\times$ 500 nm MOSCAP establishing the calibration factor. (b) Calibrated vs. uncalibrated C–V curves for 360 nm $\times$ 400 nm MOSCAP validating the calibration scheme.

B. Circuit Validation and MOSCAP-Assisted Calibration

Circuit functionality is first validated using on-chip MOMCAPs (5 fF and 10 fF), where consistent extraction across different C_f and A_{v2} configurations confirms measurement accuracy, with residual deviations within the expected process variation range (Fig. 6).

The MOSCAP-assisted calibration is then established using a 500 nm $\times$ 500 nm MOSCAP in sub-fF-level range, whose post-layout simulated C–V curve serves as the PDK reference. The gain and offset correction factor is derived from the deviation between the measured and PDK C-V curves, as shown in Fig. 7(a). The calibration is validated on a 360 nm $\times$ 400 nm MOSCAP, where the corrected curve shows significantly improved agreement with the reference compared to the uncalibrated result, as shown in Fig. 7(b).

C. Calibrated nvCAP C–V Characteristics and Scaling Analysis

Following MOSCAP-assisted calibration, the C–V characteristics of nvCAP devices under programmed and erased states are extracted across three scaled geometries, as shown in Fig. 8(a–c). The capacitance on/off ratio at $V_G = 0$ V decreases systematically with device scaling: from 12.1 at 1 μm $\times$ 1 μm, to 6.2 at 500 nm $\times$ 500 nm, and to 3 at 200 nm$\times$200 nm, confirming the scaling degradation of nvCAP on/off ratio in the sub-fF regime.

D. TCAD Simulation Validation

To further corroborate the measurement results, TCAD simulations are performed on the FeFET devices with process pa-

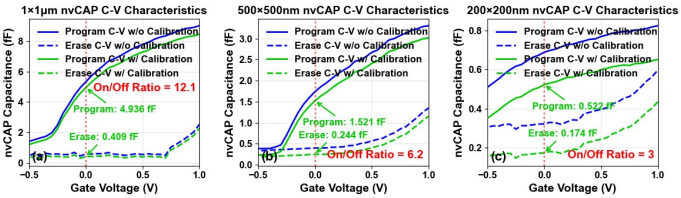

Fig. 8. Calibrated C–V characteristics of nvCAP devices under programmed and erased states for (a) $1\,\mu\text{m} \times 1\,\mu\text{m}$, (b) $500\,\text{nm} \times 500\,\text{nm}$, and (c) $200\,\text{nm} \times 200\,\text{nm}$ device geometries.

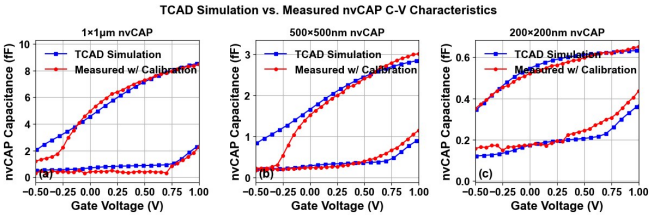

Fig. 9. TCAD simulation vs. measured nvCAP C-V characteristics for (a) $1\,\mu\text{m} \times 1\,\mu\text{m}$, (b) $500\,\text{nm} \times 500\,\text{nm}$, and (c) $200\,\text{nm} \times 200\,\text{nm}$ device geometries.

rameters fixed to nominal values ($SiO_2/HZO = 0.8/10nm$, $L_{overlap} = 30nm$). Additionally, acceptor traps (D_{IT}) with a uniform distribution at the Si/SiO_2 interface were introduced. By varying the device width and length across the three measured geometries, the simulated C–V curves under programmed and erased states are compared against the experimental data, as shown in Fig. 9. The consistent agreement across all device sizes confirms the validity of the measured C–V characteristics and the observed scaling trend within a unified process framework.

E. nvCAP C-V Measurement Comparison

As summarized in Table I, this work achieves the smallest measured device area among reported nvCAP C–V characterization works, extending the measurement capability into the nanoscale regime for the first time. The test chip micrograph and measurement setup are shown in Fig. 10.

TABLE I
COMPARISON OF NVCAP C–V MEASUREMENT

	IEDM'21 [5]	VLSI'22 [4]	EDL'23 [7]	EDL'25 [6]	This Work
Device Type	MFM nvCAP	MFS nvCAP	MFS nvCAP	MFS nvCAP	MFS nvCAP
Width	200 μm	N/A	N/A	700 μm	200 nm–1 μm
Length	200 μm	N/A	N/A	300 μm	200 nm–1 μm
Minimum Area	40000 μm^2	2200 μm^2	5540 μm^2	210000 μm^2	0.04–1 μm^2
Measurement Method	Off-Chip	Off-Chip	Off-Chip	Off-Chip	On-chip CVCM

V. CONCLUSION

This work demonstrates the first direct C–V characterization of nanoscale nvCAP devices in the sub-fF regime, enabled by an on-chip CVCM methodology with MOSCAP-assisted calibration. The measured capacitance on/off ratio degrades

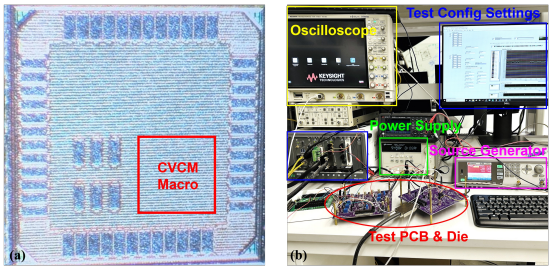

Fig. 10. (a) Labelled chip micrograph outlining the CVCM macro. (b) Test setups used for getting measurement results.

significantly from 12.1× to 3× as the device scales from $1\,\mu\text{m} \times 1\,\mu\text{m}$ to $200\,\text{nm} \times 200\,\text{nm}$, a trend corroborated by TCAD simulations. These findings highlight the necessity of overlap-length optimization and area-ratio-aware design for maintaining sufficient on/off contrast in scaled nvCAP-based compute architectures.

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