A Compact K/Ka Band Transceiver Using Edge-Combining based LO Tripler with Auto Harmonic Rejection Calibration for Phased-Array Integrations

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***Abstract*—The work presents a compact transceiver (TRX) for K/Ka band phased-array. Switched-capacitor (SC) based phase interpolator (PI) and 3-phase edge-combining techniques are proposed to triple the LO frequency while operating within 5.6-10.4GHz. The auto PI calibration logic and Class-D edge-combiner together reduce the out-of-band harmonic interferences and improve the tripling efficiency. The voltage-type stacked PA achieves supply voltage boosts to improve the output power. The stacked LNA shows lower quality factor requirements of the load inductor. With an 8-bit baseband phase shifter, the TRX provides the capability of phased-array integration. This work presents a 17-31GHz RX, featuring a gain of 18-45dB, a noise figure of 3.2-4.3dB, a power of 59-71mW with a 0.23mm² core area. The TX shows a peak output saturation power of 19.84dBm and a peak PA drain efficiency of 40.2% in 20-28.5GHz, with a 0.36mm² core.**

Keywords*—*Transceiver, Phased array, Tripler, Compactness, Class-D, Auto calibration, Phase Noise, Stack, CMOS, PA, LNA.

I. Introduction

Demands for sensing and communication with higher bandwidth have promoted the development of K/Ka band transceivers [1-3]. Facing the higher transmission loss and sensitivity requirements, phased-array systems show more suitability for mm-Wave applications. Therefore, for easier phased-array integrations, transceivers (TRX) with a small die area and high re-configurability deserve better adaptation [4]. However, high-performance but low area costs mm-Wave quadrature local oscillator (LO) generation is difficult. Commonly used methods to obtain orthogonal LOs are shown in Fig.1. The injection lock-based frequency multiplication scheme shows high system efficiency and harmonic rejection ratio (HRR). But the high Q locking process limits the LO bandwidth [5]. Compared with the RC-CR poly-phase filter (PPF), in mm-Wave frequencies, the multi-stage hybrid architecture provides a higher bandwidth, a lower signal loss, and a higher robustness to load or process mismatch. But the die area consumption is relatively high due to the existence of inductors [6]. The multi-phase edge-combining can achieve frequency multiplication with a simple LO chain and low area costs through the avoidance of inductors [7]. However, higher power consumption and extra phase calibration complexity bring difficulties to TRX.

In this work, a compact quadrate LO tripler is introduced for the proposed TRX. The switched-capacitor (SC) based multiphase generation lowers the phase noise degradation and the auto phase calibration strengthens the HRR. The stacked PA and LNA are designed to improve the front-end performance while reducing the additional area costs. With an 8-bit baseband phase shifter (PS), the TRX provides the capability of phased-array integration. This work presents a

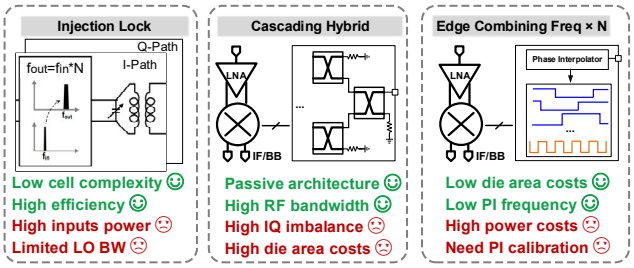


Fig. 1. Quadrate LO generation methods in mm-Wave frequencies including (a) injection lock (b) cascading hybrids and (c) edge-combining.

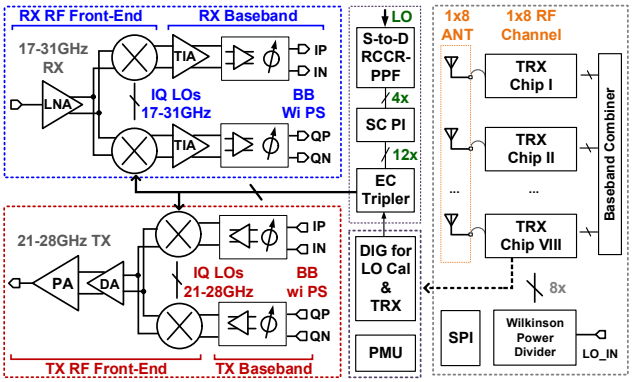


Fig. 2. Block diagram of the proposed TRX and the 1×8 phased array.

K/Ka band TRX with only a 0.59mm² core, featuring a RX gain of 25-46dB, a RX noise figure of 3.2-4.3dB, a peak TX Psat of 19.84dBm, and a peak TX Drain efficiency of 40.2%.

II. Circuit Implementation

A. The Block Diagram of the Transceiver

Fig. 2 shows the block diagram of the proposed K/Ka band compact TRX. The TRX includes two LO frequency triplers, a RX RF front-end (RFFE), a RX analog baseband (BB) with PS, a TX RFFE, a TX BB with PS, a digital module for auto PI calibration and TRX re-configuration, and power management cells. In the phased array system, LO signals are fed to each chip through the Wilkinson power divider. A 1×8 array antenna is integrated into the system and wire-bonded to TRX. The RX outputs and the TX inputs are summed in baseband and the SPI controls the chips.

B. Edge-Combining-Based Tripler and HRR Enhancement

The 17-31GHz quadrature LO tripler is shown in Fig.3. 5.6-10.4GHz signals are converted to differential ones, then they are reshaped to sine waves by the Class-AB buffer for RC-CR PPF inputs. For I-path LO generation, switched

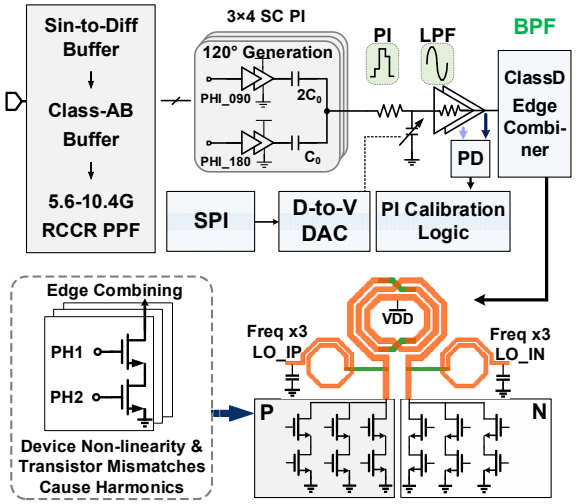


Fig. 3. The design of the LO tripler and the Class-D edge-combiner.

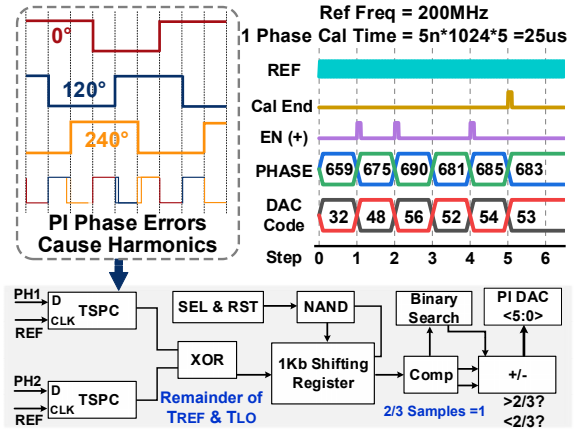


Fig. 4. Proposed auto phase calibration of PI and the timing diagram.

capacitor phase interpolator (SC-PI) is employed to generate 120° shifted signals. The harmonics of the resulting two-step square waves are filtered by the followed RC low-pass filter (LPF). Compared with the charge-based PI, the SC PI with fewer transistors and sharp transition edges can lower the phase noise contribution [8]. In the edge-combiner, three input signals with 120° phase offset would result in a frequency-tripled signal. 90° shifted inputs compared with I-path in SC-PI can generate the Q-path LOs.

The sub-harmonic spur is caused by the PI phase error and the transistor non-linearity of the edge combiner. To realize high harmonic rejection ratio (HRR) during edge combining, a Cass-D edge combiner with LC output matching is designed for frequency tripling. Compared with inverter-based edge combiners, the Class-D one owns better band-pass filtering and efficiency [7].

The auto PI phase calibration logic shown in Fig.4 is designed to lower the phase error. The 120° shifted LO signals are down-converted by the sampling clock ($f_{REF} \leq$ 200MHz is coprime to LOs) in TSPC, then the phase information is preserved in 1Kb shifting registers through XOR. The sampling is to obtain the remainder of the periods of LOs and the sampling clock. For 120° shifted signals, after XOR, 2/3 of sampling results are 1 [9]. As shown in the timing diagram, the sampled results are compared with the reference (1024×2/3) to find the direction of binary search

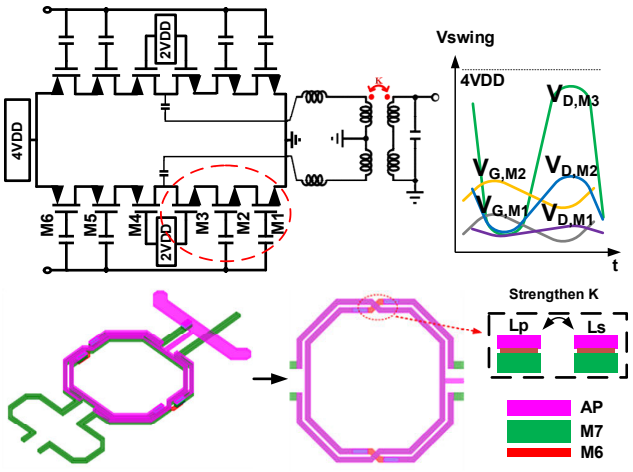


Fig. 5. The detailed structure of the proposed voltage type CMOS-stacked PA and the wideband output matching XFMR.

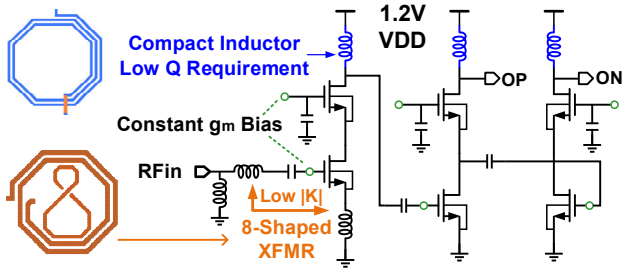


Fig. 6. Architecture of the proposed stacked LNA.

convergence and calibrate the PI by regulating the varactor in PI LPF. The calibration is completed in 5 times searching and the theoretical precision is equal to 360 / 1024. The calibration method with easy logic has configurable f_{REF}, comparison reference, and redundant bit.

C. CMOS-Stacked PA in TXFE

Fig.5 shows the detail of the proposed PA design. To achieve high output power in advanced technology nodes, a voltage-type CMOS-stacked architecture is chosen [10]. The supply voltage could be boosted to 4 × VDD while the voltage of each node is restricted in safe margin. Furthermore, for better reliability and better efficiency, a stacked double gate input structure is adopted. The wideband output matching is achieved by using an artificial transmission line together with a coupling strengthened transformer. Thus the proposed PA achieved >19.5dBm peak output power and >40% peak PA drain efficiency.

D. Design of Stacked LNA in RXFE and the BB PS

The proposed LNA shown in Fig.6 is based on the two-stage stacked LNA topology. The constant gm bias circuit prevents the overvoltage risk of the core transistors and ensures better PVT consistency. In the stacked LNA, a more relaxed voltage margin can reduce thermal noise and improve the gain. Therefore, the requirement for the quality factor of the load inductance could been lowered, thereby reducing the area consumption and unwanted mutual inductance coupling. The weakly coupled inductors connecting the gates and the sources of the input transistors are designed with an 8-shaped configuration. Here, considering the noise optimization and wideband matching,

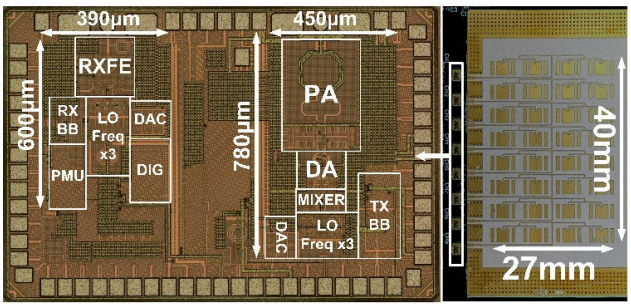


Fig. 7. Die micrograph of the TRX and the 1×8 phased array.

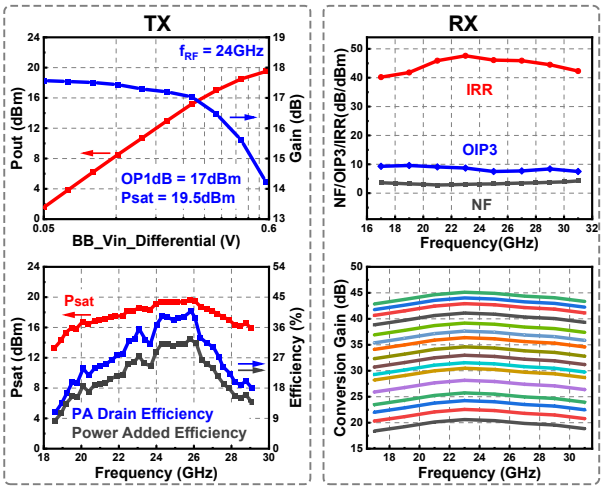


Fig. 8. Measured TX performances of gain, saturation power, drain efficiency and power added efficiency. Measured RX performances of noise figure, image rejection ratio, linearity and conversion gain.

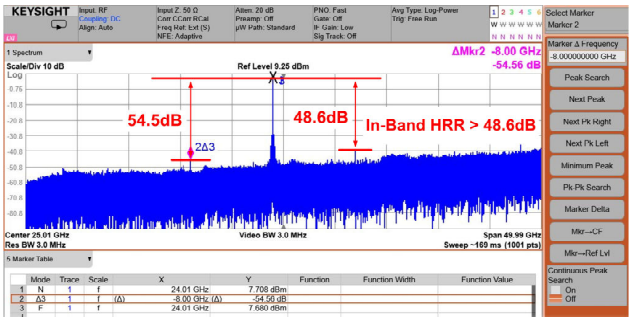
K = 0.1 is adopted for inductor co-design [11]. The PGA-style BB PS based on programmable resistors and quadrant-select switches is adopted in this TRX because it exhibits low accuracy variation in different RF bands due to the constant baseband frequencies [7].

III. Measurement Results

The proposed TRX is fabricated in 22nm CMOS process. Fig. 7 shows the photo of the TRX and the phased array system. The core areas of TX and RX are only 0.36mm^2 and 0.23mm^2, respectively.

Fig. 8 presents the measured key performance of the transceiver with the GSG probe. At 24GHz, the OP1dB/ Psat of the TX are 17dBm/19.5dBm. Within the 3dB bandwidth of 20-28.5GHz, the TX achieves a peak Psat of 19.84dBm, a peak PA drain efficiency of 40.2% and a peak power added efficiency of 32.5%. The RX covers 17-31GHz, and the noise figures (NF) are 4.0/3.2/3.7/4.5dB at 17/21/25/31GHz. In the maximum gain mode, the achieved out-of-band OIP3 is over 7.5dBm and the measured image rejection ratio (IRR) is over 40dB. The RX provides a programmable conversion gain of 18-45 dB and the gain fluctuation is less than 2.4dB.

As shown in Fig.9, the HRR of tripled LO is higher than 48.6dB at 24GHz. The LO calibration can improve the worst HRR from 33dB to 41dB and lower the standard deviations by an average of 1.4dB in multi-chip measurements. In Fig.10, the LO tripler operated at 21/24/27GHz shows a phase noise of -130/-129.3/-129.9 dBc/Hz at 10MHz offset and an integrated RMS jitter better than 28fs, showing the



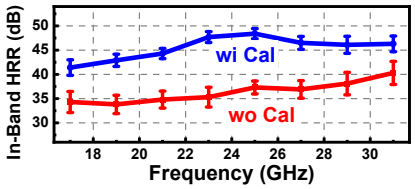


Fig. 9. Measured LO HRR at 24GHz and its variation with frequency.

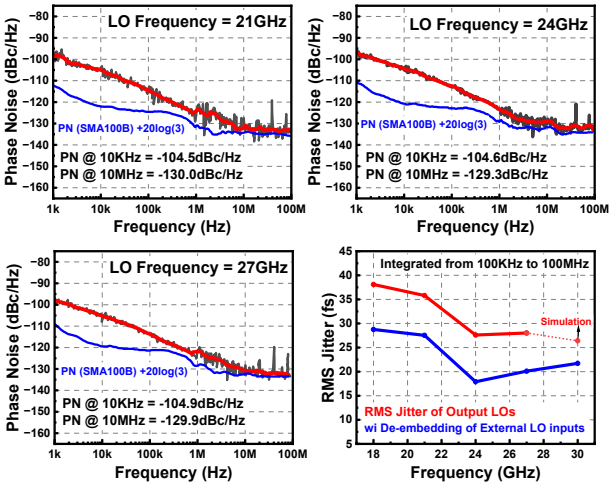


Fig. 10. Measured phase noise and integrated RMS jitter of LOs.

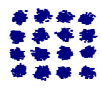
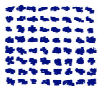
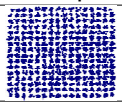
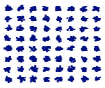
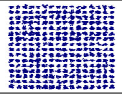
TX Modulation	16-QAM	64-QAM	256-QAM
Data Rate	160Mbps	240Mbps	320Mbps
Constellation			
EVM	8.2% (-21.7dB)	5.5% (-25.2dB)	3.3% (-29.6dB)
RX Modulation	16-QAM	64-QAM	256-QAM
Data Rate	160Mbps	240Mbps	320Mbps
Constellation			
EVM	5.2% (-25.7dB)	3.4% (-29.3dB)	2.6% (-31.7dB)

Fig. 11. Measured un-calibrated EVM constellations at 24GHz.

excellent phase noise performance of the proposed LO frequency multiplication architecture.

During EVM measurements, with 16/64/256-QAM 40MS/s signal inputs, the measured EVMs of the TX are -21.7/-25.2/-29.6dB at 24GHz without FIR compensation, while the measured EVMs of the proposed RX are -25.7/-29.3/-31.7dB, as shown in Fig.11.

As shown in Fig. 12(a), the phase shifter exhibits a precision of 1.4° with a <0.43° RMS phase error at 40MHz

TABLE I. Comparison with state-of-the-art K/Ka band transceivers

Parameters	JSSC 26[2]	ISSCC 25 [3]	VLSI 22 [4]	ASSCC 24 [6]	CICC 25[7]	This work
Technology	65nm	65nm	65nm	55nm	40nm	22nm
Integration	TX, RX	TRX FE	TRX FE	TX, RX	RX	TRX
Core Area	5.2 mm^2	1.06 mm^2	0.2 mm^2	3.3/1.8 mm^2	0.9 mm^2	0.59 mm^2
Phased Array	-	-	-	-	-	√
RF BW (GHz)	RX 17-21, TX 27-31	17.7-29.5	25.8-39.2	15-40[a]	18-40[a]	RX 17-31, TX 20-28.5
TX Psat (dBm)	15.4[b]	20.5	16.5	15.4	-	19.84
PAE max (%)	-	21.8	18	-	-	32.5
RX Power (mW)	141	48.7	45	< 135	< 113	59-71
NF (dB)	< 6.4	< 5	< 5.6	< 5.4	< 6.9	3.2-4.3
RX Gain (dB)	35.7	25	19.2	24-40	28-47	18-45
LO Jitter (fs)	-	-	-	-	33[c]	18[d]

(a) RF Channel II of the TRX. (b) Only OP1dB is provided. Measured Jitter at (c) 20GHz and (d) 24GHz with de-embedding of inputs.

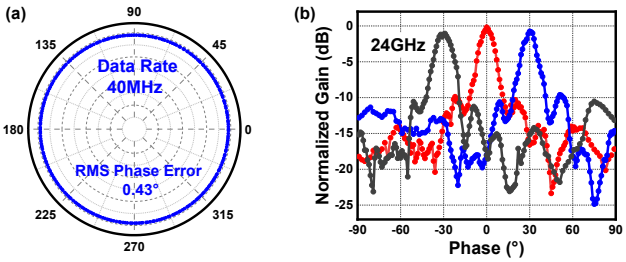


Fig. 12. Measured results of the (a) phase shifter and (b) the phased-array.

and it is stable in different RF bands because the operating frequency of the BB PS is constant. A 1 × 8 phased array demonstration is designed with a 22-32GHz wideband antenna array, as shown in Fig. 7. The TRX beam patterns with -30°, 0°, and 30° incidence angles at 24GHz after SPI-controlled calibration are shown in Fig. 12(b), which demonstrate the suitability for phased array systems.

Table I compares the proposed TRX with recently published state-of-the-art TRXs. The proposed TRX is competitive in the die area, the TX drain efficiency, the RX NF, the LO phase noise, and the re-configurability for phased-array among them.

IV. Conclusion

A compact K/Ka band transceiver that integrated a 3-phase edge-combining based frequency tripler is introduced in this work. Because of the switched-capacitor based phase interpolator and the edge-combiner, the LO chain could output 17-31GHz quadrate signals while operating within 5.6-10.4GHz. Moreover, with the assistance of the class-D edge combiner and the auto calibration scheme, this system greatly strengthen the HRR and simplifies the calibration procedure. Besides, stacked PA improves the Psat and the LNA lowers the load Q requirements to avoid the extra die area costs. The TX measures a peak Psat of 19.84dBm and a peak drain efficiency of 40.2% within the 3dB bandwidth of 20-28.5GHz. The RX measures a maximum gain of 45dB and a minimum noise figure of 3.2dB within 17-31GHz. Besides, the reconfigurable TRX and integrated phased shifter provides the suitability for phased-array demonstration. Overall, these merits make the transceiver very suitable for K/Ka band phased-array applications.

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