A 0.025 mm² 1.45 pJ/cycle RC Oscillator with V_{GS}-ratio-based Temperature Compensation Achieving 44.3 ppm/°C from -40 °C to 150 °C

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***Abstract*—This paper presents a compact closed-loop RC oscillator architecture, utilizing a V_{GS}-ratio technique to cancel the first-order temperature coefficient (TC). Additionally, current compensation is proposed to further extend the operating temperature range. Fabricated in a 0.18 µm CMOS process, the design occupies an area of only 0.025 mm². The output frequency is 21.2 MHz while consuming 30.8 µW, resulting in an energy efficiency of 1.45 pJ/cycle. An average TC of 44.3 ppm/°C is obtained over a wide temperature range from −40 °C to 150 °C. Moreover, the temperature compensation technique does not require resistors with complementary TCs, which greatly enhances design flexibility and process compatibility.**

Keywords*—CMOS, RC frequency reference, frequency-locked loop (FLL), V_{GS}-ratio, temperature compensation, AEC-Q100 Grade

I. Introduction

Recently, automotive and industrial systems require timing signals with much wider temperature resilience than consumer electronics, as specified by AEC-Q100 Grade 0 (−40 °C to 150 °C). RC oscillators have become increasingly attractive for generating on-chip frequency references due to their area and power efficiency. Open-loop RC oscillators [1–5] are often favored for their simplicity, but they are vulnerable to comparator offset and delay variations over temperature, resulting in relatively large TCs (>100 ppm/°C) [1,2]. R–RC architecture [3] and additional calibration loop [4,5] offer effective TC reduction; the former increases design and trimming complexity, while the latter degrades energy efficiency (>10 pJ/cycle). In contrast, closed-loop RC oscillators [6-10] with frequency-locked loops (FLLs) achieve better process-voltage-temperature (PVT) stability, though at the cost of larger area (>0.1 mm²) [6-8] or higher energy consumption (>4 pJ/cycle) [6,9,10]. Delta-sigma modulation techniques, applied to polynomial calibration [6] or switched-resistor configurations [7,8], can effectively reduce temperature dependence but often require two-point trimming. In addition, BJT-based second-order TC compensation [10] demands a higher supply voltage that increases power consumption. Therefore, despite various compensation techniques, meeting both high energy efficiency and a wide temperature range remains a significant challenge.

This work adopts a compact closed-loop RC oscillator architecture, utilizing a V_{GS}-ratio technique to cancel the first-order TC. Additionally, current compensation is proposed to further extend the operating temperature range. Fabricated in a 0.18 µm CMOS process, the design occupies an area of only 0.025 mm² and delivers an output frequency of 21.2 MHz while consuming 30.8 µW, resulting in an energy efficiency of 1.45 pJ/cycle. A TC of 44.3 ppm/°C is obtained over a wide temperature range from –40 °C to 150 °C. Moreover, the temperature compensation technique does not require resistors with complementary TCs, which greatly enhances design flexibility and process compatibility.

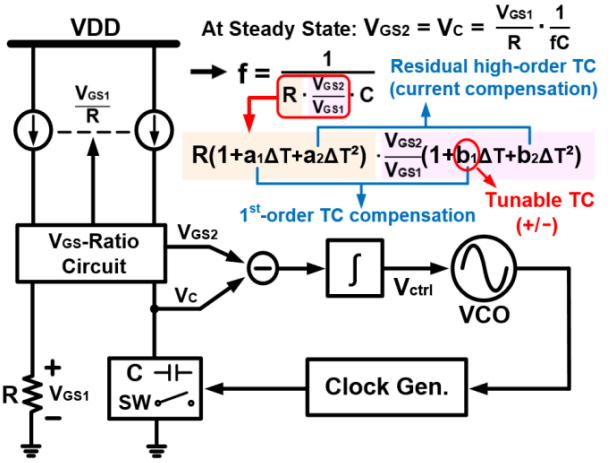

Fig. 1: Block diagram and temperature compensation principle of the proposed RC frequency reference.

II. Proposed Circuit Design

A. Architecture of Proposed RC Oscillator

Fig. 1 presents the architecture of the proposed RC oscillator, which incorporates a p-poly resistor (R = 700 kΩ) and a V_{GS}-ratio circuit for generating both the current source ($I = V_{GS1}/R$) and the reference voltage V_{GS2}. The current charges a switched-capacitor circuit with a capacitance of 1 pF, resulting in the voltage V_C. The difference between V_{GS2} and V_C is integrated to produce the control voltage V_{ctrl}, which regulates the output frequency of the voltage-controlled oscillator (VCO). The clock generator following the VCO manipulates the operational frequency of the switched-capacitor circuit to keep V_C equal to V_{GS2}. Under the operation of FLL, the output frequency can be expressed as :

$$f = \frac{1}{R \cdot \frac{V_{GS2}}{V_{GS1}} \cdot C} \quad (1)$$

The temperature dependence of the FLL is compensated by the combined TCs of the resistor R and the V_{GS}-ratio, expanded as:

$$R(1 + a_1\Delta T + a_2\Delta T^2)\frac{V_{GS2}}{V_{GS1}}(1 + b_1\Delta T + b_2\Delta T^2) \quad (2)$$

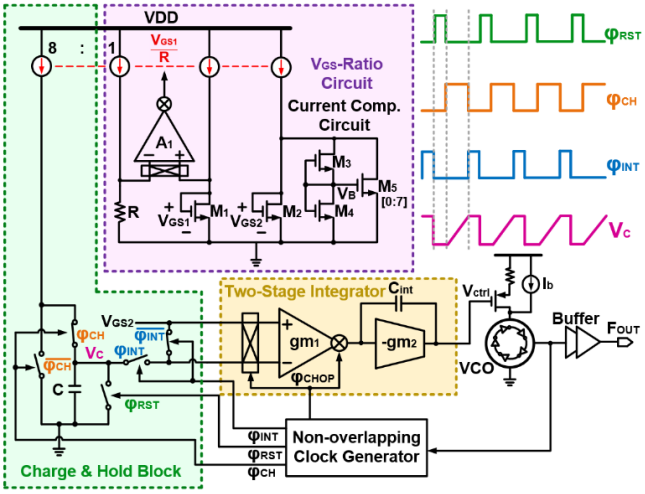

Fig. 2: Circuit diagram and timing waveforms.

where a_1, b_1 , a_2 , b_2 correspond to the first and second-order TC of resistor and V_{GS}-ratio. Notably, b_1 can be adjusted to be either positive or negative by designing transistor sizes to cancel a_1 [11]. This relaxes the constraints on resistor selection and improves immunity to process-induced mismatches compared with dual-resistor implementations [5-9]. Moreover, the residual high-order TC can be removed through the current compensation associated with the V_{GS}-ratio circuit.

B. V_{GS}-Ratio Circuit and Current Compensation

Fig. 2 illustrates the detailed circuit implementation along with the corresponding clock timing waveforms. In the V_{GS}-ratio circuit, the resistor R and diode-connected transistor M_1 are connected to the inverting and non-inverting inputs of amplifier A1, respectively, to establish a stable current of approximately V_{GS1}/R (~ 500 nA). This current is mirrored to M_2 to generate V_{GS2}. The current mirror is designed with long-channel transistors to further suppress flicker noise and channel-length modulation, ensuring that both V_{GS1} and V_{GS2} remain robust against supply fluctuations. Note that M_1 and M_2 are in the subthreshold region for power saving. Accordingly, the TC of the V_{GS}-ratio can be expressed as:

$$\frac{\partial}{\partial T}\frac{V_{GS2}}{V_{GS1}} \propto ln\left(\frac{I_{D2}}{I_{D1}}\frac{W_1L_2}{W_2L_1}\right) \quad (3)$$

indicating that it can be tailored by adjusting the aspect ratios of M_1 and M_2. For this design, M_1 and M_2 are sized with an aspect ratio of 5:3. The resulting V_{GS}-ratio yields a positive TC (~ +280 ppm/°C), which compensates for the negative TC of the p-poly resistor to the first order.

To further reduce the overall TC and extend the operating temperature range, two stacked transistors M_3 and M_4, together with M_5, are introduced for high-temperature current compensation [12]. M_3–M_4 generate a proportional-to-absolute-temperature (PTAT) voltage $V_B \propto V_T \ln\left(\frac{W_3L_4}{L_3W_4}\right)$ that biases M_5. Since M_3 is reversely biased, it exhibits a much higher impedance than the diode-connected M_4. Therefore, V_B is less influenced by V_{GS2}. Consequently, the gate bias applied to M_5 is stably maintained, ensuring accurate current extraction. Owing to the temperature dependence of V_B, the current of M_5 increases rapidly with temperature, which in turn reduces V_{GS2} and counteracts the decrease of output frequency. To mitigate process variations, a 3-bit trimming scheme is employed to fine-tune the amount of compensation current.

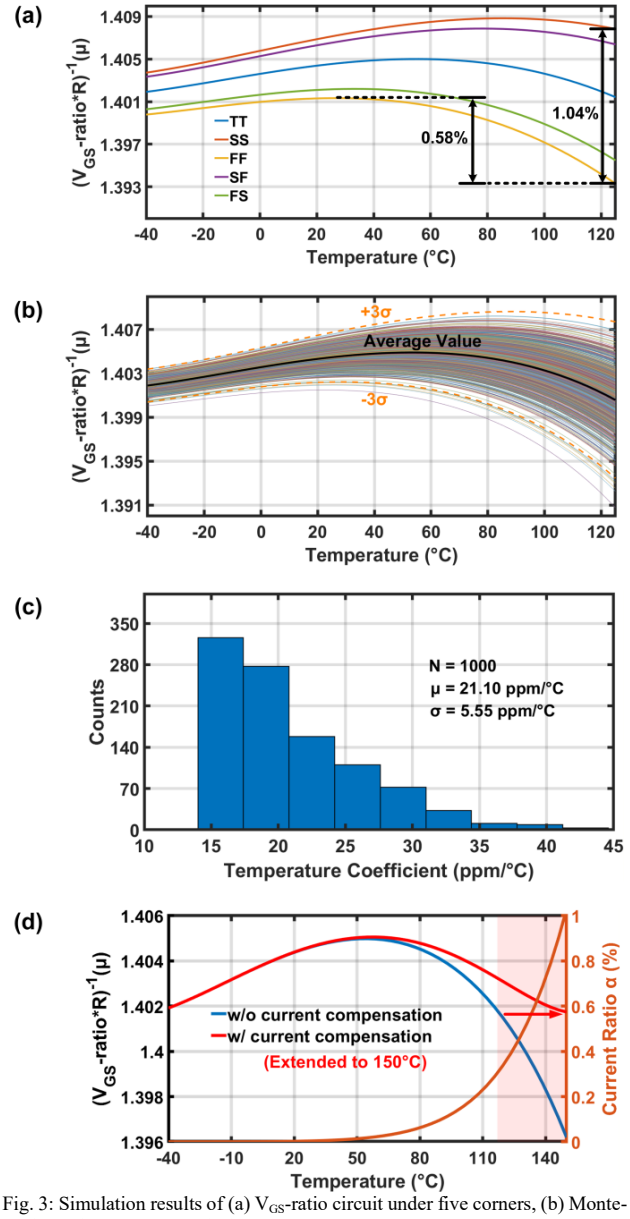

Fig. 3: Simulation results of (a) V_{GS}-ratio circuit under five corners, (b) Monte-Carlo analysis, (c) TC and (d) current compensation.

Fig. 3 shows the simulated results of the reciprocal of the product of the V_{GS}-ratio and the resistance R under five process corners, along with the Monte-Carlo simulation results. If there is no drift in the nominal value of the resistor, the largest temperature variation is 0.58% at the FF corner, and the corner variation gradually increases with temperature, reaching a maximum of 1.04% at 125 °C, which corresponds to a 3σ-to-mean ratio of 0.51%. The TC distribution obtained from 1000 samples has a mean value of 21.1 ppm/°C and a standard deviation σ of 5.5 ppm/°C, remaining well-behaved against

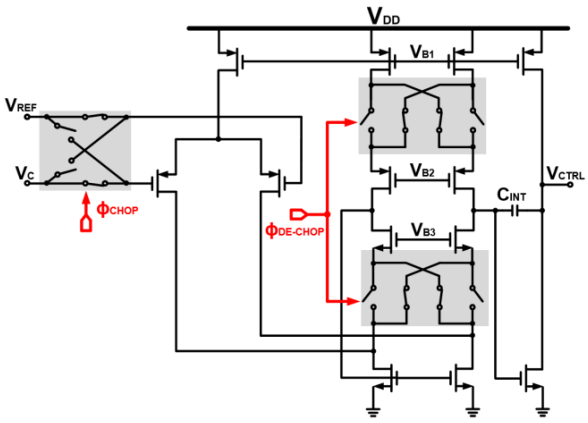

Fig. 4. Schematic of integrator

process variations and device mismatch. Furthermore, the effectiveness of current compensation for high temperature range extension and TC improvement is demonstrated. Here, α denotes the ratio of the compensation current to the main current V_{GS1}/R. With compensation, the high-temperature degradation is mitigated, and the temperature stability is enhanced to 150 °C.

C. FLL Timing Operation and Circuit Implementation

The operation of the proposed FLL is defined by a three-phase timing scheme [9] , based on which the generation of V_C and the implementation of the loop circuits are described as follows. First, when ϕ_{RST} is high, the top plate of the capacitor and the current source output are connected to ground, discharging the capacitor. Next, when ϕ_{CH} is high, the current source is connected to the top plate, charging it with a controlled current (4 μA), mirrored by an 8:1 ratio from V_{GS1}/R. Finally, when ϕ_{INT} is high, the voltage difference between V_C and V_{GS2} is processed by the integrator. To generate the three required clock phases, a 4:1 clock divider is inserted between the VCO output and the phase-generation circuit. The duration of ϕ_{CH} is designed to be twice that of ϕ_{RST} and ϕ_{INT}, thereby reducing the impact of clock propagation delay on the charging time and minimizing the resulting timing error. Based on this timing operation, a two-stage chopped integrator, as shown in Fig. 4, is employed to achieve high DC loop gain, effectively suppressing the temperature and supply sensitivity of the VCO. To reduce 1/f noise and input offset, chopping is applied to the first stage of the integrator, which also enhances the long-term stability of the output frequency. The chopping signal ϕ_{CHOP} is generated by dividing the output frequency F_{OUT} by 64, and the resulting ripple is effectively attenuated by C_{int} at the second stage acting as a low-pass filter. In addition, the VCO is implemented using a current-starved five-stage ring oscillator with resistor degeneration. For reliable startup from zero-current conditions, a small bias current ($I_b \approx 100$nA) is provided to the VCO.

III. Measurement Results

The RC frequency reference was fabricated using a 0.18 μm CMOS process. Fig. 5 shows the chip micrograph. The design has a core area of 0.025 mm². For temperature characterization, one chip was tested across a temperature range from −40 °C to 150 °C to determine the optimal trimming code for temperature extension. Subsequently, the 3-bit trimming codes were applied

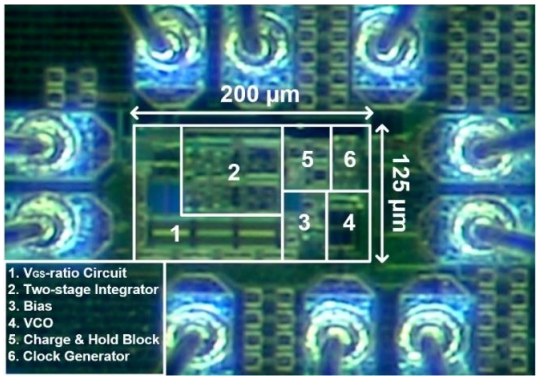

Fig. 5. Chip micrograph.

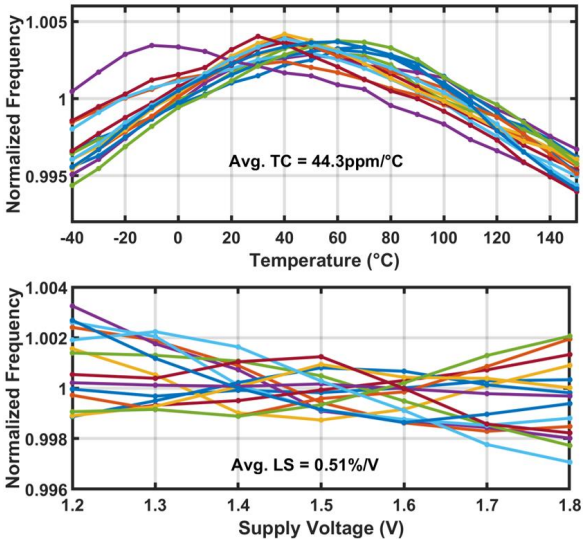

Fig. 6. Normalized measured frequency from 15 samples over temperature (top) and supply voltage (bottom).

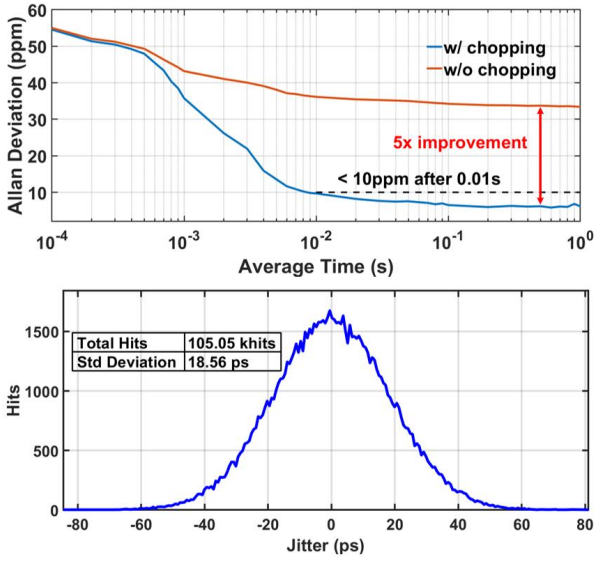

Fig. 7. Measured Allan deviation (top) and period jitter (bottom).

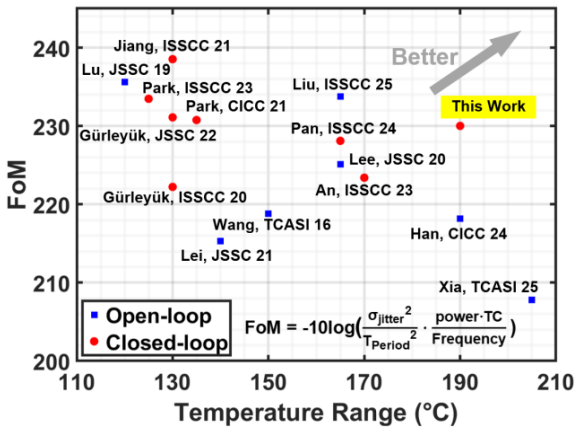

Fig. 8: Benchmarks with recently reported state-of-the-art RC oscillators.

to other chips prior to measurement. Fig. 6 illustrates the measured performance of 15 samples over temperature and supply voltage. At 25 °C, the average output frequency is 21.2 MHz, and the average TC is 44.3 ppm/°C across the −40 °C to 150 °C range. The line sensitivity (LS) over a supply voltage range of 1.2 V to 1.8 V is 0.51 %/V. The average power consumption at 1.5 V is 30.8 µW, corresponding to an energy efficiency of 1.45 pJ/cycle. Fig. 7 presents the measurement results of Allan deviation and period jitter. The Allan deviation for a 0.5s-stride is 34 ppm without chopping and improves to 7 ppm with chopping. The measured output jitter is 18.6 ps_{rms} (394 ppm). Additionally, the measured output frequency settling time is about 150 µs.

Table I summarizes the performance metrics of the proposed oscillator in comparison with those of previously reported state-of-the-art RC oscillators. Compared with [4], which has similar TC in a comparable temperature range, this design demonstrates nearly a 10x improvement in energy efficiency. Moreover, it achieves the widest operating temperature range among designs with comparable figures of merit (FoM > 230). Fig. 8 provides a benchmark comparison.

IV. Conclusion

This work presents an FLL-based RC oscillator for low-power systems requiring a stable clock reference over a wide temperature range. By employing a closed-loop architecture, the proposed design suppresses the effects of PVT variations, such that the output frequency is primarily determined by the front-end RC time constant. A V_{GS}-ratio-based first-order temperature-compensation technique, together with a high-temperature current-compensation scheme, is adopted to improve temperature stability and extend the operating range. Fabricated in a 0.18-µm CMOS process, the prototype occupies 0.025 mm² and achieves an average TC of 44.3 ppm/°C from -40 °C to 150 °C with an energy efficiency of 1.45 pJ/cycle. These results demonstrate that the proposed oscillator is well suited for IoT, industrial, and automotive applications requiring a compact and energy-efficient wide-temperature-range clock reference.

TABLE I. Performance Summary and Comparison to State-of-the-Art.

Reference	JSSC 2020 [1]	ISSCC 2022 [3]	CICC 2024 [4]	ISSCC 2023 [9]	ISSCC 2024 [10]	This Work
Technology (nm)	180	180	180	180	180	180
Architecture	Open Loop			Closed Loop		
Resistor Type (No.)	N/A (1)	P/S-Poly N-Well (3)	N/A	P/N-Poly (2)	N-Well (1)	P-Poly (1)
Frequency (MHz)	10.5	2.3	16	10	32	21.2
Supply Voltage (V)	1.4	1.6	5	1.5	1.8	1.5
Power (µW)	219.8	7.6	405	85.1	131	30.8
Energy (pJ/cycle)	20.9	3.3	25.31	8.5	4.1	1.45
Temp. Range (°C)	-40~125 (165)	-40~125 (165)	-40~150 (190)	-45~125 (170)	-40~125 (165)	-40~150 (190)
Temp. Coeff. (ppm/°C)	116[a]	7.93[a]	25.6[a]	31.5[b]	10.6[b]	44.3[a]
Supply Range (V)	1.4~2.0	1.3~2.0	4.5~5.5	1.5~1.8	1.7~2.0	1.2~1.8
Supply Sensitivity (%/V)	4.4	0.51	0.26	0.9	0.3	0.51
Period Jitter (ps_{rms})	9.86 (104ppm)	N/A	30.23 (484ppm)	41.3 (413ppm)	18.7 (598ppm)	18.6 (394ppm)
Allan Deviation (ppm)	2.8	9	N/A	2.3	18.8	7
Calibration Points	0	2	0	1+batch	2	1+batch
Samples	15	11	280	112	28	15
Area (mm²)	0.015	0.07	0.086	0.01	0.028	0.025
FoM	225.1	N/A	218.2	223.4	228.1	230

$FoM = -10\log\left(\frac{\sigma_{Jitter}^2}{T_{Period}^2} \cdot \frac{Power \cdot TC}{Frequency}\right)$ [a] average value [b] box method

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