Sub-5 ns Vertical ECRAM Enabled by Sm-Doped CeO_2: 64×64 Cross-Point Array and Tiki-Taka Training for M3D a-PIM

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***Abstract*—We demonstrate a high-speed switching vertical electrochemical random-access memory (HSV-ECRAM) achieving sub-5 ns switching, enabled by a high ionic conductivity Sm-doped CeO_2 electrolyte (~10^6 times higher than conventional HfO_2) and an ultra-thin vertical channel (< 20nm). The proposed HSV-ECRAM exhibits large conductance modulation (ΔG > 8,000), together with a near-linear switching energy per conductance change (E/ΔG) scaling trend with device area reduction, reaching ~10^{-4} J/S. Furthermore, a 64×64 cross-point array is fabricated, showing conductance modulation with 100% device yield across selected rows of the array. Finally, we experimentally demonstrate array-level training using Tiki-Taka algorithm, showing that HSV-ECRAM devices can be used for both core and auxiliary arrays and highlighting their potential for high-performance analog processing-in-memory applications.**

***Keywords*—Electrochemical Random-Access Memory, Sm-doped CeO_2, Vertical Cross-Point Array, Analog In-Memory Computing, High-Speed Switching.**

I. Introduction

Cross-point array (CPA)-based resistive processing unit accelerators have attracted considerable attention for analog processing-in-memory (a-PIM), as they enable highly parallel vector-matrix multiplication and vector-vector outer-product operations for deep neural network training [1]–[3]. For monolithic three-dimensional (M3D) integration with reduced area overhead and increased bandwidth in high-performance a-PIM systems [4], vertical CPA architectures are particularly attractive, as shown in **Fig. 1(a)**.

Among various a-PIM device candidates, metal-oxide-based electrochemical random-access memory (MO-ECRAM), which allows separate read and write operations, is a promising analog synaptic device for a-PIM because of its favorable analog synaptic characteristics, including symmetry, linearity, and low cycle-to-cycle variation [5], [6]. MO-ECRAM also supports vertical device structures and CPA architectures, making it suitable for M3D-stackable vertical CPAs [7], [8]. However, its switching speed is still limited by slow ion dynamics. To address this limitation, various materials such as bismuth vanadate and ceria have been investigated [9], [10]. Nevertheless, achieving the switching speed required for high-performance a-PIM remains a major challenge (**Fig. 1(b)**).

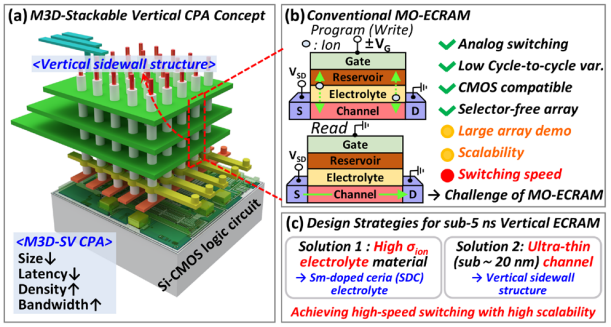

Fig. 1. (a) Schematic illustration of an M3D-stackable vertical cross-point array (M3D-SV CPA) integrating MO-ECRAM devices on Si-CMOS logic circuits for a-PIM applications. (b) Operation principle, advantages, and limitations of conventional MO-ECRAM. (c) Proposed design strategies for achieving high-speed switching with high scalability in MO-ECRAM.

In this study, we propose two key strategies: (1) using a Sm-doped CeO_2 (SDC) electrolyte with high ionic conductivity and (2) adopting a vertical structure with an ultra-thin channel to enhance conductance modulation, as shown in **Fig. 1(c)**. SDC has been reported to exhibit high oxygen ionic conductivity [11], making it a promising electrolyte candidate for accelerating ion transport in ECRAM. Based on these strategies, we develop a high-speed vertical ECRAM (HSV-ECRAM) featuring an SDC electrolyte and an ultra-thin channel, and demonstrate sub-5 ns switching together with enhanced conductance modulation and improved energy efficiency compared to ECRAM with a conventional HfO_2 electrolyte. Furthermore, we fabricate a 64×64 CPA and experimentally demonstrate array-level neural network training using the Tiki-Taka version 1 (TTv1) algorithm. These results indicate the potential of HSV-ECRAM for scalable, high-performance a-PIM applications.

II. Structural and Compositional Analysis

Fig. 2 shows the fabrication process of the HSV-ECRAM cross-point array. A pre-patterned wafer is first prepared by forming Ti/TiN/W drain and source lines with Si_3N_4 insulating layers, followed by via-hole and contact pad etching (**Fig. 2(a)–(d)**). The WO_x/SDC/WO_x stack is then deposited into the via-holes by reactive sputtering at room temperature (RT), and W gate lines are subsequently formed to complete the cross-point array architecture (**Fig. 2(e)–(f)**). **Fig. 3(a)** shows an optical micrograph (OM) of the HSV-ECRAM device.

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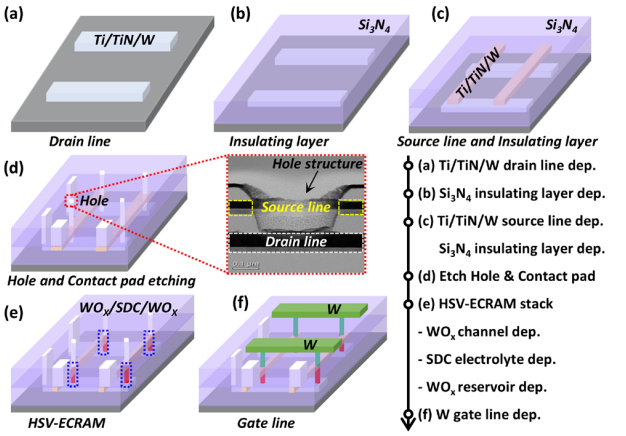

Fig. 2. Fabrication process of HSV-ECRAM cross-point array: (a)-(d) pre-patterned wafer fabrication including drain/source lines, insulating layers, and hole etching, followed by (e) HSV-ECRAM stack deposition and (f) gate line formation.

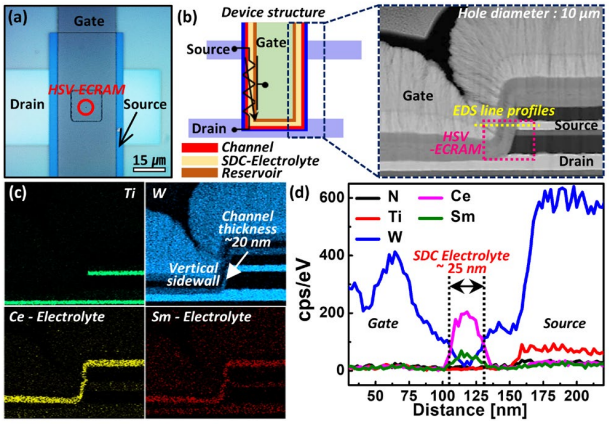

Fig. 3. (a) Optical micrograph of HSV-ECRAM. (b) Device structure schematic and cross-sectional TEM image of HSV-ECRAM in the via-hole region. (c) EDS elemental mapping showing an ultra-thin WO_x channel and uniform SDC electrolyte distribution. (d) EDS line profiles across the device region, showing distinct Ce and Sm signals.

Fig. 3(b) presents the device structure schematic and a cross-sectional TEM image, confirming the formation of a vertical sidewall channel inside the via-hole. **Fig. 3(c)–(d)** show EDS elemental mapping and line profiles, indicating the formation of ultra-thin vertical WO_x channel (<20 nm) and uniform SDC electrolyte distribution (<25 nm) along the via-hole sidewall, with distinct Ce and Sm signals. These results support the structural compatibility of HSV-ECRAM with M3D-stackable CPA architectures.

III. Impact of SDC Electrolyte on HSV-ECRAM

Fig. 4(a) shows that sputtered SDC exhibits approximately 10^6 times higher ionic conductivity than HfO_2 at RT, following a clear Arrhenius-type behavior. **Fig. 4(b)** presents simulated oxygen vacancy concentration profiles under varying potentiation conditions, showing increased vacancy accumulation at the channel-electrolyte interface with higher ionic conductivity. **Fig. 4(c)** shows ramp-time-dependent channel conductance modulation with enhanced counterclockwise hysteresis during gate-voltage sweep, while **Fig. 4(d)** presents the corresponding gate current-voltage behavior exhibiting clockwise hysteresis, indicating ion-driven switching [12]. This behavior is attributed to the

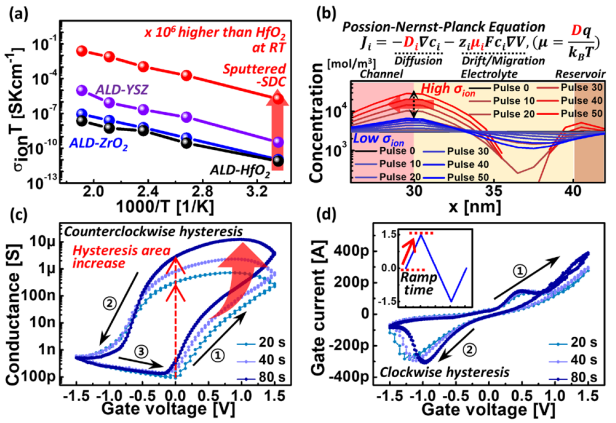

Fig. 4. (a) Arrhenius plot of ionic conductivity for various oxide electrolytes. (b) Simulated oxygen vacancy concentration profiles under varying potentiation conditions. (c) Ramp-time-dependent conductance modulation during gate-voltage sweep. (d) Corresponding gate current-voltage characteristics

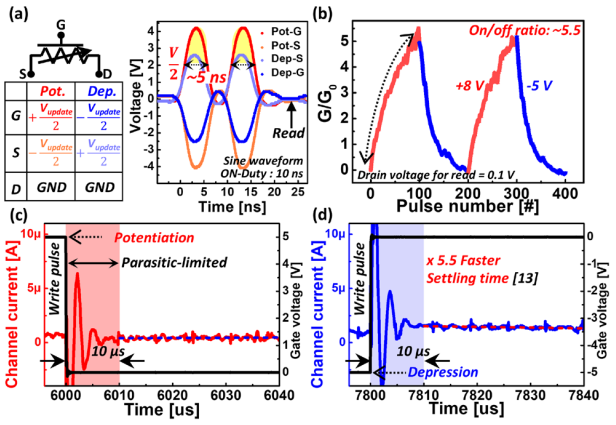

Fig. 5. (a) Half-bias scheme and applied sine-wave update pulse with a 10 ns ON-duty. (b) Repeatable sub-5 ns switching with an on/off ratio exceeding 5. (c)-(d) Transient channel current response in HSV-ECRAM during read operations immediately after a write pulse, showing rapid settling within 10 μs.

sufficient time allowed for ion transport, consistent with the simulation results in **Fig. 4(b)**.

Fig. 5(a) illustrates the half-bias (HB) programming scheme in HSV-ECRAM and the applied sine-wave update pulse with a 10 ns ON-duty, where the pulse width at half amplitude is ~5 ns. In the HB scheme, opposite-polarity half voltages are applied to the gate and source, with positive gate/negative source bias for potentiation and negative gate/positive source bias for depression, while the drain is grounded. **Fig. 5(b)** shows repeatable sub–5 ns switching with an on/off ratio exceeding 5 under +8/–5 V sine-wave pulses. Furthermore, **Fig. 5(c)–(d)** show the transient channel current response during read operations immediately following a ±5 V write pulse, showing rapid settling time within 10 us. This is 5.5 times faster than HfO_2-based ECRAM reported in [13], although the transient response is still affected by parasitic components such as electrode overlap.

Fig. 6(a) shows stable endurance characteristics for 70 cycles, corresponding to a total of 1.4×10^5 up/down pulses applied at +5/–4 V with a pulse width of 25 μs. Consistent switching behavior is observed in both the initial and final five cycles. **Fig. 6(b)** shows low cycle-to-cycle variation,

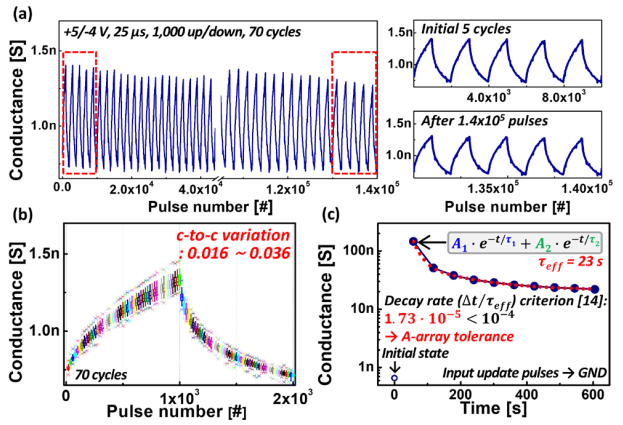

Fig. 6. (a) Endurance characteristics for 70 cycles (1.4×10^5 pulses). (b) c-to-c variation for 70 cycles. (c) Time-dependent conductance relaxation satisfying the auxiliary (A)-array tolerance criterion of Tiki-Taka (TT) algorithm.

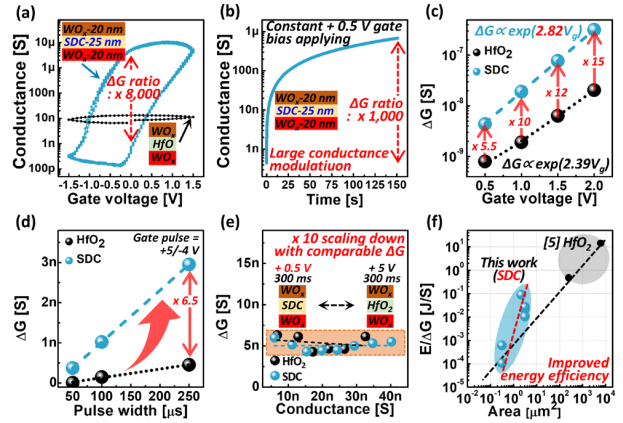

Fig. 7. (a) Conductance modulation of V-ECRAMs with different electrolyte stacks during gate-voltage sweep. (b) Conductance modulation of HSV-ECRAM under a constant gate bias of +0.5V. (c)–(d) ΔG of HSV-ECRAM under different pulse amplitudes and widths. (e) Comparable ΔG under identical pulse widths with a 10× reduction in gate voltage. (f) Switching energy per conductance change (E/ΔG) as a function of device area, showing improved energy efficiency of HSV-ECRAM.

with a coefficient of variation (σ/μ) of 0.016–0.036 across all 70 cycles. **Fig. 6(c)** presents time-dependent conductance relaxation fitted with an effective time constant (τ_{eff} = 23 s), resulting in a decay rate ($\Delta t/\tau_{eff} = 1.73\times10^{-5}$), which satisfies the auxiliary (A)-array tolerance criterion of the Tiki-Taka version 1 (TTv1) algorithm. In the TTv1 algorithm, the A-array is used to accumulate weight updates, while the core (C)-array is used for inference. Therefore, the this relaxation behavior satisfies the A-array tolerance criterion for successful training [14], [15], supporting the use of HSV-ECRAM in TTv1-based training.

Fig. 7(a) compares the conductance modulation of V-ECRAMs with different electrolyte stacks, where the HSV-ECRAM with an SDC electrolyte and an ultra-thin channel achieves a large conductance change (ΔG > 8,000). **Fig. 7(b)** shows an on/off ratio exceeding 1,000 under a low gate bias of +0.5 V applied for 150 s. **Fig. 7(c)–(d)** present ΔG of HSV-ECRAM under different pulse amplitudes and widths, revealing up to a ~15× improvement compared to HfO_2-based V-ECRAM, attributed to the high ionic conductivity of the SDC electrolyte. **Fig. 7(e)** shows that comparable ΔG is maintained even with a tenfold reduction in gate voltage. under an identical pulse width of 300 ms.

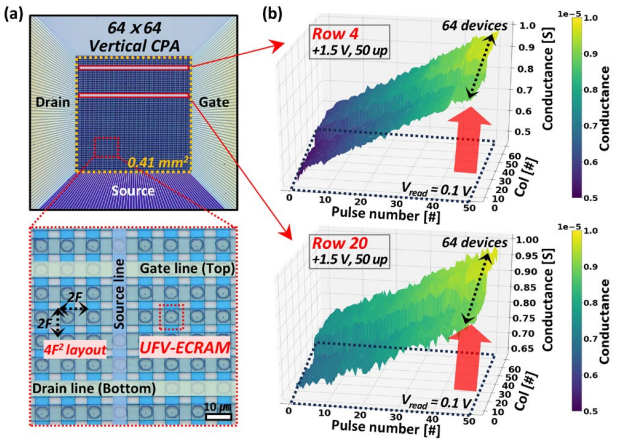

Fig. 8. (a) Optical micrograph of the fabricated 64×64 HSV-ECRAM cross-point array, with a compact $4F^2$ layout. (b) Large-scale array-level conductance modulation across all 64 devices in two selected rows, showing highly consistent responses

Fig. 7(f) presents the switching energy per conductance change (E/ΔG), showing a near-linear scaling trend with device area reduction and values down to 10^{-4} J/S. These results suggest that the proposed HSV-ECRAM can achieve both large conductance modulation and low-voltage operation while maintaining favorable energy scaling with continued device scaling.

IV. HSV-ECRAM Cross-Point Array Demonstration

Fig. 8(a) shows an OM image of the fabricated 64×64 HSV-ECRAM cross-point array with a compact $4F^2$ layout, demonstrating the large-scale integration capability of the proposed vertical CPA architecture. **Fig. 8(b)** presents large-scale array-level conductance modulation across all 64 devices in two selected rows, achieving 100% functional yield under programming pulses of +1.5 V for 30 ms and read pulses of +0.1 V for 10 µs. The highly consistent conductance modulation across the selected rows confirms uniform update behavior over the corresponding column devices, supporting the scalability of HSV-ECRAM for large-scale array-level operation.

Fig. 9(a) shows the measurement setup for precise electrical characterization using external instruments and a specially designed 64×64 HSV-ECRAM cross-point array layout with contact pads for each source line (SL), drain line (DL), and gate line (GL). **Fig. 9(b)** shows conductance modulation of all 64 devices with 100% functional yield. To validate the array-level training capability of the HSV-ECRAM cross-point array, **Fig. 9(c)** presents experimental neural network training results, showing that HSV-ECRAM devices can operate in both core (C)-array for inference and auxiliary (A)-array for weight-update accumulation in the TTv1 algorithm.

Fig. 9(d) compares minimum pulse width and on/off ratio, showing that HSV-ECRAM approaches the ideal a-PIM device region with both short update pulse width and sufficient on/off ratio. Together, these results demonstrate that HSV-ECRAM satisfies the key device requirements for practical array-level training, including uniform conductance update, compatibility with both inference and weight-update operations, and fast update capability.

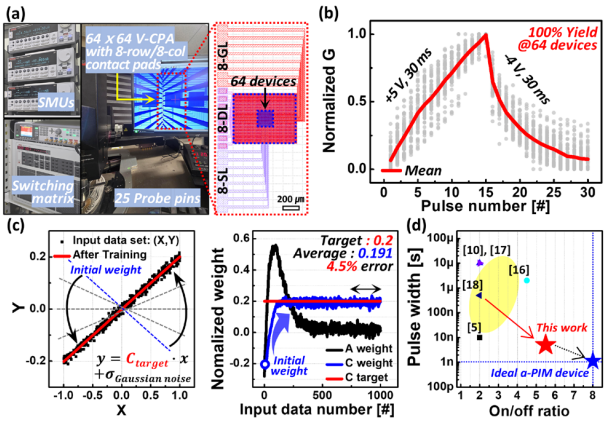

Fig. 9. (a) Measurement setup and specially designed 64×64 HSV-ECRAM cross-point array with 8-row/8-column contact pads. (b) Conductance modulation of all 64 devices, showing 100% functional yield. (c) Experimental array-level training results using Tiki-Taka (TT) algorithm. (d) Comparison of minimum pulse width and on/off ratio, showing the advantage of HSV-ECRAM for practical a-PIM device.

Table I. Benchmark table of key performance metrics MO-ECRAMs

	2019 [5]	2020 [16]	2021 [17]	2024 [18]	2025 [10]	2025 [9]	This work
Minimum Area	$8F^2$	$8F^2$	$4F^2$	$4F^2$	$8F^2$	$8F^2$	$4F^2$
Material	WO_3 HfO_2 MO	TiO_{2-x} YSZ TiO_{2-x}	WO_3 AlO_x GdO_x	WO_3 HfO_2 WO_3	ZnO HfO_2 CeO_2 + OA ligands	LSF50 /BISC UVOS/ LSF50	WO_3 **SDC** WO_3
Operating Voltage (V)	+4/ -4	+1.5/ -1.5	+6.5/ -6.5	+12/ -10	+15/ -2	+0.7/ -0.7	**+8/ -5**
Minimum Pulse Width	10 ns (RT)	2 μs (160°C)	10 μs (RT)	500 ns (RT)	10 μs (RT)	400 ms (150°C)	**sub-5 ns (RT)**
G_{max}/G_{min} Ratio	< 2	< 4.5	< 2	< 2	< 2	< 5	**< 5.5**
Array size	2 x 2	-	2 x 2	64 x 64	-	-	**64 x 64**

V. Conclusion

In this paper, we present a vertically integrated HSV-ECRAM based on a WO_x/SDC/WO_x stack, achieving sub-5 ns switching enabled by a high ionic conductivity Sm-doped CeO_2 electrolyte and a vertical sidewall channel structure. As summarized in **Table I.**, the proposed HSV-ECRAM shows improved switching speed compared to previously reported MO-ECRAMs. In addition, it exhibits large conductance change ($\Delta G > 8{,}000$) and low switching energy per conductance change ($E/\Delta G \sim 10^{-4}$ J/S). Furthermore, a 64×64 HSV-ECRAM cross-point array is fabricated and shown to achieve 100% functional yield in the measured array region. Finally, array-level neural network training is experimentally demonstrated using the TTv1 algorithm, highlighting the potential of HSV-ECRAM for M3D-compatible a-PIM applications.

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