A 5-12V to 1-1.8V DC-DC Converter with Transient Energy Buffer Achieving 3.4× Overshoot Reduction under 5A/20ns Load Transients

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***Abstract*—This paper presents a DC-DC converter with transient energy buffer (TEB). During load step-down events, by redirecting excess inductor energy from low-voltage output to an internal voltage-tolerant node and absorbing it with a buffer capacitor, output voltage overshoot is significantly reduced without large output capacitance. In steady state, the buffer capacitor and associated switches form a parallel capacitive power path, reducing the inductor current stress, improving power density and also heavy-load efficiency. Measured results demonstrate a 3.4× reduction in output voltage overshoot under a 5A/20ns load transient.**

***Keywords*—DC-DC Converter, Transient Energy Buffer, Fast Transient Responses**

I. Introduction

As XPU current density continues to scale toward 2A/mm² and beyond, voltage regulation modules (VRMs) become increasingly space-constrained, leaving little headroom to further scale power passives (inductors and extensive capacitors) for sufficient transient energy buffering, as shown in Fig.1. Consequently, during load step-down transients, the persisting inductor current I_L is forced into the output capacitors, causing large voltage overshoot for low-voltage (LV) loads, such as XPUs or downstream integrated voltage regulators (IVRs). This behavior is fundamentally constrained by the limited inductor demagnetization voltage under LV output, which is typically 5-10× lower than the available magnetization voltage. As voltage margins continue to shrink in advanced XPU designs, transient voltage overshoot increasingly manifests not as a regulation accuracy issue, but as a device-level overvoltage issue and reliability challenge driven by system-level transient behaviors. This observation motivates alternative transient-handling approaches that redirect the transient inductor current path, rather than relying solely on energy buffering at output node [1-4].

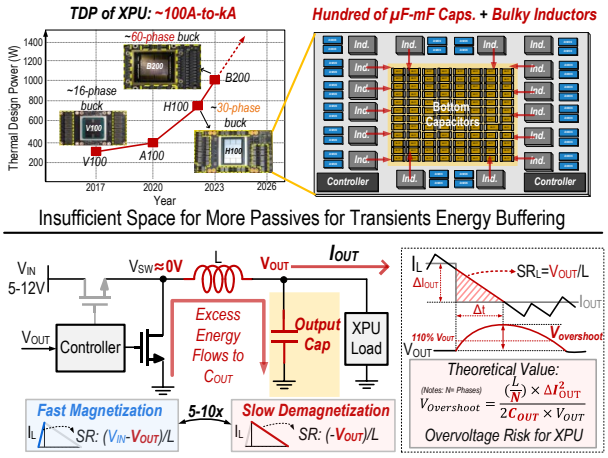


Fig.1 Overvoltage issue for XPU during load step-down events.

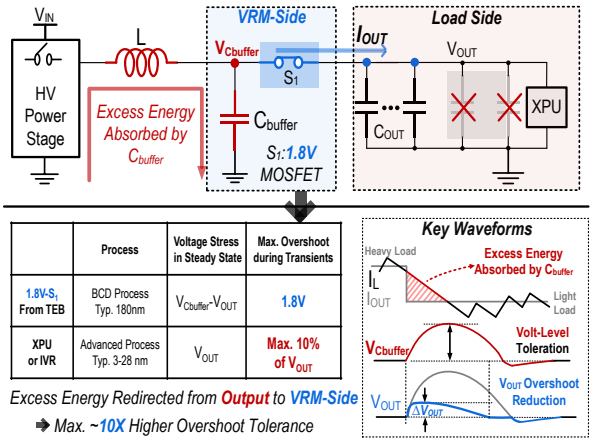


Fig.2 Design concept of proposed transient energy buffer (TEB)

II. Proposed DC-DC Converter With Transient Energy Buffer

A. Design Concept

This paper presents a transient energy buffer (TEB) for output overshoot voltage reduction. As shown in Fig.2, a portion of the output capacitor (C_{OUT}) is decoupled and reconfigured as buffer capacitor (C_{buffer}). Through a dedicated switch S_1 which connects C_{buffer} to the output node, C_{buffer} forms an independent VRM-side energy absorption path that diverts excess transient inductor energy. Since the voltage stress across S_1 is $V_{Cbuffer}$-V_{OUT}, the buffer node can tolerate volt-level transient overvoltage (e.g., using a 1.8-V MOSFET for S_1), well beyond the allowable voltage excursion at the LV output node. Accordingly, the proposed TEB operates in two modes, as shown in Fig.3. During load step-down transients, TEB operates in transient mode, where a local V_{OUT}-regulation loop drives S_1 to momentarily support load current I_{OUT} and rapidly stabilize V_{OUT} while absorbing excess inductor energy in C_{buffer}, thereby reducing output voltage overshoot without scaling large output capacitance. In steady state mode, C_{buffer} and the reconfigured switches provide a capacitive current path in parallel with the inductor, relaxing inductor DC current stress and enabling higher power density. This reconfiguration also allows parallel TEBs to reduce conduction loss and enhance heavy-load efficiency.

B. Operation Principle of Proposed Converter with TEB

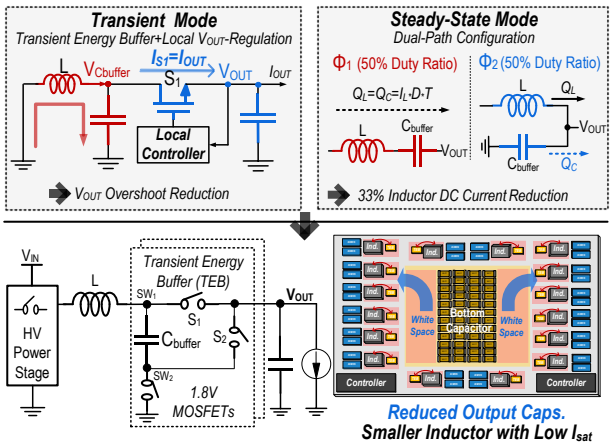


Fig.3 Topology and operation principle of the proposed converter with transient mode and steady-state mode

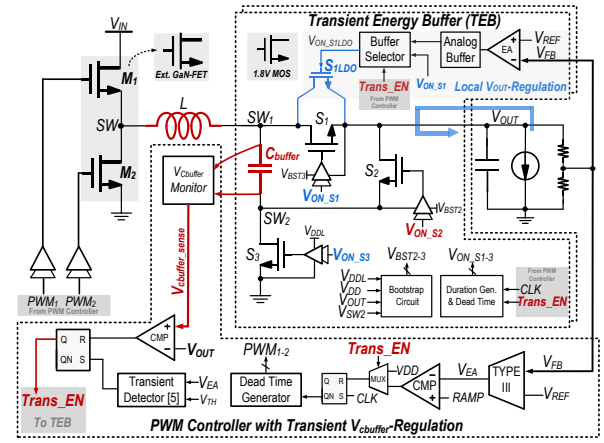


Fig.4 Block diagram of proposed DC-DC converter with TEB

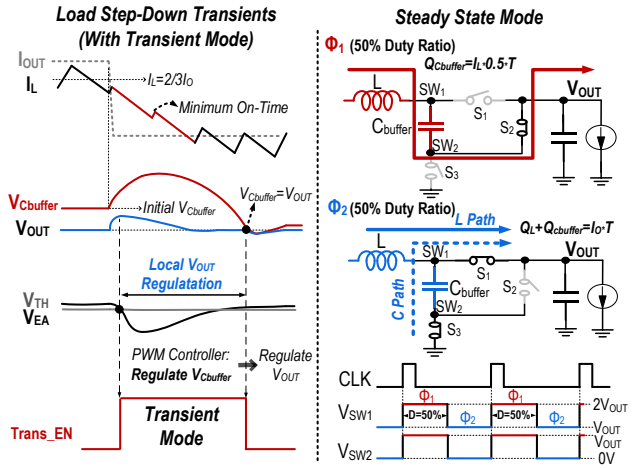


Fig.5 Key waveforms of the proposed converter during load step-down transients and steady state.

Fig.4 shows the system block diagram. It consists of a high-voltage buck power stage with two switches $M_{1\text{-}2}$, an inductor L, a PWM controller for steady-state V_{OUT} regulation, and the proposed TEB which comprises C_{buffer}, switches $S_{1\text{-}3}$ and a local V_{OUT}-regulation loop. A transient detector [5] in the PWM controller generates the rising edge of the detection signal Trans_EN. Fig.5 illustrates the key waveforms in transient and steady-state modes. When

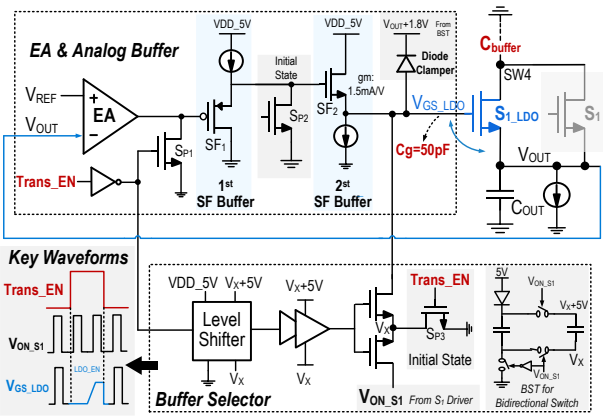
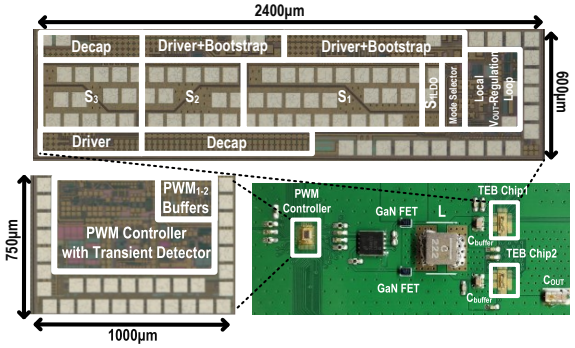


Fig.6 Implementation of the local V_{OUT}-regulation loop.

Trans_EN is asserted, indicating a load step-down event, the proposed TEB operates in transient mode, the V_{OUT} regulation is handed over to the TEB-side, with S_3 turned on and $S_{1\text{-}2}$ turned off. V_{OUT} is locally fed back to the TEB-side error amplifier (EA), which then drives S_{1LDO} (derived from S_1), forming a local LDO scheme with $V_{Cbuffer}$ as its input. Meanwhile, the PWM controller changes to regulate $V_{Cbuffer}$ to its steady-state value (approximately equal to V_{OUT}). After that, Trans_EN is deasserted, the proposed TEB resumes steady-state mode, and the V_{OUT} regulation is handed back to the PWM controller.

C. Circuit Implementaion

Fig.6 shows the implementation of local V_{OUT}-regulation loop. Leveraging ~10× higher saturation current capability compared with linear operation, S_{1LDO} is sized to only 1/10 of S_1. With C_{OUT} remaining at μF-level, the dominant pole is located at output node and lies in the tens of kHz. Two-stage buffers $SF_{1\text{-}2}$ are introduced to push secondary poles well beyond the dominant pole, ensuring sufficient phase margin. The EA and buffers are powered by a 5V supply to maintain adequate headroom for maximum 1.8V output. A diode clamper is placed at the gate of S_{1LDO} to avoid gate overvoltage stress. A bidirectional switch selects the control signal, i.e., V_{ON_S1} from S_1's driver in steady-state mode or the analog control signal in transient mode driving S_{1LDO},



Topology	2.2uH Inductor		Output Capacitor +Buffer Capacitor	Total Volume (Passives)
	Isat (20% Drop)	Size		
Buck	8A (6.8mΩ)	5.5mm×5.3mm×5.1mm	10μF 0603×4 1.6mm×0.8mm×1mm×4	153mm³
Buck+TEB	6.8A (9.2mΩ)	5.5mm×5.3mm×3.1mm	10μF 0603×4+10μF 0603×2 1.6mm×0.8mm×1mm×6	98mm³

Fig.7 Die photo and PCB prototype.

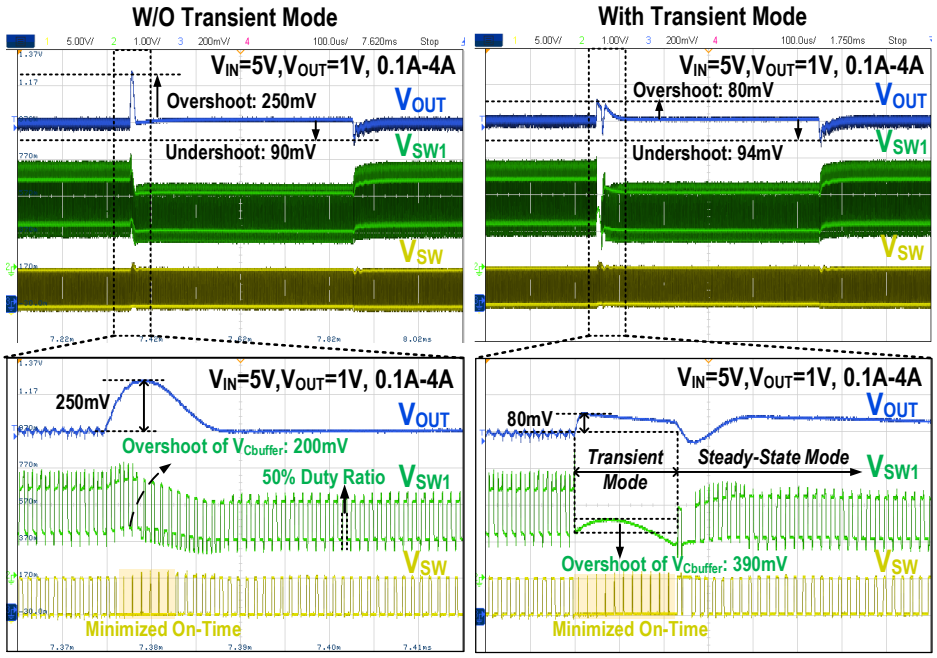


Fig.8 Measured load transient responses with or without the transient mode at V_{IN}/V_{OUT}=5V/1V.

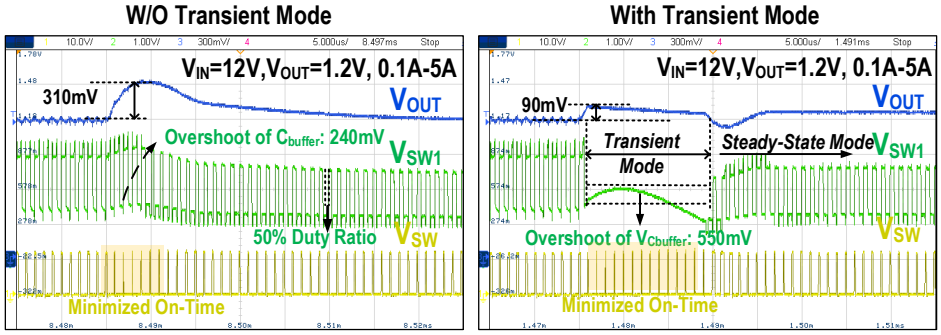


Fig. 9. Measured load transient responses with or without the transient mode at V_{IN}/V_{OUT}=12V/1.2V

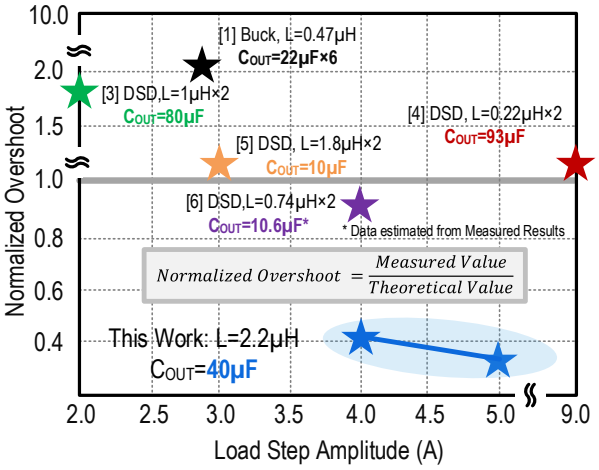


Fig.10 Normalized overshoot comparison

avoiding false triggering through the body diode.

III. Measurement Results

The prototype of the proposed converter is shown in Fig.7. The PWM controller and the proposed TEB are fabricated in a 0.18μm BCD process. The HV buck power stage switches at 0.8-1MHz with two GaN switches ($M_{1\text{-}2}$), a 2.2μH inductor and 40μF output capacitor, while the proposed TEBs operate synchronously with total 20μF buffer capacitance.

Fig.8 shows the measured load transient responses at V_{IN}/V_{OUT}=5V/1V with a 4A/20ns load step. V_{OUT} exhibits 250mV overshoot and 90mV undershoot without the transient mode. The zoom-in waveforms during load step-down verify that the PWM controller operates at minimum on-time. With the proposed transient mode, V_{OUT} overshoot is significantly reduced to 80mV, even lower than the undershoot during load step-up. The zoom-in waveforms show that the excess inductor energy is absorbed by C_{buffer}, resulting in 390mV voltage overshoot on it. Nearly 3.4× overshoot reduction is observed at V_{IN}/V_{OUT}=12V/1.2V with 5A/20ns load transients as shown in Fig.9. The normalized overshoot comparison shown in Fig.10 (measured overshoot normalized to the theoretical value) indicates that the proposed converter achieves the highest overshoot reduction. Fig.11 depicts the measured efficiency up to 8A load current. Peak efficiency of 91.2% and 89.8% are achieved at V_{IN}/V_{OUT}=5V/1V and 12V/1.2V,

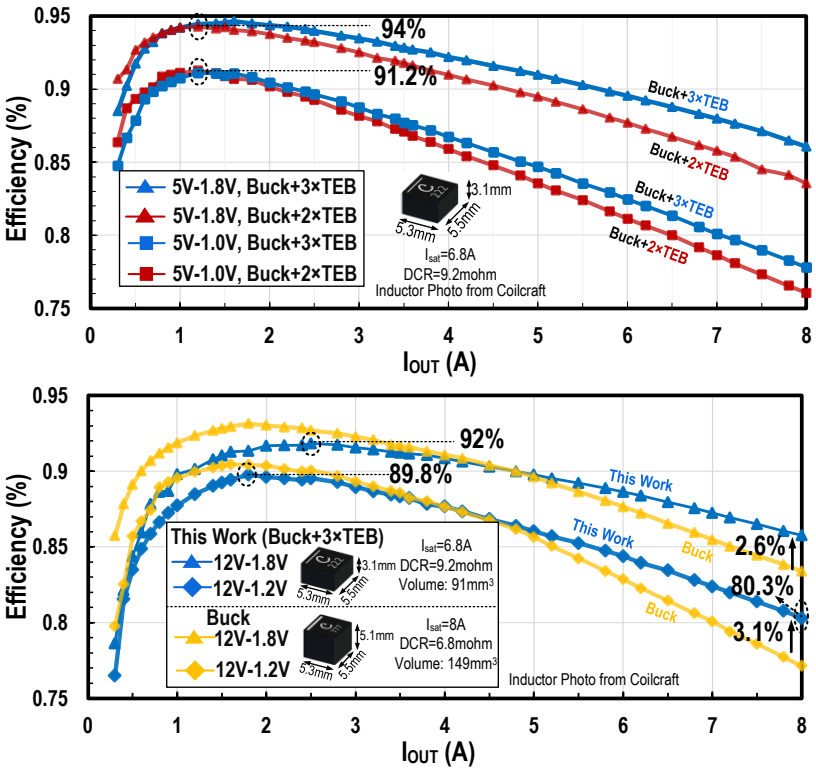


Fig.11 Measured power efficiency and comparison with a buck converter with bulky inductor.

TABLE I. COMPARISON WITH PREVIOUSLY WORKS

Publication		ADI MAX77542 [1]	ISSCC'22 [6]	ISSCC'23 [2]	ISSCC'25 [3]	This Work	
Topology		4-Phase Buck	CCC (2-Phase)	ReSC-PL	DSD (2-Phase)	**Buck+TEB**	
Nominal V_{IN}		12V	12V	12V	12V/24V	**5V-12V**	
Nominal V_{OUT}		0.3V-5.2V	0.9V-1.8V	0.6V-1.2V	1.2V-2V	**1V-1.8V**	
f_{SW}		0.5-1.5MHz	2MHz	0.8MHz	1.1MHz	**0.8-1MHz**	
Maximum Load Current		16A	4A	5A	6A	**8A**	
Inductor		0.47μH×4	0.74μH×2	1μH	1μH×2	**2.2μH**	
Flying Capacitor		No	2.2μF	22μF×2+10μF×2	4.7μF	**10μF×2 (C_{buffer})**	
Output Capacitor		(22μF×6)×4	10.6μF***	100μF	80μF	**10μF×4**	
Peak Efficiency (12V-1.2V)		85%* (4A)	86.8% (2A)	91.5% (1A)	92% (2.5A)	**89.8% (1.8A)**	
Full Load Efficiency (12V-1.2V)		78%* (16A)	81%* (4A)	81% (5A)	87.5% (6A)	**80.3% (Buck+TEB, 8A) 77.2% (Buck, 8A)**	
Down-Transient	Load Step	2.8A/500ns* (Single-Phase)	4A/20ns	4.2A/20μs	2A	**5A/20ns**	**4A/20ns**
	V_{OUT} Overshoot	40mV	210mV	180mV	25mV	**90mV**	**80mV**
	Normalized Overshoot**	2.87	0.9***	8.18	1.8	**0.29**	**0.4**

* Data estimated from the figures

** Measured results normalized to the theoretical overshoot of corresponding buck, CCC, DSD, ReSC-PL and topology of this work

*** Output capacitance estimated from measured V_{OUT} ripple, smaller than nominal value

respectively with three TEB chips paralleled and a compact inductor (6.8A saturation current)

Compared to the conventional buck converter with bulky inductor (I_{sat}=8A), the proposed converter with TEB achieves up to 3.1% full-load efficiency improvement at V_{IN}/V_{OUT}=12V/1.2V while reducing the total passive component volume (including C_{OUT}, C_{buffer} and L) by 30%.

Table I summarizes the performance. This work achieves highest normalized overshoot reduction and delivers comparable transient overshoot per ampere to [1], while requiring only 1/3 of C_{OUT} (40μF vs. 132μF).

ACKNOWLEDGEMENTS

This work was supported in part by the National Natural Science Foundation of China under Grant 62504216, National Natural Science Foundation of China under Grant 92373203 and Natural Science Foundation of Anhui Province under Grant 2508085QF218. (Corresponding author: Lin Cheng.)

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