A 71.2 dB SNDR, 50 MS/s Predictive SAR ADC with Quasi-Monotonic Switching and Fully Integrated Reference Buffer

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***Abstract*—This paper presents a SAR ADC that integrates a fully digital Newton–Gregory predictor, enabling the ADC to operate from a supply approximately equal to half the input signal swing. This halves the Walden figure-of-merit, improving the overall ADC efficiency. With a 1 V supply, a diode-flipped-voltage-follower buffer provides compact on-chip reference buffering with high accuracy and fast settling, without external components. The prototype demonstrates > 71.2 dB peak SNDR over a 5 MHz bandwidth and across PVT variations.**

Keywords— Predictor, reference buffer, on-chip, SAR ADC, predictive level-shifting, diode-flipped-voltage-follower.

I. Introduction

High-resolution, high-speed SAR ADCs require an on-chip reference buffer, which incur significant power and area overhead to deliver large charge bursts within a few picoseconds. Its power dissipation can be comparable to, or even exceed, that of the ADC core itself [1], [2]. Prior solutions [1]–[6] mitigate this issue by reducing the DAC weights during the initial conversion cycles [1], calibrating reference-buffer-induced errors [2], or employing an auxiliary DAC to support fine settling [3]. However, these approaches increase complexity and reduce system efficiency by requiring precise calibration. Furthermore, these techniques are applicable only to relatively low resolutions (SNDR < 60 dB) [1]–[5], or they require an on-chip decoupling capacitance at least an order of magnitude larger than the capacitive DAC array (CDAC) [3], [6], thereby incurring a significant area penalty. To further improve system efficiency, prediction techniques have also been explored in SAR ADCs. In [7], prediction is employed to limit the voltage swing of the ADC input buffer, enabling true rail-to-rail operation without compromising linearity. However, the predictor is analog and must still operate from a higher supply voltage than the following ADC. It also relies on an additional coarse ADC and DAC, thereby increasing power overhead, unlike the proposed work, which uses only a fully digital predictor. In [8], area and power efficiencies are further improved by replacing the analog predictor with a digital one. Nevertheless, adaptive coefficients are required for its FIR filter, leading to high hardware complexity and power consumption while still necessitating the coarse ADC and DAC inherited from its analog counterpart. In [9], a digital prediction technique is proposed to minimize toggling of the DAC MSB. However, achieving a 3-bit prediction accuracy requires a high oversampling ratio (OSR) of 9, which limits its applicability to lower-bandwidth systems. In [10], part of the CDAC is reused to generate a tri-level MSB prediction, which is then used to preset the CDAC bottom plates during the sampling phase Φ_s, enabling the ADC to process input amplitudes up to twice its reference voltage. However, because the prediction is performed in a dedicated phase preceding Φ_s, it introduces a conversion-time penalty. Despite these advances, prior work does not provide a fully digital predictor with low power and area overhead together with an efficient fully integrated reference buffer. This work addresses these limitations by introducing a SAR ADC with a fully digital 3-MSB prediction and an integrated diode-flipped-voltage follower (DFVF) reference buffer. Rather than digitizing the full-scale input, the ADC predicts the next sample, $V_{in}[k+1]$, from past conversion results and samples only the prediction error. The prediction is performed during the conversion of the current sample $V_{in}[k]$, thereby avoiding any conversion-time penalty. As a result, the ADC, including its reference buffer (REFBUF), can operate from a lower supply voltage, improving overall system efficiency. Fig. 1(a) shows the proposed ADC with digital predictor and integrated REFBUF, while Fig. 1(b) illustrates the CDAC switching sequence of a 4-bit example for $V_{in}\geq 0$. A symmetric switching sequence applies for $V_{in}<0$.

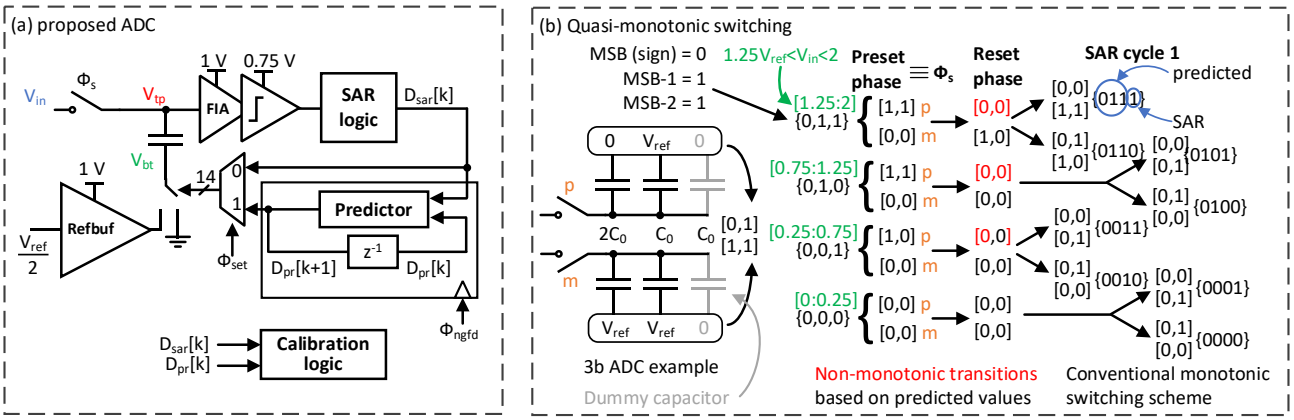

Fig. 1. Proposed ADC with on-chip reference buffer (a) and simplified 4b ADC switching sequence with input $V_{in}[k]>0$ (b).

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Because the predictor drives the CDAC during Φ_s, before the SAR conversion begins, some CDAC transitions become non-monotonic (quasi-monotonic switching). The remainder of this manuscript is organized as follows: Section II introduces the employed predictor, highlights its advantages over prior approaches, and discusses how robust predictor startup operation is ensured. Section III describes the implementation of the proposed DFVF. Section IV presents the overall SAR ADC implementation. Section V reports the measurement results and compares the proposed ADC with state-of-the-art designs employing fully integrated reference buffers.

II. NGFD PREDICTOR

The first three MSBs are predicted so that, before the sampling phase begins, both the sign of $V_{in}[k+1]$ and its amplitude with 2-bit precision are known. Accordingly, during the preset phase (Φ_{set}), the CDAC bottom plates V_{bt} are driven by the predictor output D_{pr}. Although the effective ADC reference is V_{ref}=1.5 V, the REFBUF only needs to provide $V_{ref}/2$=0.75 V; assuming a correct prediction, the residue to be resolved by the SAR ADC is then smaller than $V_{ref}/4$. The first two MSBs, namely the sign bit and the $V_{ref}/2$ step, are not implemented by physical CDAC capacitors, but are applied through simultaneous control of all capacitor bottom plates during the preset and reset phases. Fig. 2(a) shows the timing diagram of the proposed ADC and highlights two key differences with respect to a conventional SAR ADC. First, the predicted value is applied during Φ_{set}. Second, while sample $V_{in}[k]$ is still being resolved, the predictor computes the estimate of the next sample, $V_{in}[k+1]$, during phase Φ_{ngfd} from the first nine resolved MSBs. As a result, the prediction introduces no conversion-time penalty. In addition, the quasi-monotonic switching scheme reduces the switching energy with respect to conventional monotonic switching, as shown in Fig. 2(b), because the effective V_{ref} is halved and the first few MSBs are applied in a single operation during the preset and reset phases, thereby avoiding unnecessary transitions. The predictor is implemented as a fully digital third-order Newton–Gregory forward-difference (NGFD) predictor [11]. The NGFD predictor is defined by (1), while the prediction-error transfer function H_{err} is given in (2), where $Z\{\cdot\}$ denotes the Z-transform. Here, $D_{pr}[k+1]$ denotes the prediction of the next input sample, $D[k]$ is the digitized value of $V_{in}[k]$, and R_P is the prediction order.

$$D_{pr}[k+1] = \sum_{m=0}^{R_p} \binom{R_P}{m} (-1)^m D[k-m-1] \quad (1)$$

$$H_{err}[z] = \frac{V_{err}[z]}{V_{in}[z]} = 1 - \frac{Z\{D_{pr}[k]\}}{V_{in}[z]} \quad (2)$$

Fig. 2(c) plots $H_{err}[z]$ for different values of R_P as a function of input frequency f_{in} and sampling frequency f_s, which directly translates into the OSR required to achieve a given number of predicted MSBs. In this work, three MSBs are predicted; therefore, the remaining SAR bits, spanning 25% of the single-ended input range, act as redundancy to correct the prediction error, which must remain smaller than $|V_{in}|/4$. An operating point of R_P=3 and OSR=5 is selected, ensuring a prediction error below -16 dB with respect to the maximum $|V_{in}|$, and therefore always correctable by the subsequent ADC bits. For R_P=3, the predictor transfer function simplifies to $D_{pr}[z]=z^{-1}D[z](4-6z^{-1}+4z^{-2}-z^{-3})$, with $D[z]\approx V_{in}[z]$. The hardware overhead remains minimal, since the predictor is implemented using only digital adders, shifters, and registers. Fig. 2(c) also highlights the range of f_{in} for which an input of amplitude A_{in} can be predicted with an error below -16 dB.

A. Prediction error tolerance and startup robustness

The previous section described how the in-band prediction error can be bounded below the ADC redundancy range by design. In practice, the anti-aliasing filter preceding the ADC in the AFE attenuates unwanted frequency components above the ADC bandwidth. Even with a non-ideal anti-aliasing filter, the -16 dB prediction error bound set by OSR = 5 provides additional margin beyond the maximum correctable prediction error of -12 dB to correct any residual error. Prediction errors can still occur at startup, before sufficient past samples are available to the NGFD predictor. Because a monotonic switching scheme is employed, this condition is detected by the NGFD logic when all the bits on one side of the CDAC are either 0 or 1 at the end of conversion. This indicates that the top-plate voltage of the ADC did not converge the residue to less than one LSB. In this case, the predictor enters a startup mode in which the allowable prediction error is relaxed by two mechanisms. First, only a 1-MSB prediction is used, thus doubling the ADC redundancy. Second, R_P is dynamically adjusted by a finite state machine and, in startup mode, the NGFD relies on a smaller number of previous samples.

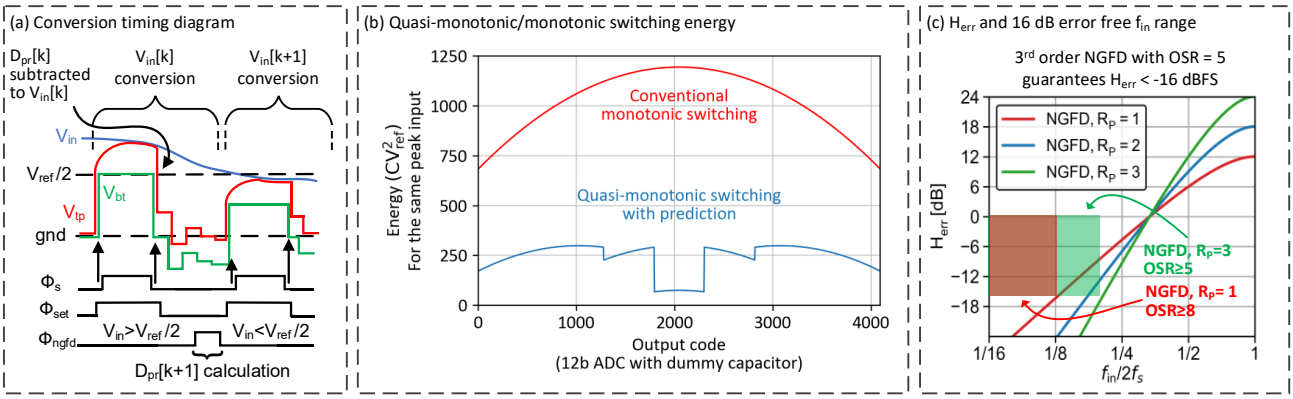

Fig. 2. Timing diagram of the proposed ADC including Φ_{ngfd} (a), quasi-monotonic switching scheme energy compared to the monotonic switching scheme (b), and H_{err} for different NGFD orders (c).

III. Diode Flipped Voltage Follower

The fully-integrated reference buffer operates at V_{DD}=1V and is built using only thin-oxide devices. Still, challenging GHz-bandwidth is required to achieve accurate settling for 13 DAC cycles in 15 ns and input sampling in 5 ns. This challenge is addressed by the proposed slew-free DFVF shown in Fig. 3. Similar to a conventional flipped-voltage-follower (FVF), the local feedback loop reduces the output impedance improving transient behavior. A key shortcoming of the FVF is that its dominant and non-dominant poles are close to each other, reducing the phase margin. They cannot be separated without burning excessive power. The DFVF naturally spreads them apart by making $gm_{N0}/(Cgs_{N0}+Cgs_{P0})$ the non-dominant pole while the dominant pole is $\sim gm_{P1}/C_{DEC}$, which are separated as $C_{DEC}>>Cgs_{N0}+Cgs_{P0}$. Additionally, bi-directional current drive is required for the buffer during Φ_s: while the PMOS device sources the required current like an FVF, the diode-connected NMOS also sinks the required current, both without slewing. The output stage is biased with a constant current (proportional to I_B) by regulating the threshold voltages of P_0 and N_0 through body biasing (V_{bp} and V_{bn}), which is permissible in this FDSOI process. A replica body biasing loop achieves this, leading to a PVT-independent output-stage current.

IV. ADC Implementation

The proposed ADC is clocked at 50 MHz. The 14-bit CDAC adopts the quasi-monotonic switching scheme with two redundant bits for prediction error correction. The floating inverter amplifier (FIA) is chosen for its robustness against common-mode variation. It operates at V_{DD}=1V and it is the interface between the input in the 1.5 V domain and the rest of the ADC at lower supply. Its input devices are the only ones that require thick oxide for reliability. The comparator following the FIA and all the digital circuits are under a 0.75 V supply. The DFVF provides the $V_{ref}/2$ voltage to the CDAC array and capacitor mismatch is addressed by an on-chip calibration scheme similar to [12]. The capacitor weights are stored in registers and applied by the calibration logic during regular operation.

V. Measurement Results

The ADC was fabricated in a 22nm FDSOI technology and occupies an area of 0.15 mm^2. Fig. 4 shows the measured output spectrum for 0.1 MHz (a) and 4.5 MHz (b) inputs, achieving SNDRs of 73.1 dB and 71.2 dB, over a 5 MHz bandwidth. The dual-tone test (c) with band-edge signals exhibits an IM3 of 71.2 dB, and the total power consumption (d) is 690 µW. Fig. 5 shows that the dynamic range (DR) is 76.7 dB and decreases by 6 dB without the predictor enabled. Fig. 6 reports that the measured SNDR remains above 72 dB from −40 °C to 125 °C (a) and summarizes SNDR and SNR across different chips as well as the same metrics under ±5% supply variation (b)-(c). Fig. 6 (d) shows the chip micrograph, while Fig. 7 compares this design with state-of-the-art ADCs featuring integrated reference buffers. The proposed 3rd-order NGFD-predictor halves the ADC supply and reduces the CDAC switching energy by employing the quasi-monotonic switching scheme. This is achieved with the lowest reported OSR = 5 for fully digital predictors. The predictor itself only consumes 6% of the total ADC power. The proposed DFVF achieves fast settling with a decoupling capacitor C_{DEC} only 5 times larger than the CDAC, while consuming 366 µW and maintaining >11.5-bit ENOB across PVT corners at 50 MS/s. This makes the DFVF competitive with state-of-the-art integrated reference buffers when all the ADC SNDR, sampling frequency and the C_{DEC}-to-CDAC ratio are jointly considered.

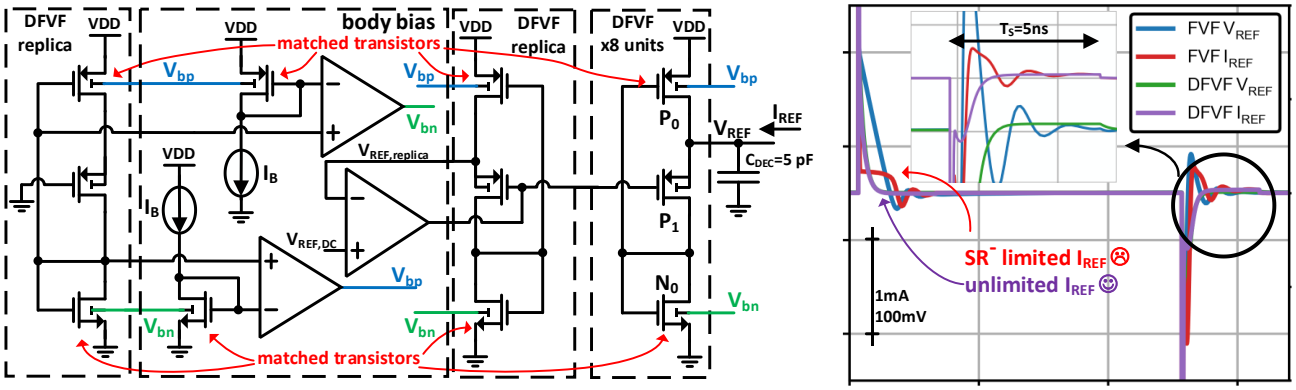

Fig. 3. Proposed DFVF-based reference buffer without external capacitor. The body bias block together with DFVF replica sets the body voltage of the output stage consisting of eight DFVF (left). Simulated DFVF output voltage and current compared to those of a FVF with the same power consumption (right).

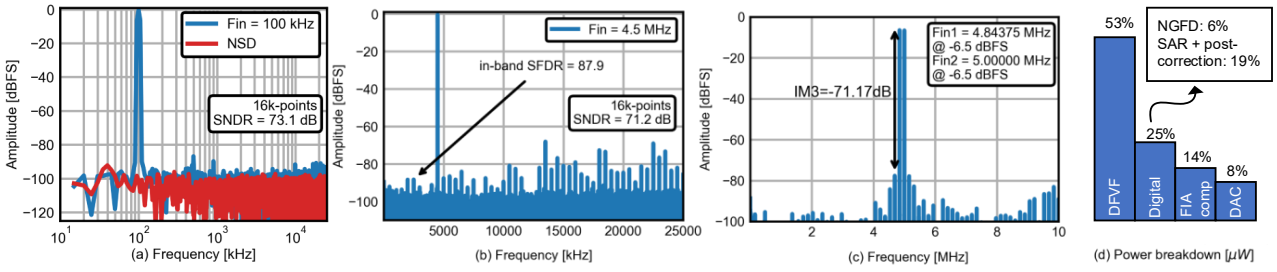

Fig. 4. Measured noise spectral density (NSD) and FFT of a measured input at 0.1 MHz (a) and 4.5 MHz (b), dual tone test at band-edge (c) and power breakdown (d). All the FFTs are taken with Hann window.

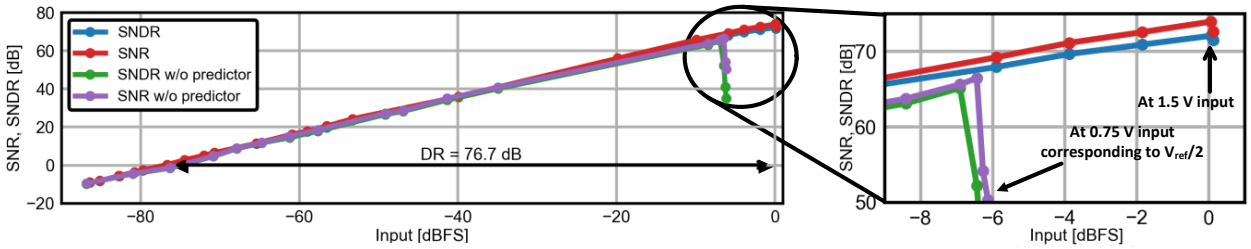

Fig. 5. Dynamic range (DR) with and without predictor enabled, showing the extension of the DR beyond the reference buffer voltage $V_{ref}/2$ when the predictor is enabled.

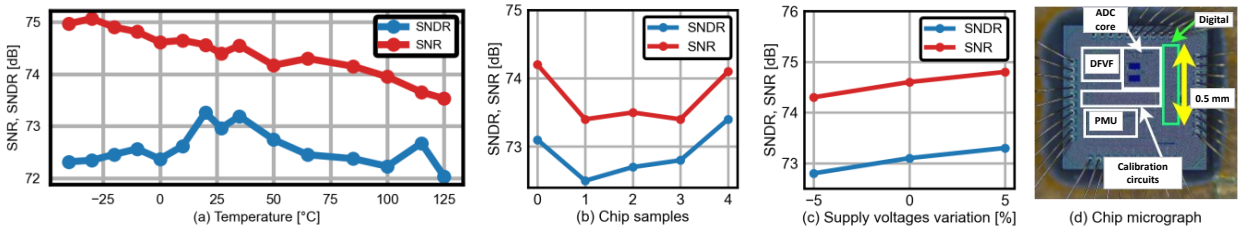

Fig. 6. SNDR and SNR variation in the [-40°C ; +125°] temperature range (a), SNDR across five chip samples (b), SNDR and SNR across supply variation (c) and chip micrograph (d).

	This work	[2] JSSC17	[3] JSSC19	[6] JSSC16	[7] JSSC23	[13] ISSCC25
Technology	**22nm**	65nm	65nm	28nm	180nm	55nm
SFDR [dB]	**87.9**	68.35	72.4	66	99.2	105.4
SNDR [dB] (LF/HF)	**73 / 71.2**	59	56.8	60.7 / 58	91.3	82.9
Supply [V]	**1.0 / 0.75**	1.2	1.0 /0.8	1.5 / 1.2	3.3 / 1.8	1.2
Power [mW]	**0.324[C]/0.690[R]**	2.44[R]	0.15[R]	17.5[A]	9.43[A]	0.47
Fs / BW [MHz]	**50 / 5**	100 / 50	20 / 10	600 / 300	12 / 6	40 / 2.5
Area [mm^2]	**0.15**	0.012	0.074	0.076	0.6	0.043
VDD [V]	**1 / 0.75**	1.2	1.0 / 0.8	1.2 / 1.5	3.3 / 1.8	1.2
Refbuffer power [µW]	**366**	840	17	150	-	-
C_{DEC}/C_{DAC}	**5**	3.9	20	16.7	-	-
Onchip reference buffer?	**YES**	YES	YES	YES	NO	NO
FoMs[P] [dB]	**174.9[C]/171.6[R]**	162.1[R]	165	160.3[A]	182.1[A,C]/177	180.2[C]
FoMw[P] [fJ/conv]	**8.8[C]/18.9[R]**	37.9[R]	13.3	44.9[A]	26.2[A,C]/84.4	8.2[C]

[A] = Predictor (if applicable) and input buffer power not included
[C] = Without DAC reference buffer / FoMW = Power/(fNyq×2ENOB) [P] = peak FoM
[R] = With reference buffer, NGFD predictor, calibration control, post correction

Fig. 7. Performance comparison with state of the art.

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