A Wide-Range, 5.03 ps Resolution Coarse-Fine Noise-Shaping TDC Using a Voltage-Controlled Switched-Ring Oscillator for dToF LiDARs

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***Abstract*—This paper presents a coarse-fine noise-shaping time-to-digital converter (CF-NS TDC) for direct time-of-flight (dToF) LiDAR applications. First-order noise shaping is achieved using a voltage-controlled switched-ring oscillator (VCSRO) to enhance the resolution and PVT robustness of fine quantization. Meanwhile, a ripple counter performs coarse quantization, which limits the operating range of the VCSRO sub-TDC and thus suppresses noise degradation over a wide input range in conventional SRO-TDCs. Fabricated in a 0.18 µm CMOS process, the proposed TDC occupies an active area of 0.031 mm² and achieves an equivalent resolution of 5.03 ps with an integrated noise of 1.453 ps_{rms} over a 2046 ns dynamic range in a 100 kHz bandwidth. The single-shot precision and worst-case INL are 2.12 ps and +1.81/-2.45 LSB, respectively. Owing to the coarse-fine quantization scheme, the VCSRO sub-TDC maintains an integrated noise of 1.091-1.777 ps_{rms} across -40 °C to 85 °C and ±0.1 V supply variations.**

***Keywords*—time-to-digital converter, direct time of flight (dToF), switched-ring oscillator (SRO), LiDAR, noise shaping.**

I. Introduction

With advances in dToF LiDARs, the demand for time-to-digital converters (TDCs) capable of achieving a wide dynamic range while providing picosecond-level resolution has grown rapidly. Time amplifier (TA)-based TDCs obtain sub-gate-delay resolution and extend the dynamic range through the coarse-fine quantization scheme [1]. However, the tradeoff between the TA gain and linearity constrains the TDC to further enhance the resolution. Similar to their ADC counterparts, oversampling TDCs are widely adopted to achieve high resolution. In conventional gated-ring oscillator TDCs (GRO-TDCs), the sampling rate equals the event rate of *Start/Stop* signals. A high oversampling ratio (OSR) typically results in reduced bandwidth. This limits the achievable frame rate in LiDAR applications, since a lower bandwidth requires more laser emissions [2]. Switched-ring-oscillator TDCs (SRO-TDCs) [3] alleviate this limitation by decoupling the sampling clock from the input carrier signal. However, the oscillation frequency of conventional SROs is highly sensitive to PVT variations, and both power consumption and integrated RMS noise increase significantly with a large input range [4].

To address these issues, this paper presents a coarse-fine noise-shaping TDC (CF-NS TDC) that achieves high resolution and wide dynamic range with low circuit overhead (Fig. 1). For fine quantization, a voltage-controlled switched-ring oscillator (VCSRO) sub-TDC is proposed to implement first-order noise shaping while improving PVT robustness. Moreover, a ripple counter based coarse quantizer confines the input range of the VCSRO sub-TDC within a single counting clock period, thereby suppressing integrated noise degradation over a wide input range. The prototype TDC achieves a 2046 ns dynamic range, an equivalent resolution of 5.03 ps, and a single-shot precision of 2.12 ps, while occupying an active area of 0.031 mm².

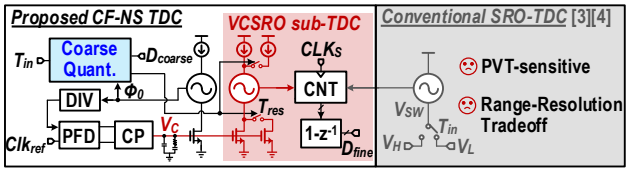

Fig. 1. Proposed CF-NS TDC and prior arts.

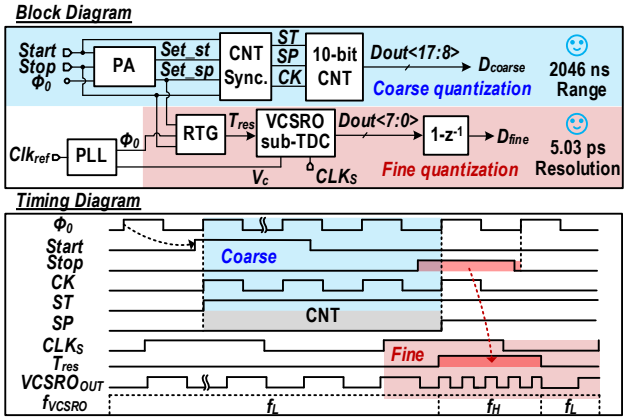

Fig. 2. Overall block and timing diagram of proposed CF-NS TDC.

II. Proposed Coarse-Fine Noise-Shaping TDC

Fig. 2 shows the overall block diagram and timing diagram of the proposed CF-NS TDC. A coarse-fine quantization scheme is presented to achieve both a wide input range and high resolution. A 500-MHz clock Φ_0 is generated by a PLL, and a ripple counter is employed for coarse quantization. In dToF LiDAR applications, the *Start* signal is synchronized with the PLL's reference clock Clk_{ref}, ensuring a fixed time offset T_{offset} between *Start* and Φ_0. During coarse quantization, a phase arbiter (PA) is proposed to determine the phase information of the *Start/Stop* signals with respect to Φ_0 for subsequent counter synchronizer [1]. The *ST/SP* signals are then generated after *Start* and *Stop* signals are synchronized with Φ_0, respectively, thereby eliminating the misalignment error [5]. The *CK* signal is also synchronized with Φ_0 and serves as the counting clock. The ripple counter is enabled after the rising edge of *ST*, and its results are sampled at the rising edge of *SP*.

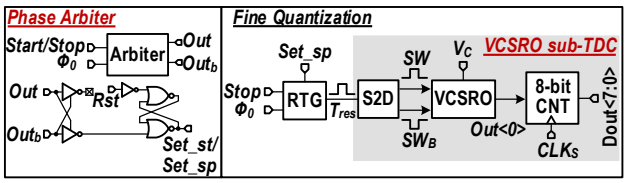

Fig. 3. Block diagram of the phase arbiter and fine quantization stage.

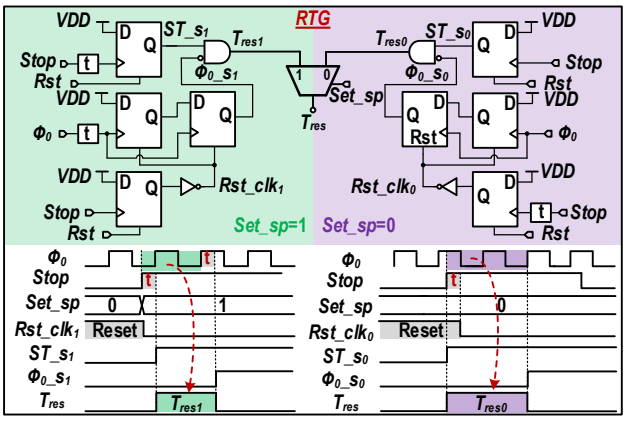

Fig. 4. Implementation of the RTG (top) and its timing diagram (bottom).

During fine quantization, a residue time generator (RTG) produces a pulse T_{res}, whose width represents the residue time after coarse quantization. To ensure complete frequency switching of the VCSRO, T_{res} is designed as the interval between the *Stop* signal and the second rising edge of Φ_0 following *Stop*. Consequently, the input range of the VCSRO sub-TDC is constrained to 2-4 ns, thereby suppressing integrated noise degradation in conventional SRO-TDCs. As shown in Fig.1, the tail current of the VCSRO is controlled by the voltage-controlled oscillator (VCO) control voltage V_C generated from the PLL. The VCO in the PLL is implemented as a replica of the VCSRO and operates at a frequency of f_L. When the input (i.e., T_{res}) toggles, the driving current of the VCSRO is doubled, yielding an operating frequency of $f_H \approx 2 \cdot f_L$, which improves robustness to PVT variations. The measured time interval between *Start* and *Stop* is expressed as $ToF = D_{coarse} \cdot T_{\Phi 0} - T_{res} + T_{offset}$, where D_{coarse} is the coarse quantization result and $T_{\Phi 0}$ is the period of Φ_0.

A. Fine Quantization Stage

Fig. 3 shows the block diagram of the PA and the fine quantization stage. In the PA, an arbiter followed by a cross-coupled inverter latch is employed to determine the phase of the *Stop* signal. To ensure correct extraction of the residue time, the RTG incorporates two topologies (Fig. 4), whose outputs are selected based on the PA output (i.e., *Set_sp*). The *Stop* and Φ_0 signals drive one- and two-stage DFFs, respectively, and are then combined to generate two candidate pulses T_{res1}/T_{res0}. One of these pulses is selected as the final residue time T_{res}, ensuring a minimum pulse width of one period of Φ_0. The VCSRO oscillation clock *Out<0>* is fed to an 8-bit counter, whose outputs are sampled by the clock CLK_S. The fine quantization result D_{fine} is calculated by sample-by-sample differentiation of *Dout<7:0>* as [4]

$$D_{fine}(z) = \frac{(f_H - f_L)}{T_c \cdot f_s} T_{res} + \frac{f_L}{f_s} + (1 - z^{-1}) T_q(z) \quad (1)$$

where T_c is the period of the *Start/Stop* signals, f_s is the frequency of the sampling clock CLK_S, and T_q is the time-domain quantization error. This indicates that first-order noise shaping is achieved in the fine quantization.

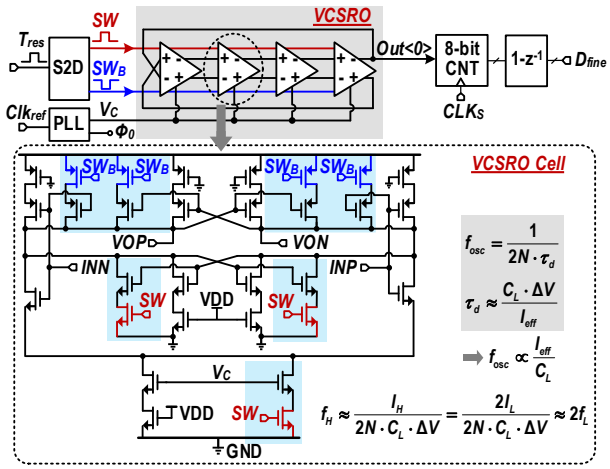

Fig. 5. Implementation of the proposed VCSRO sub-TDC.

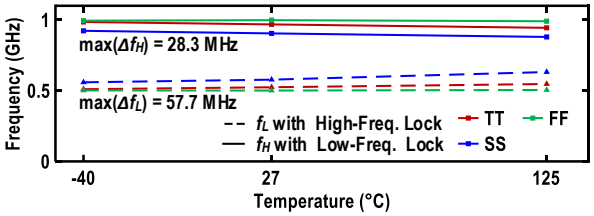

Fig. 6. Post-layout simulation results of the VCSRO frequency across PVT variations in two lock modes.

B. VCSRO Implementation and Lock Mode Analysis

Fig. 5 shows the schematic of the proposed VCSRO sub-TDC and the VCSRO cell. *SW* and SW_B are generated by an S2D circuit with a pulse width identical to that of the T_{res} signal. The VCSRO frequency in the sub-TDC is switched under the control of *SW* and SW_B. To improve frequency stability against PVT variations, an identical VCSRO is implemented in the PLL to generate the control voltage V_C for the VCSRO in the sub-TDC. In the PLL, *SW* and SW_B are tied to GND and VDD, respectively, such that the VCSRO operates at a fixed low frequency f_L. Since the oscillation frequency is proportional to the ratio of the effective driving current I_{eff} to the load capacitance C_L, switching half of both the pull-down and pull-up currents through *SW* and SW_B yields an approximate frequency ratio of $f_H:f_L \approx 2:1$. Although either f_H or f_L can be locked by the PLL, the other frequency remains PVT-sensitive. Taking the PVT-induced frequency variations into account, D_{fine} can be expressed as

$$D_{fine}(z) = \frac{(\Delta f + \Delta f_H - \Delta f_L)}{T_c \cdot f_s} T_{res,c} + \frac{f_L + \Delta f_L}{f_s} + (1 - z^{-1}) T_q(z) \quad (2)$$

where $\Delta f = f_H - f_L$, $T_{res,c}$ denotes the calculated residue time, and Δf_H and Δf_L represent the PVT-induced deviations of f_H and f_L, respectively. The residue time error Δt can be calculated as

$$\Delta t = T_{res,c} - T_{res} = \frac{(\Delta f_L - \Delta f_H)}{\Delta f} T_{res} - \frac{T_c \cdot \Delta f_L}{\Delta f}. \quad (3)$$

For low-frequency lock mode, setting $\Delta f_L = 0$ yields

$$\Delta t_{low} = -\frac{\Delta f_H}{\Delta f} T_{res}. \quad (4)$$

For high-frequency lock mode, setting $\Delta f_H = 0$ yields

$$\Delta t_{high} = -\frac{\Delta f_L \cdot (T_c - T_{res})}{\Delta f} = -\frac{\Delta f_L}{\Delta f} T_{res} \left(\frac{T_c}{T_{res}} - 1 \right). \quad (5)$$

In the proposed design, the input range of the VCSRO sub-TDC is constrained to 2-4 ns, and the *Start/Stop* event

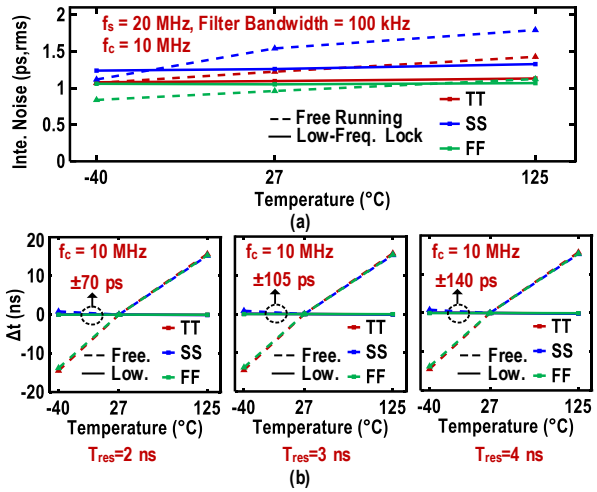

Fig. 7. Post-layout simulation results of the VCSRO sub-TDC and the free-running SRO-TDC across PVT variations. (a) Integrated noise. (b) Residue time error.

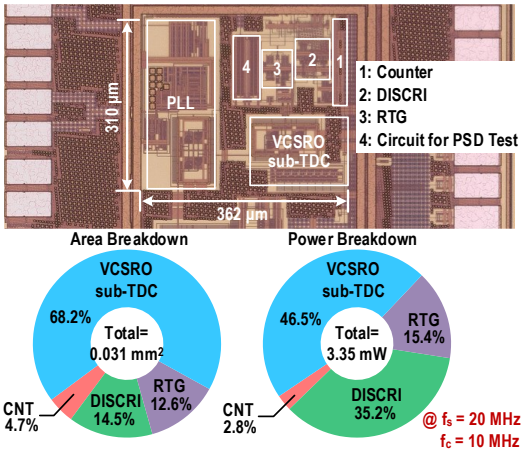

Fig. 8. Chip micrograph and area and power breakdown.

rate is typically below 10 MHz. As a result, T_c is much larger than T_{res}. Assuming that Δf_H and Δf_L are comparable, the residue time error under high-frequency lock mode (i.e., Δt_{high}) is significantly larger than that under low-frequency lock mode (i.e., Δt_{low}). Fig. 6 shows the post-layout simulation results of the VCSRO frequency, indicating that Δf_L is larger than Δf_H under PVT variations. Therefore, the low-frequency lock mode is adopted in this work to enhance robustness against PVT variations. Moreover, the integrated noise of the VCSRO sub-TDC under the low-frequency lock mode and that of the free-running SRO-TDC are simulated, as shown in Fig. 7(a). The free-running SRO-TDC, where V_C is fixed at a constant bias voltage, exhibits larger integrated noise variation across different temperatures. Three residue time inputs across the VCSRO sub-TDC range are applied in the simulation to evaluate the residue time error under PVT variations, as shown in Fig. 7(b). The results confirm that the proposed VCSRO sub-TDC achieves smaller residue time error than conventional free-running SRO-TDCs.

III. Measurement Results

The prototype TDC is fabricated in a 0.18 µm CMOS process and occupies an active area of 0.031 mm². The die micrograph, area breakdown, and power breakdown are shown in Fig. 8. It consumes 3.35 mW from a 1.8 V supply while operating with a 10 MHz input carrier and 20 MHz

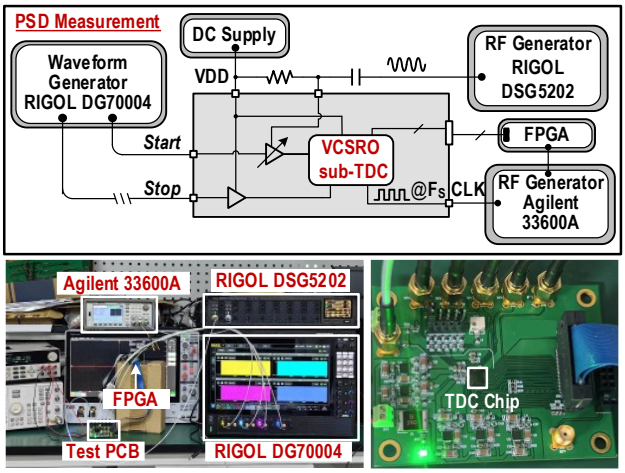

Fig. 9. TDC measurement setup.

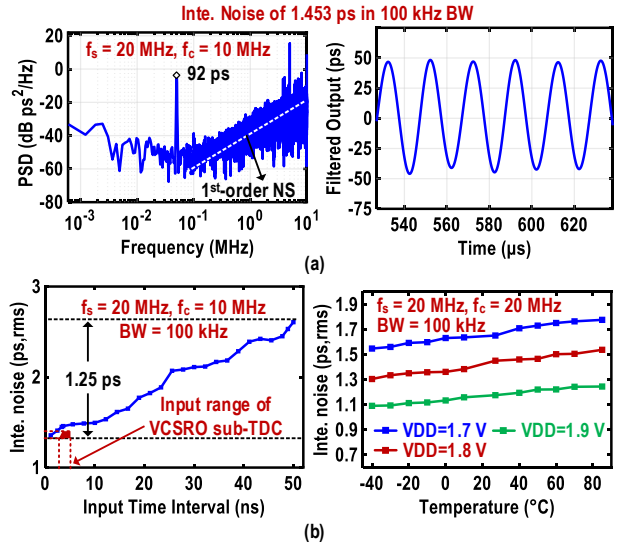

Fig. 10. (a) Measured power spectral density of the VCSRO sub-TDC and the filtered time-domain waveform. (b) Integrated noise vs. input time intervals, and temperature and supply variations.

sampling rate. During the measurement, the *Start* signal is synchronized to the PLL's reference clock, and the phase between *Start* and Φ_0 is removed as an offset.

The output power spectral density of the VCSRO sub-TDC is measured using a 50 kHz, 92 ps peak-to-peak sinusoidal input, with the measurement setup shown in Fig. 9. An additional DC offset of ~3.5 ns is applied to satisfy the input range requirement. The output spectrum is shown in Fig. 10(a), which exhibits good agreement with the ideal first-order noise-shaping. An integrated noise of 1.453 ps_{rms} is calculated over a 100 kHz bandwidth. The corresponding time-domain waveform after 100 kHz digital low-pass filter is also shown in Fig. 10(a). The integrated noise is evaluated with only the VCSRO sub-TDC operating, as shown in Fig. 10(b), varying by 1.25 ps over a 50 ns input range. In practice, the VCSRO sub-TDC operates over a 2-4 ns range enabled by the coarse-fine quantization scheme, thereby effectively mitigating noise degradation. Moreover, the VCSRO sub-TDC exhibits an integrated noise of 1.091-1.777 ps_{rms} across -40 °C to 85 °C and ±0.1 V supply variations. To measure the transfer characteristics of the CF-NS TDC, a 10 MHz *Start* signal and a 10.0001 MHz *Stop* signal are applied to generate a ramp input. Due to the limited memory space of the test setup, the measurement is

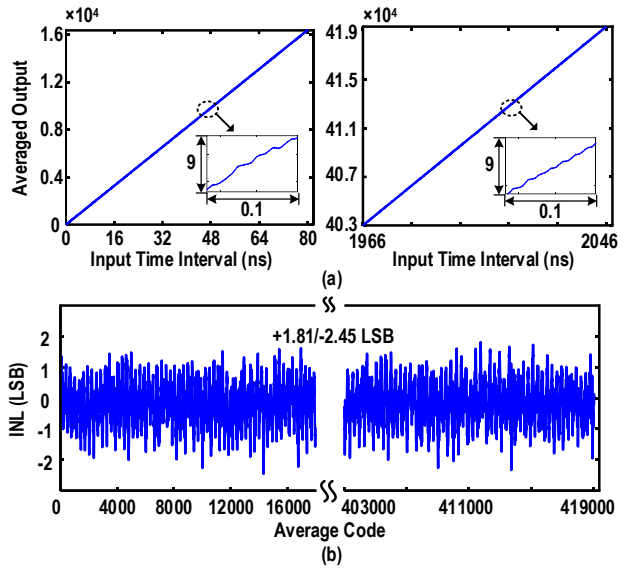

Fig. 11. Measured (a) transfer characteristics and (b) INL of the entire TDC.

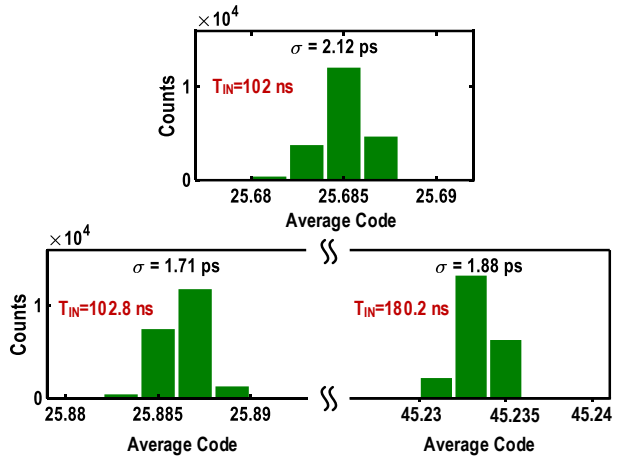

Fig. 12. Measured single-shot precision.

performed over two segments (i.e., 0-80 ns and 1966-2046 ns), as shown in Fig. 11(a). Assuming the TDC operates as a 14-bit converter after 100 kHz low-pass filtering, the INL is calculated to be +1.81/-2.45 LSB, as shown in Fig. 11(b). Fig. 12 shows the measured single-shot precision with about 32,000 samples in three different inputs, and the worst case standard deviation is less than 2.12 ps.

Table I summarizes the TDC performance. The proposed CF-NS TDC achieves a 5.03 ps resolution, a best single-shot precision of 2.12 ps and a 2046 ns dynamic range. Compared to state-of-the-art TDCs with comparable linearity, power and area for dToF applications, this design achieves the highest resolution and precision. FoM_1 and $FoM_{2\pi}$ [4] have been defined to ensure a fair evaluation of TDC performance. The proposed TDC achieves the best FoM_1 and $FoM_{2\pi}$ among the comparable TDCs reported for dToF applications.

IV. Conclusion

This paper presents a CF-NS TDC that achieves high resolution while extending the input dynamic range. The proposed design employs a two-stage quantization scheme, where a compact VCSRO-based sub-TDC is used for fine quantization to achieve picosecond-level resolution and enhanced PVT robustness. Meanwhile, the coarse quantization stage confines the input of the VCSRO sub-TDC within a narrow range. Consequently, the proposed coarse-fine noise-shaping scheme effectively alleviates the tradeoff between input dynamic range and resolution in conventional noise-shaping TDCs. Compared with prior works for dToF applications with similar linearity, power, and area, the proposed TDC achieves superior resolution and precision, as well as the best FoM_1 and $FoM_{2\pi}$.

TABLE I. Comparison with State-of-the-Art TDCs

	JSSC' 2025 [1]	JSSC' 2023 [6]	TCAS1' 2025 [7]	ASSCC' 2023 [2]	This Work
Process [nm]	180	180	180	65	180
Application	dToF	dToF	dToF	dToF	dToF
Architecture	Cont. CNT + TA	GRO + Cont. CNT	TDL + TA	Phase-Domain ΔΣ	Cont. CNT + VCSRO
Resolution [ps]	7.9	100	16.5	8.5	5.03**
Range [ns]	2033.5	96	20	200	2046
F_S [MHz]	80	50	1	4	20
BW [MHz]	-	-	-	0.0625	0.1
$T_{int,rms}$ [ps]	-	-	-	7.2*	1.453
Precision [ps]	10.74	30	12.1	25	2.12
INL [LSB]	+0.69/-0.43	+1.4/−1.3	+2.83/-4.21	9.4	+1.81/-2.45
Area [mm²]	0.14	-	0.35	0.002	0.031
Power [mW]	10.8	15.9	0.434	0.136	3.35
#FoM_1 [×10⁹]	2.11	-	3.14	1.09	11.90
##$FoM_{2\pi}$ [dB]	-	-	-	134.48	137.52

*Estimated $T_{int,rms}=\sqrt{Resolution^2/12}$ **Estimated $Resolution=\sqrt{T_{int,rms}^2 \cdot 12}$

#$FoM_1=2^{N_{Linear}} \cdot F_S \cdot Range/(LSB \cdot Power \cdot Area)$

##$FoM_{2\pi}=DR+10log_{10}(BW/Power)$ [4] $DR=20log_{10}(T_{range,2\pi}/T_{int,rms})$

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