An 8-phase Dual-core Coupled Ring Oscillator with R-C Hybrid Tuning Technique Achieving 164.1dBc/Hz FoM at 1MHz Offset in 55nm FDSOI

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***Abstract*—This paper presents a dual-core coupled ring oscillator that achieves phase noise reduction and phase expansion to support low noise eight-phase clock outputs. A detailed analysis of the relationship between the oscillator stage and key parameters such as phase noise, power consumption, and oscillation frequency is provided, demonstrating that using a fewer-stage ring oscillator at a fixed frequency yields performance advantages. In addition, an R-C hybrid frequency tuning technique is employed to further improve phase noise performance and maintain stable FoM across the tuning range. Fabricated in a 55 nm FDSOI process, the proposed oscillator achieves an operating frequency range of 1.59–2.76 GHz while consuming 2 mW of power. The measured phase noise at a 1 MHz offset ranges from –99.7 dBc/Hz to –95.9 dBc/Hz, corresponding to an FoM of 162–164.1 dBc/Hz.**

Keywords—ring oscillator, multi-core, phase noise

I. Introduction

As the consumer electronics market continues to expand, ring oscillators have increasingly replaced traditional large-area *LC* oscillators as system clocks operating above the gigahertz range, owing to their compact size, cost efficiency, and strong process compatibility. Beyond those advantages, ring oscillators offer the benefit of multi-phase outputs, which are essential for half-rate and quarter-rate SerDes transceivers and for time-interleaved data converters. Moreover, in digital circuit integration, multi-phase clocks enable uniform clock-edge distribution, reducing the load and jitter within the clock tree [1]. However, the use of numerous active components introduces substantial noise, which degrades the RVCO's phase noise performance.

Recent researches have explored various methods to optimize ring oscillator noise performance. [2] proposes a differential two-stage ring oscillator to increase operating frequency, reduce power consumption, and generate orthogonal signals. By increasing the PLL bandwidth, this design achieves sub-picosecond jitter performance. However, the PLL bandwidth is constrained by the Gardner limit, limiting its applications. In [3], a reconfigurable time-interleaved VCO with phase synthesizer is proposed. Since the 35-stage oscillator operates at a low frequency with a low noise corner, the noise performance of the multiplied signal is improved. However, this approach is limited to odd-stage oscillators, which prevents the generation of binary phases. In [4], a multi-phase clock injection technique is proposed, where a 32-stage VCO generates a low-frequency pulse signal that is injected into the high-frequency 8-stage ring oscillator. While this method maintains multi-phase output and reduces noise, the need for multi-phase injection requires a long oscillator chain, which limits further frequency increasing. Moreover, such large-stage, long-chain VCOs, although beneficial for phase noise, typically result in increased area and power consumption. To address these challenges, this paper proposes a coupled dual-core ring oscillator. The proposed design generates low-noise signals above gigahertz using a two-stage ring oscillator with R-C hybrid tuning technique, while simultaneously producing eight-phase clock outputs through dual-core coupling.

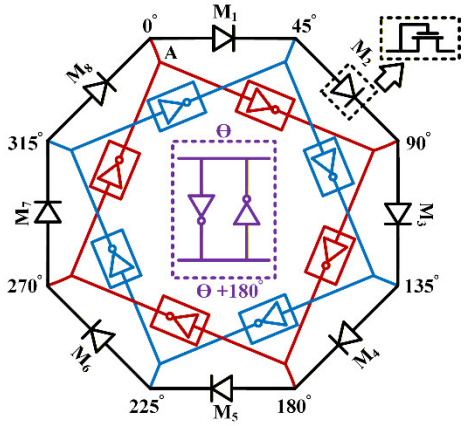

Fig. 1. Proposed dual-core coupled eight-phase ring oscillator.

This paper details the design methodology, structural features, and performance optimization strategies of the proposed VCO. The remainder of this paper is organized as follows: Section II introduces the fundamental principles of the proposed ring oscillator and analyzes the in-phase coupling network; Section III discusses the detailed design of the VCO core; Section IV presents the measurement results and performance analysis; and Section V concludes the paper.

II. Working Principle of the In-phase Coupling RVCO

A. In-phase Coupling Network

In RVCO feedback loops formed by inverter-based delay cells, an odd number of stages is typically required to prevent the circuit from settling at a DC point. However, an even number of delay cells can also form a differential ring oscillator by adding an additional latch at the output of each delay cell, thereby enabling oscillation. Fig. 1 shows the block diagram of the proposed dual-core coupled eight-phase ring oscillator. The architecture consists of two identical sub-ring oscillators, each implemented as a two-stage differential ring oscillator. These two sub-oscillators are interconnected through an external coupling network, which introduces a 45° phase shift between them. Combined with the inherent 90° phase difference of each two-stage differential oscillator, this configuration produces eight evenly spaced phase

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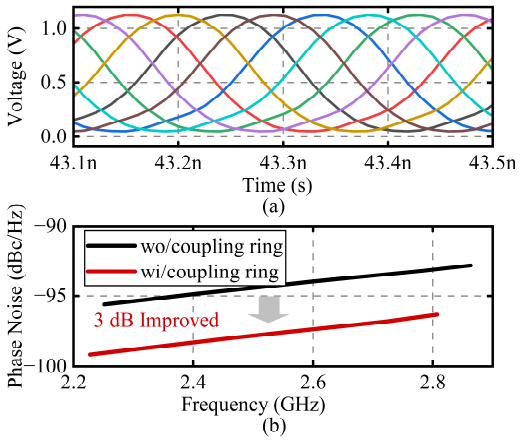

Fig. 2. (a) Output phase with thte coupling ring, (b) phase noise comparison.

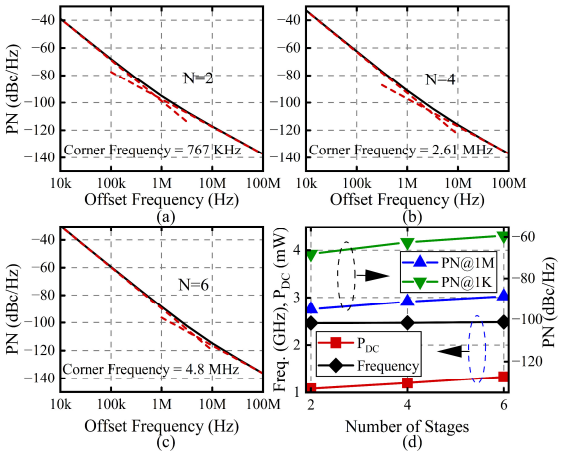

Fig. 3. Phase noise of a (a) 2-stage, (b) 4-stage, (c) 6-stage oscillator, (d) power consumption, phase noise, and frequency versus the number of stages.

outputs. The coupling network is composed of eight MOSFETs arranged in a diode-ring configuration, forming a closed loop that sequentially connects the eight output nodes of the oscillator. Once steady-state oscillation is reached, the coupler ensures stable generation of eight-phase outputs. Consider node A, which connects to two rectifiers and one oscillator port. At oscillation frequencies in the gigahertz range, the waveform of the ring oscillator more closely approximates a sine wave rather than a square wave [2]. Assuming the voltage at node A is $V_A\cos(\omega t)$, and the currents flowing through transistors M_1 and M_8 are given by:

$$I_{DS1} = gmV_A(\cos(\omega t) - \cos(\omega t + \pi/4)) \quad (1)$$

$$I_{DS8} = gmV_A(\cos(\omega t - \pi/4) - \cos(\omega t)). \quad (2)$$

In the above equations, *gm* represents the transconductance of the coupling transistor. The current injected into the oscillator is:

$$I_{inj} = I_{DS8} - I_{DS1} = gmV_A(\sqrt{2} - 2)\cos(\omega t). \quad (3)$$

As shown in (3), once the circuit reaches steady-state oscillation, the coupler injects a pure in-phase current into the oscillator node, free from DC or harmonic components. As a result, the coupler itself consumes no power and does not distort the oscillator waveform, thereby avoiding any phase noise degradation. Furthermore, the amplitude and phase of the injected current are independent of frequency, ensuring that the coupler does not alter the oscillation mode of the ring oscillator across the entire tuning range. Regarding noise performance, since the two sub-oscillators are synchronized through the coupler, the phase noise performance improves by 3 dB. This principle resembles that of the popular multi-core oscillators in *LC* oscillators [5], essentially representing a method to reduce phase noise.

B. Number of the Stages

The ring oscillator utilized in this work consists of two stages of differential delay cells. Typically, increasing the number of stages increases both area and power consumption while reducing frequency. Conversely, fewer stages minimizes both wiring parasitic and buffer parasitic in the delay elements, improving frequency and power efficiency [2]. However, as noted in [3] and [4], the 1/*f* noise corner frequency decreases with increasing number of stages. Thus, employing lower-stage ring oscillators incurs worse 1/*f* noise. Nevertheless, in a two-stage ring oscillator, the inherent 1/*f* noise can be effectively suppressed by increasing the device size, resulting in a reduced noise corner frequency. Fig. 3 compares the phase noise, power consumption, and noise corner frequencies of 2-, 4-, and 6-stage ring oscillators operating at similar frequencies. By proportionally enlarging the gate width and length of the MOS transistors in the 4- and 2-stage oscillators to match the oscillation frequency of the 6-stage configuration, the noise corner frequency decreases from 4.8 MHz to 2.61 MHz and 767 kHz, respectively. This confirms that enlarging the device area can effectively lower the noise corner frequency. At the same time, the 2-stage oscillator achieves a 0.25 mW power reduction and occupies only one-third of the area of the 6-stage design. Furthermore, due to the reduced noise corner frequency, the phase noise improves by 8.7 dB and 6.4 dB at 100 kHz and 1 MHz frequency offsets, respectively. Therefore, when maintaining a constant oscillation frequency, a larger-device, fewer-stage ring oscillator can deliver superior phase noise and power efficiency.

III. Circuit Implementation

Fig. 4 illustrates the two-stage differential ring oscillator circuit employed in this work. The two-stage differential ring oscillator can be viewed as an extension of a four-stage single-ended ring oscillator. The proposed design incorporates a PMOS cross-coupled pair, which forms a latch while simultaneously acting as the active load for the NMOS main buffer. Compared with the conventional inverter-based four-stage single-ended ring oscillator, this differential configuration features a simpler structure, effectively reducing parasitic capacitance and power consumption.

As reported in [2] and [6], enlarging the cross-coupled transistors injects additional noise into the loop—a phenomenon also observed in this design. As shown in the simulation results of Fig. 5(a), increasing the PMOS size causes a noticeable rise in the injected noise energy, thereby elevating the normalized noise level. Moreover, due to the lower carrier mobility of PMOS, larger transistor sizes introduce greater parasitic capacitance, resulting in a rapid frequency reduction and increased power consumption.

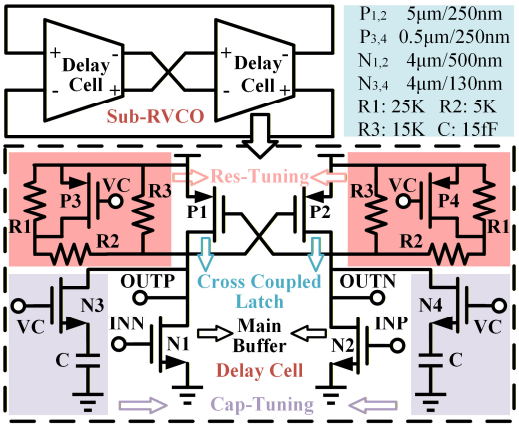

Fig. 4. Proposed two-stage differential ring oscillator.

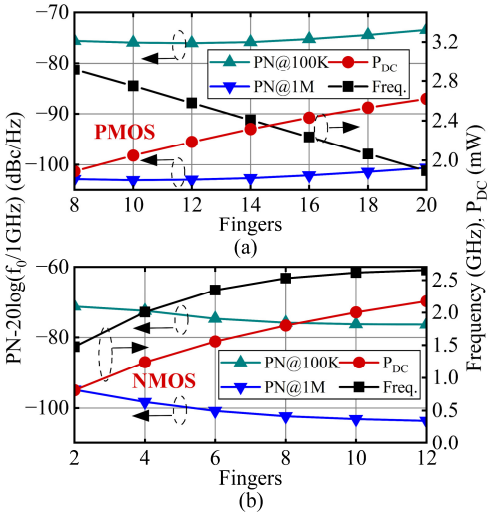

Fig. 5. Normalized phase noise, power consumption, and frequency versus (a) PMOS and (b) NMOS size.

Therefore, the PMOS size should be chosen such that the circuit avoids the zero-frequency latch-up point while maintaining reasonable noise performance. To enhance the circuit speed, the size of the main NMOS buffer can be increased. As shown in Fig. 5(b), enlarging the NMOS transistors can reduce circuit delay and increase oscillation frequency while simultaneously lowering normalized phase noise. However, excessive transistor scaling leads to startup difficulty and diminishing improvements in both frequency and phase noise, while power consumption continues to rise.

In conventional tuning methods, directly connecting a MOS transistor to the oscillator output node introduces significant 1/f noise into the VCO. Current-based tuning methods typically result in an excessively large K_{VCO}, which is unfavorable for system integration. Meanwhile, varactor-based tuning suffers from a limited linear voltage range. To address these limitations, this work proposes an R–C hybrid tuning scheme that achieves low K_{VCO}, low noise, and full-range voltage tuning. As shown in Fig. 4, a PMOS transistor together with three resistors forms a variable-resistance tuning network (RTN), while an NMOS transistor and a capacitor constitute a capacitive tuning network (CTN). When the control voltage varies from 0 to 0.6 V, the PMOS gradually turns off, increasing the equivalent impedance of RTN and thereby reducing the oscillation frequency. When

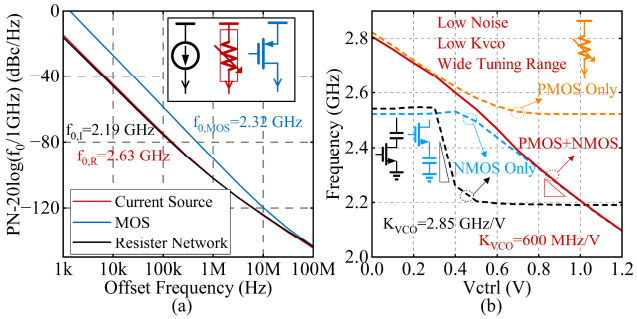

Fig. 6. (a) Phase noise and frequency comparison, and (b) VCO gain for different CTN connection configurations.

the control voltage varies from 0.6 to 1.2 V, the PMOS is fully turned off and the equivalent resistance of RTN remains constant, while the NMOS turns on. As a result, the effective capacitance seen at the output node increases with voltage, further lowering the oscillation frequency.

In the RTN, R1 improves the linearity of the impedance variation, R2 isolates the PMOS noise from the oscillator core, and R3 sets the initial oscillation frequency. By properly selecting the resistor values and PMOS size, both K_{VCO} and linearity of the tuning curve can be optimized. Fig. 6(a) compares the normalized phase noise under constant power consumption for three cases: the proposed RTN, a single PMOS, and an ideal current source. The results show that, at a 1 MHz offset, the proposed RTN achieves a 12 dB phase-noise reduction compared to the single-PMOS configuration. Even relative to the ideal current source, the degradation is limited to only 1.5 dB at low frequencies.

In the CTN, a capacitor-grounded configuration is adopted, such that the source voltage increases synchronously when the NMOS transistor turns on. This approach slows the variation of the equivalent impedance and effectively reduces K_{VCO}. Fig. 6(b) compares the frequency tuning characteristics of the two connection schemes. In the MOS-grounded configuration, the transistor rapidly enters strong inversion after turn-on, causing the capacitor to be totally loaded at the output node. Further increases in control voltage result in negligible frequency change, leading to a high K_{VCO} of 2.85 GHz/V. In contrast, the capacitor-grounded configuration achieves the same tuning range while significantly improving the linearity of the tuning curve after turn-on, reducing K_{VCO} to 600 MHz/V. Such a low K_{VCO} is particularly beneficial for suppressing power supply and charge pump noise.

By properly selecting transistor sizes and capacitance values, the K_{VCO} of the CTN can be matched to that of the RTN, enabling a continuous, full-range, low-K_{VCO} tuning characteristic. The proposed R–C hybrid tuning scheme requires no additional active circuits, occupies a compact area, and exhibits excellent noise performance. Moreover, the power consumption remains nearly constant across the tuning range, resulting in a consistent FoM.

IV. Experimental Results

Fig. 7(a) shows a micrograph of the proposed dual-core coupled ring oscillator, fabricated in a 55 nm FDSOI process. The active area occupies only 0.002 mm², which is comparable to that of a conventional four-stage differential ring oscillator. Fig. 7(b) presents the measured phase noise at

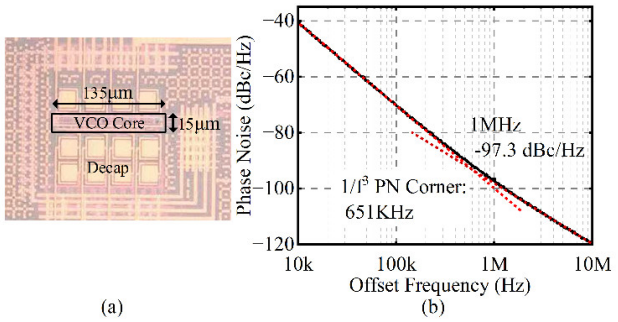

Fig. 7. (a) Chip micrograph and (b) measured phase noise.

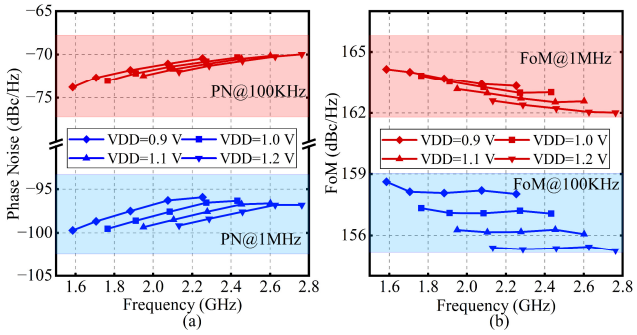

Fig. 8. Measured (a) PN and (b) FoM at 100 kHz and 1 MHz offset versus the carrier frequency.

a 2.7 GHz carrier frequency under a 1.2 V supply voltage. The VCO exhibits a noise corner frequency of only 651 KHz, achieving a phase noise of –97.3 dBc/Hz at a 1 MHz offset, with a power consumption of only 2 mW.

The proposed frequency tuning method achieves a 25.8% tuning range at 1.2 V supply voltage. The frequency range can be further extended by adjusting the supply voltage. When the supply voltage is reduced by 25%, the total frequency coverage expands to 54.4%, and significant overlap can be observed between the various tuning curves. Fig. 8 illustrate the phase noise and FoM of the VCO at different frequencies. At a 100 kHz offset, the measured phase noise ranges from –70 to –73.8 dBc/Hz, while at a 1 MHz offset, it ranges from –95.9 to –99.7 dBc/Hz. Owing to the R-C hybrid tuning technique, the FoM variation within a single frequency band remains within 1 dB, with the overall FoM spanning 162–164.1 dBc/Hz. However, FoM variations across different frequency bands, evaluated at a 100 kHz offset, are more pronounced. This is mainly attributed to the differing 1/*f* noise corners of the transistors under varying supply voltages, leading to noticeable differences in close-in phase noise [3]. Consequently, the lower-VDD frequency bands in Fig. 8(b) exhibit better FoM performance.

Table 1 summarizes the performance of the proposed ring oscillator and compares it with previously reported designs. The results demonstrate that the proposed oscillator achieves excellent FoM, compact area, and low power consumption, while also supporting multi-phase clock outputs.

V. Conclusion

This work presents a dual-core ring VCO implemented in a 55 nm FDSOI process, utilizing a passive coupling network to achieve low phase noise and eight-phase clock outputs. The frequency-independent coupling network injects in-phase current into the oscillator output nodes without introducing additional power consumption, effectively enhancing phase noise performance. For the VCO core, an R-C hybrid tuning technique is proposed to extend the oscillation frequency and the voltage tuning range while maintaining low phase noise. It ensures a consistent FoM across the entire tuning range and reduces K_{VCO} without sacrificing frequency coverage.

TABLE I. Performance Summary and Comparison

	TCASII'19 [7]	MWCL'20 [8]	JSSC'16 [9]	TCASII'23 [4]	**This Work**
Process	65nm CMOS	180nm CMOS	45nm CMOS	65nm CMOS	**55 nm FDSOI**
Freq. (GHz)	2.68~3.56	1.78~2.53	2-3	1.91~3.79	**1.58~2.76**
TR (%)	28.2	34.8	40	66	**54.4**
PN@1MHz (dBc/Hz)	-95.8/-93.5	-94.6/-92.7	-96	-96.2	**-99.7/-95.8**
FoM@1MHz (dBc/Hz)	159.4~160	145~146.3	158.7	159~160	**162~164.1**
P_{DC} (mW)	3.23	28	3.1	3.57	**2**
Area (mm^2)	0.0017	0.015	0.001	0.003	**0.002**
Eight-Phase Output	Yes	Yes	NO	Yes	**Yes**

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