A 96.6%-Peak-Efficiency 4.63-A/mm^3-Peak-Density Resonant-Tank Converter with RDL Trace Inductor and Trajectory Control for Vertical Power Delivery

Xuliang Wang[1], Zhoutong Liu[1], Yuan Yao[2], Weiping Wu[3], Junmin Jiang[4], Yan Wang[1], and Xiaosen Liu[1]
[1]Tsinghua University, BNRist, Beijing, China, [2]The Hong Kong University of Science and Technology, Hong Kong SAR,
[3]College of Semiconductors (College of Integrated Circuits), Hunan University, Changsha, China,
[4]Southern University of Science and Technology, Shenzhen, China
Email: xwangef@tsinghua.edu.cn, liuxiaosen@tsinghua.edu.cn

***Abstract*—A resonant-tank converter with RDL trace inductor and Phase-Shifted Trajectory Control is proposed to achieve ultra-high-density vertical power delivery for high-performance computing (HPC). Fabricated in a 65-nm CMOS process with flip-chip assembly, it achieves 96.6% peak efficiency and 4.63-A/mm^3 peak density with stable closed-loop regulation.**

***Index Terms*—Resonant-tank converter, RDL trace inductor, trajectory control, vertical power delivery**

I. Introduction

With the rapid emergence of versatile AI technologies and the proliferation of digital content, a revolutionary power supply architecture is pivotal for powering large-scale, high-performance computing (HPC) processors. Regarding point-of-load (PoL) conversion, the ever-increasing and dynamically changing HPC power requires both high power density and rapid load response. A ring-type converter architecture is gaining significant attention for its inherent current balance and scalability [1]–[3]. However, excessive use of bulky, high-Q inductors poses substantial integration challenges for vertical power delivery (VPD). In this paper, a Stacked-Ladder Resonant-Tank converter (ReLA) with vertical scalability fundamentally resolves the VPD integration challenge. As shown in Fig. 1(a), the proposed ReLA is fully packaged in a 2.5D flip-chip assembly, with flying/decoupling capacitors and RDL trace inductors vertically integrated into an ultra-thin interposer. It can also be configured as a 3D architecture (Fig. 1(b)), thereby reducing regulation latency and IR drop. Furthermore, the proposed ReLA also provides lateral scalability through a ring-type extension.

II. Overall Architecture

Fig. 2 illustrates the overall architecture of the proposed ReLA ring, where every two adjacent phases are paired with complementary current flows for cross-phase charge balance without mid-rail DC capacitors (C_{MID}). A shared back ring enables one-shot activation/deactivation of ReLA phases at the zero-current crossing (ZCS) points. Furthermore, the ReLA ring can be reconfigured into "Boost" or "Buck" trajectory-control modes using high-frequency phase-shift modulation to maintain a stable V_{OUT}. Furthermore, the phase-shift information is fed forward to regulate the IBC bus voltage (V_{BUS}) and retain the nominal voltage conversion ratio (VCR), thereby maintaining ultra-high steady-state efficiency [4].

This work was supported by BNR2026RC01013, the National Natural Science Foundation of China (NSFC) under Grant 62374100, and the Beijing Municipal Natural Science Foundation under Grant 4244106. *Corresponding Author: Xiaosen Liu.*

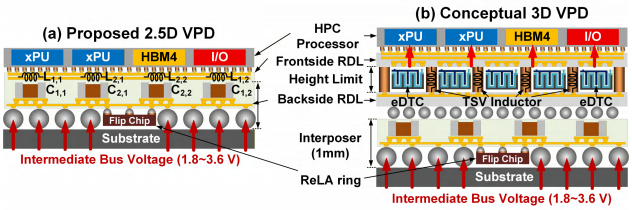


Fig. 1. (a) Proposed 2.5D VPD architecture using RDL trace inductors; (b) Conceptual 3D VPD architecture built of TSV inductors & DTCs.

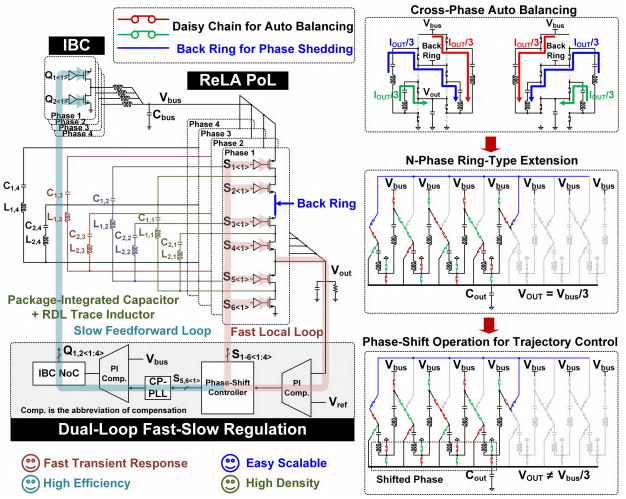


Fig. 2. Overall architecture of the proposed ReLA ring (left); proposed cross-phase auto-balancing, N-phase ring-type extension, and phase-shift operation for trajectory control (right).

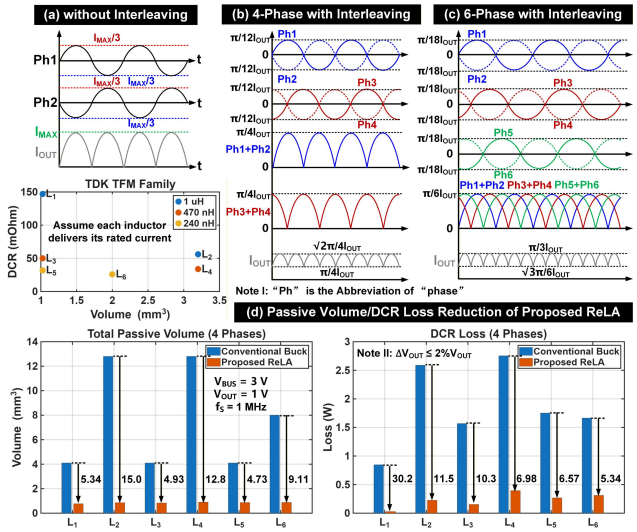


Fig. 3. (a) Conceptual waveforms (a) without phase interleaving, (b) with 4-phase interleaving, and (c) with 6-phase interleaving. (d) Passive volume/DCR loss reduction of the proposed ReLA ring.

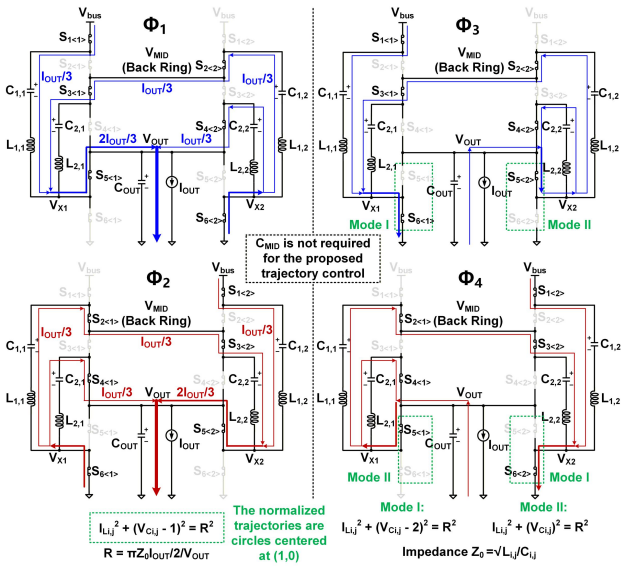


Fig. 4. Proposed nominal switching states (left) and those for phase-shift operation (right) with corresponding trajectory equations.

III. Interleaved Ripple Suppression

Fig. 3(a) shows the conceptual waveform of the proposed ReLA under complementary two-phase operation. The cross-phase auto-balance enables finer current splitting than conventional resonant topologies [5]–[7], thereby achieving a current reduction ratio (I_L/I_{OUT}) of 2/3N (N = $2, 4, 6, \cdots$). With N-phase interleaving, the proposed ReLA ring achieves similar ripple cancellation as a conventional multi-phase Buck (MPB) converter (Fig. 3(b-c)). By using RDL trace inductors, the proposed ReLA ring achieves up to 15(30) times reduction in total passive volume (DCR loss) compared to MPB under the same V_{OUT} ripple constraint and rated I_L (Fig. 3(d)).

IV. Phase-Shifted Trajectory Control

Fig. 4 shows the proposed nominal switching states and those for phase-shift operation (Mode I/II). The conceptual waveforms of "Boost" and "Buck" operating modes are illustrated in Figs. 5(a) and 5(b), respectively. While the equivalent trajectories of nominal operation are circles centered at (1,0) on the state plane [8], the proposed phase shift operation (Mode I/II) evokes cross-circle leaps centered at (2,0) or (0,0). As a result, the proposed Phase-Shifted Trajectory Control compensates for load-regulation damping and maintains the target V_{OUT} regardless of the varying I_{OUT}.

V. Modular Handshake Driving

To fully exploit the intrinsic DC rails of the ReLA topology, a Modular Handshake Driving technique is proposed as shown in Fig. 6(a). The gate-driving signals for each CMOS pair are fed back locally (inner loop) and combined with the level-shifted turn-on/off signals to enable non-overlapping switching. In the outer loop, the raw turn-off signals are generated in the core-voltage domain and level-shifted upward

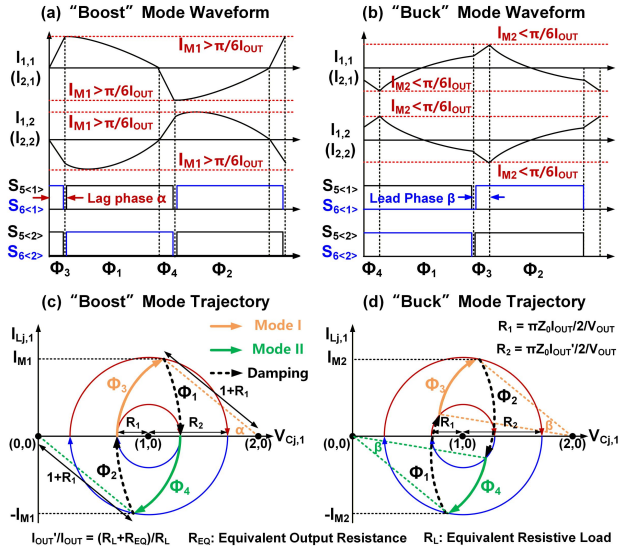


Fig. 5. Conceptual waveforms of (a) "Boost" mode & (b) "Buck" mode, and trajectories of (c) "Boost" mode & (d) "Buck" mode.

in the same direction as the voltage stacking. Then, the gate-driving signals at the highest stack level are level-shifted in the opposite direction to ensure non-overlapping switching between inter-level power switches. By using the Vertical Scalable Level Shifter [9], the proposed ReLA is implemented by low-voltage devices exclusively (Fig. 6(b)). Furthermore, a phase-shedding arbiter, cooperated with the proposed daisy chain configuration, enables one-shot activation/de-activation of ReLA phases at the ZCS points (Fig. 6(c)).

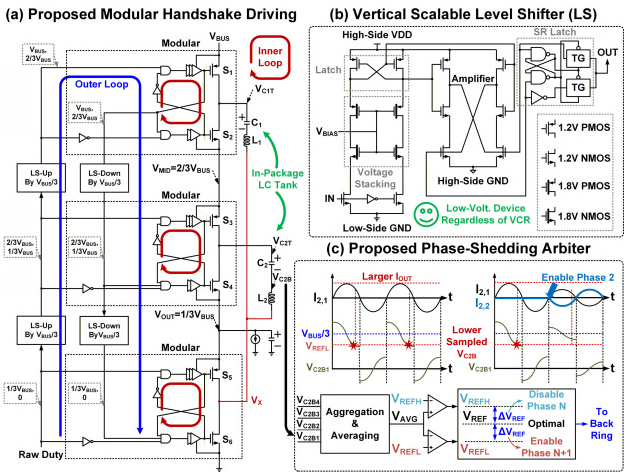
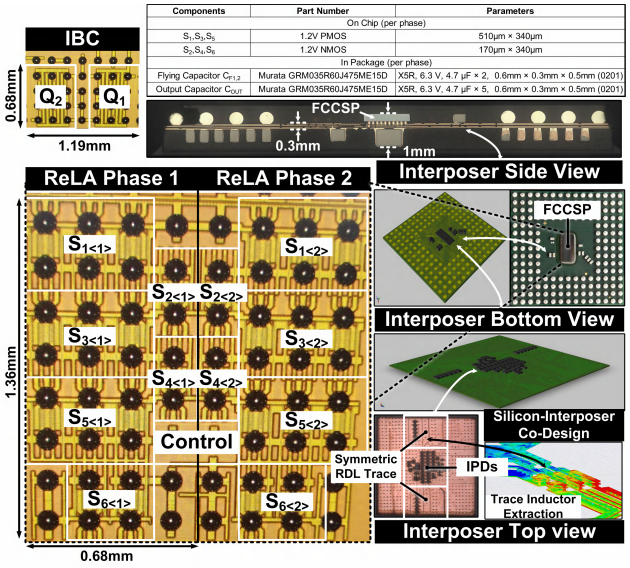


Fig. 6. (a) Proposed Modular Handshake Driving technique for ReLA ring; (b) Vertical scalable level shifter for power-stacking module; (c) Proposed one-shot phase-shedding arbiter.



Components	Part Number	Parameters
On Chip (per phase)		
S_1, S_2, S_5	1.2V PMOS	510μm × 340μm
S_3, S_4, S_6	1.2V NMOS	170μm × 340μm
In Package (per phase)		
Flying Capacitor $C_{FLY1,2}$	Murata GRM035R60J475ME15D	X5R, 6.3 V, 4.7 μF × 2, 0.6mm × 0.3mm × 0.5mm (0201)
Output Capacitor C_{OUT}	Murata GRM035R60J475ME15D	X5R, 6.3 V, 4.7 μF × 5, 0.6mm × 0.3mm × 0.5mm (0201)

Fig. 7. On-chip/in-package component list of the proposed ReLA (top), FCCSP die (left), and interposer photos (right).

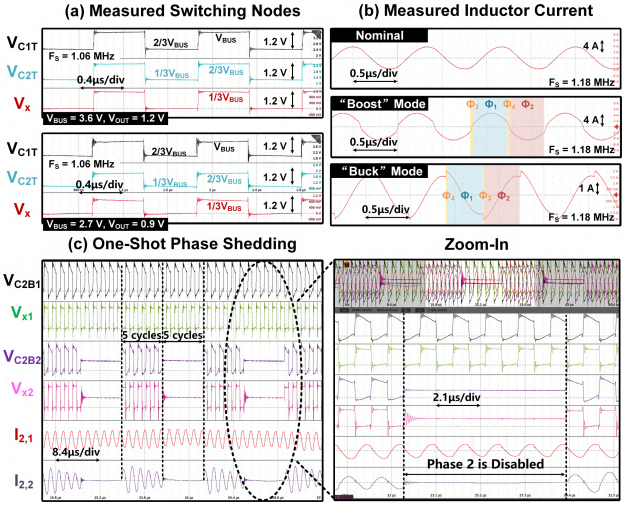


Fig. 8. (a) Measured steady-state switching-node voltages; (b) Measured inductor current waveforms in different operating modes; (c) Measured one-shot phase shedding at the ZCS points.

VI. Measurement Results

Fig. 7 shows the FCCSP die photo of the proposed ReLA. The inter-phase power traces are symmetrically redistributed to the integrated passive devices (IPDs). Each RDL trace inductor is tuned at a nominal value of 5.6 nH through silicon-interposer co-design, and the estimated ACR at 1 MHz is 7.9 mΩ. To comply with the 1-mm interposer height constraint, flying/decoupling capacitors are all in 0201 footprints.

Fig. 8(a) shows the measured steady-state waveforms of the switching nodes. The measured inductor waveforms under nominal, "Boost", and "Buck" operating modes are highly consistent with the theoretical analysis (Fig. 8(b)). As shown in Fig. 8(c), the phase-shedding command is issued every five switching cycles. At the ZCS point, the number of activated ReLA phases is adjusted in a single shot, as expected.

Under 4-phase interleaved operation, the V_{OUT} ripple is approximately reduced by half compared to that under 2-phase operation (Fig. 9(a)). Fig. 9(b) shows the measured transient waveforms with a 1-A I_{OUT} step. With the proposed Phase-Shifted Trajectory Control, the V_{OUT} undershoot and overshoot are clamped within 127.5 mV and 129.6 mV, respectively. At the nominal VCR, the proposed ReLA ring achieves peak power conversion efficiencies (PCE) of up to 96.6% (Fig. 9 (c)), with V_{OUT} varying from 0.8 V to 1.2 V. The 2-phase prototype delivers a maximum I_{OUT} of 4.23 A at a V_{OUT} of 1.2 V and sustains 79.5% PCE under full load.

Fig. 10 and Table I compare state-of-the-art (SOTA) high-density PoL designs [4], [10]–[13]. The proposed ReLA ring achieves the best peak density of 1.66 A/mm^2 (equivalent to 4.63 A/mm^3) and a comparable peak PCE of 96.6%.

References

[1] Z. Tong *et al.*, "HOOP: A Scalable Hybrid DC-DC Converter Ring for High-Performance Computing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 1-3.

[2] J. Yang, R. P. Martins, and M. Huang, "A Segmented-Interlacing Multi-Phase Hybrid Converter with Inherently Auto-Balanced I_Ls and Boosted I_L Slew Rate During Load Transients," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 378-380.

[3] J. Yang, Z. Tang, R. P. Martins, and M. Huang, "A Multi-Phase Hybrid Converter with Q Samplers Enabling Simultaneous I_L Auto-Balance and Arbitrary Phase Count," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2026, pp. 450-452.

[4] S. Ren *et al.*, "A 12A 89.3% Peak Efficiency and 26mV Undershoot 12-to-1V Two-Stage Converter with Regulated Resonant Switched-Capacitor Regulators," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 374-376.

[5] C. Schaef, K. Kesarwani, and J. T. Stauth, "A variable-conversion-ratio 3-phase resonant switched capacitor converter with 85% efficiency at

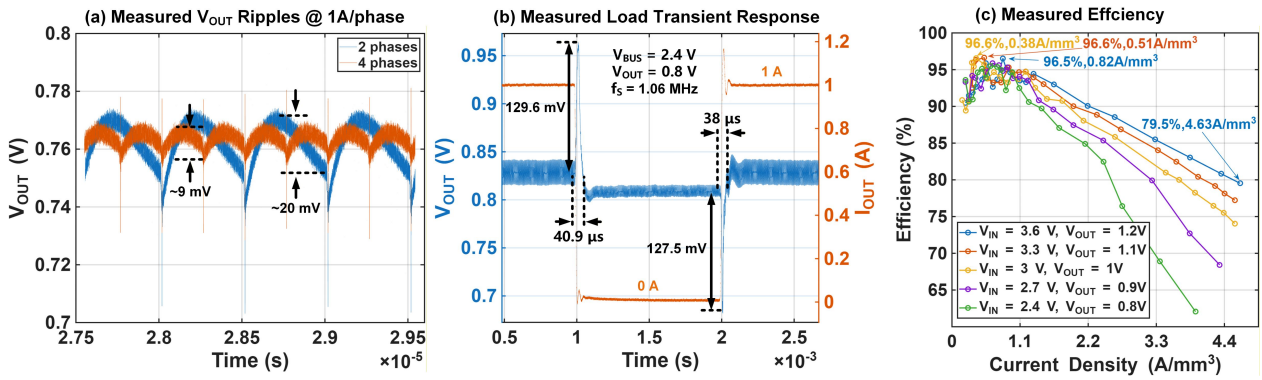


Fig. 9. (a) Measured V_{OUT} ripple suppression with phase interleaving, (b) measured 1-A load transient response, and (c) measured efficiencies with scaled V_{OUT} and current densities.

TABLE I
COMPARISON WITH STATE-OF-THE-ART (SOTA) POL DESIGNS.

	ISSCC'22 [10]	VLSIC'23 [11]	VLSIC'24 [12]	ISSCC'24 [13]	ISSCC'25 [4]	**This Work**
Process	180nm BCD	180nm BCD	180nm BCD	28nm	65nm	**65nm**
Topology	Parallel SC	OISC	ABDP	Parallel SC	Resonant SC	**ReLA**
V_{BUS} (V)	3-4.2	1.5-3.3	1.8	3-3.6	2	**1.8-3.6**
V_{OUT} (V)	0.6-1	0.8-1.8	0.2-1.5	0.6-1	0.6-1	**0.6-1.2**
f_{SW} (MHz)	2	1 or 2	1	2	9	**1.06 - 1.18**
No. of Phases	1	2	1	1	6	**2,4,6**
Max. I_{OUT} (A)	1.2	1.55 (per phase)	2.5	1.5	2 (per phase)	**2.12 (per phase)**
Inductor Value	470 nH	1 µH	470 nH	560 nH	850 pH	**5.6 nH**
Inductor DCR	N.R.	144 mΩ	N.R.	N.R.	N.R.	**7.9 mΩ**
Inductor Type	SMD	SMD	SMD	SMD	PCB Trace	**RDL Trace**
Inductor Volume	1.02mm³	2mm³	1.02mm³	1.02mm³	N.A.	**N.A.**
I_L/I_{OUT}	1/(1+2D) or 1/(1+D)	1/2/(2-D)	Fixed 2/3	2/(3D+2)	No	**2/3 @ 3:1**
C_{FLY} (per phase)	2 × 4.7 µF	2 × 4.7 µF	2 × 10 µF	10 µF + 2 × 4.7 µF	1 µF	**2 × 4.7 µF**
C_{OUT} (µF)	10 µF	0	10 µF	10 µF	2 × 10 µF	**5 × 4.7 µF**
Peak Efficiency	92.9%	97.3%	94.2%	94.1%	96.0%	**96.6%**
V_{IN} (V) & V_{OUT} (V)	3 & 0.8	3.3 & 1.8	1.8 & 1.2	3.3 & 1	2 & 1	**3 & 1**
Efficiency	82.0%	90.1%	75.0%	82.0%	84.0%	**79.5%**
I_{MAX} & V_{OUT}	1.2A & 0.6V	3.1A & 1.8V	2.5A & 0.9V	1.5A & 0.6V	6A & 0.6V	**4.23A & 1.2V**
Die Area (per phase)	2.72 mm²	3.81 mm²	4 mm²	3.08 mm²	1.06 mm²	**0.93 mm²**
Total Area[a] (per phase)	4 mm²	12.19 mm²	6.28 mm²	5.64 mm²	1.56[b] mm²	**1.28 mm²**
Max. Current Density	0.3 A/mm²	0.25 A/mm²	0.398 A/mm²	0.266 A/mm²	1.282 A/mm²	**1.656 A/mm²**

[a]Total Area = Die Area + Inductor Area + C_{FLY} Area
[b]Assume 0204 Capacitor is Used

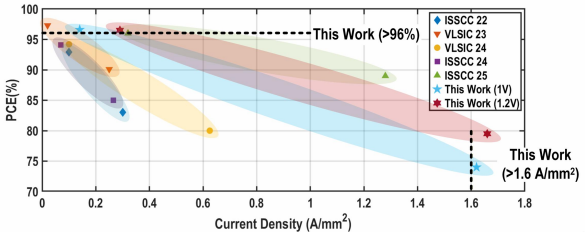


Fig. 10. Efficiency/density trade-offs of SOTA designs.

0.91W/mm² using 1.1nH PCB-trace inductors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1-3.

[6] D. -Y. You, H. -J. Chiu, and S. -H. Kuo, "Ladder-Type Resonant Switched-Capacitor Converter Achieving 99.1% Peak Efficiency and 4750 W/in³ Power Density for High-Current Application," *IEEE Trans. Power Electron.*, vol. 39, no. 7, pp. 8040-8053, Jul. 2024.

[7] G. Ripamonti *et al.*, "A Monolithic Regulated 160 MHz Resonant DC-DC Converter," in *IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2025, pp. 479-484.

[8] H. T. W. Ma Yang, L. Wang, H. Wang, and W. T. Ng, "A Trajectory Controlled 48-to-24 V Resonant Switched Capacitor Converter with 98.7% Efficiency and Ultrafast Dynamic Response," in *IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2025, pp. 983-989.

[9] X. Liu *et al.*, "A Monolithic 5.7 A/mm² 91% Peak Efficiency Scalable Multistage Modular Switched Capacitor Voltage Regulator for Base Die Vertical Power Delivery in 3D-ICs," *IEEE J. Solid-State Circuits*, vol. 60, no. 4, pp. 1265-1276, Apr. 2025.

[10] G. Cai, Y. Lu, and R. Martins, "A Battery-Input Sub-1V Output 92.9% Peak Efficiency 0.3A/mm² Current Density Hybrid SC-Parallel-Inductor Buck Converter with Reduced Inductor Current in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 312-314.

[11] X. Zhang et al., "A 0.05-to-3.1A 585mA/mm³ 97.3%-Efficiency Out-phase Switched-Capacitor Hybrid Buck Converter with Relieved Capacitor Inrush Current and C_{OUT}-Free Operation," in *IEEE Symp. VLSI Tech. Circuits*, Jun. 2023, pp. 1-2.

[12] D. -H. Kim, J. -H. Cho, H. Han, and H. -S. Kim, "A 1.8V-Input 0.2-to-1.5V-Output 2.5A 930mA/mm³ Always-Balanced Dual-Path Hybrid Buck Converter with Seamlessly All-VCR-Coverable Tri-Mode Operation," in *IEEE Symp. VLSI Tech. Circuits*, Jun. 2024, pp. 1-2.

[13] H. Han, J. -H. Cho, W. Jang, Y. Park, J. Lee, and H. -S. Kim, "A 94.1%-Efficiency Parallel-SC Hybrid Buck Converter Designed Using VCR-Aware Topology Optimizer for a 4.2A/mm² Current-Density FoM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 464-466.