A 200-MHz Bandwidth, OSR=6, 2–0 MASH CT DSM Employing a 4xTI SAR Quantizer

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***Abstract*—Delta-Sigma modulators (DSMs) are inherently constrained by the oversampling ratio (OSR) determining the balance between bandwidth and resolution. As the achieved bandwidth of wideband continuous-time (CT) DSMs has been saturating, techniques to allow lower OSR while maintaining decent resolution and the CT input are required. In this work, a second-order CT DSM in Leslie-Singh architecture is realized achieving 200 MHz bandwidth with OSR = 6. The design incorporates a Flash quantizer (QTZ) inside the DSM loop and a 4x time-interleaved (TI) successive-approximation-register (SAR) QTZ as zero-order second stage. The Flash QTZ output is used to preload the TI SAR, implicitly extracting the residue and realizing an inter-stage gain (ISG) for further quantization. Implemented in 22 nm FDSOI and operating from 0.9 V, the DSM achieves 162 dB Schreier figure of merit (FoM$_S$), 65 dB signal-to-noise-and-distortion ratio (SNDR), and 66 dB dynamic range (DR).**

***Index Terms*—ADC, CT, DSM, MASH, TI, SAR, Flash**

I. Introduction

CT DSMs are a popular choice for wireless receiver analog-to-digital converters (ADCs), as they offer easy drivability due to their resistive input, as well as implicit signal and anti-aliasing filtering (AAF) [1], [2]. In recent years, the advancement towards ever wider bandwidths of CT DSM has somewhat stalled. For single-loop DSMs as in Fig. 1(a), this is due to the limited loop-filter order and stability constraints, as well as the required OSR which leads to excessively high sampling frequencies. Increasing the internal QTZ resolution is possible, but exponentially increases the complexity of the QTZ and feedback digital-to-analog converter (DAC) and its linearization, which is why highest-linearity designs partially restrict the bitwidth to as low as two [3]. Furthermore, excess loop delay (ELD) becomes a limiting factor when high internal resolution is used, since Flash QTZs become impractical for resolutions larger than 4-bit, and SAR QTZs operate sequentially with high latency.

Alternatively, CT DSMs with hundreds of MHz bandwidth have been realized as multistage noise-shaping (MASH) CT DSMs, cf. Fig. 1(b) [2], [4]–[6]. Although they achieve efficient high-order noise-shaping, even at low OSR, they suffer from noise-leakage due to static and dynamic mismatch between analog loop filter and digital noise cancellation filter (NCF). Moreover, while the resolution can be improved by high inter-stage gain (ISG) in an ideal MASH DSM, non-idealities limit the ISG in practice [4], [6].

A recent alternative are continuous-time pipelined (CTP) ADCs, which achieve wideband operation using low OSR $\approx 3..5$ [7]–[10]. Even though they achieve bandwidths exceeding 1 GHz, this comes at the cost of very precisely trimmed delay matching in the residue generation path to maximize the possible ISG [2], [9], as well as excessive foreground calibration to eliminate the NCF mismatch [9], [11].

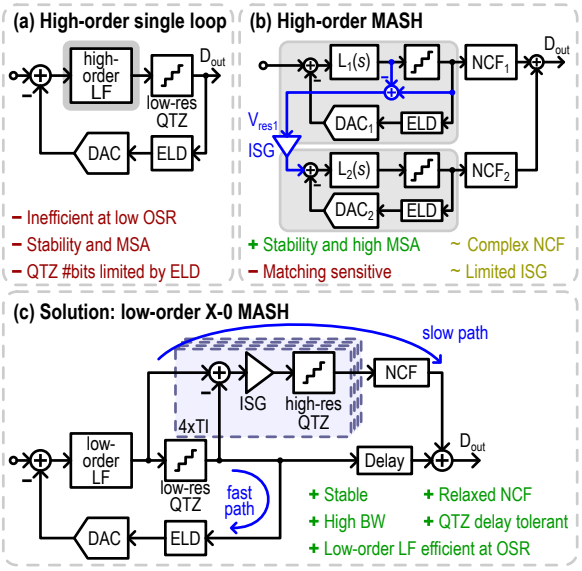

Fig. 1: Design approaches for wideband CT DSMs at low OSR.

Alternatively, the resolution of a low-order, low-bitwidth, and low-OSR single-loop DSM can be increased by outsourcing the high-resolution quantization from within the DSM feedback loop to the backend. This is known as an X–0 MASH or Leslie-Singh architecture [12]. An early implementation of this idea was presented in [13], where a 2–0 MASH switched-capacitor DSM was realized for a 1.25 MHz bandwidth with a low OSR = 8. The DSM employed a 5-bit Flash QTZ, whose quantization error was explicitly extracted and re-quantized by a 4-stage, 12-bit pipelined ADC. This allowed to operate the pipelined QTZ outside the DSM loop, where its high latency is tolerable. Similarly, [14] worked on how a TI high-resolution QTZ could be incorporated within a DSM, and beyond others, analyzed a TI QTZ as second stage of a Leslie-Singh DSM [14, Sec. II-A]. In this work, we combine both ideas to the proposed architecture shown in Fig. 1(c) to realize a 200 MHz bandwidth CT DSM with OSR = 6.

The paper is organized as follows: Section II gives details on the architectural design, Section III describes the circuit-level realization, Section IV shows measurement results, and Section V concludes the paper.

II. Proposed System Architecture

Fig. 1(c) illustrates the architectural idea: a second-order multi-bit CT DSM is used in the first stage allowing for CT drivability and implicit AAF. The QTZ and DAC complexity are kept manageable by limiting the resolution inside the

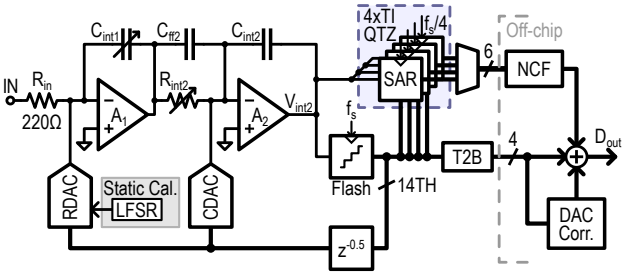

Fig. 2: Simplified schematic of the proposed 2–0 MASH CT DSM.

loop to approximately 4-bit. The Flash quantization error is extracted, amplified by an ISG and processed by the second stage. This stage uses a 4xTI SAR QTZ, as it achieves superior speed and efficiency in scaled technologies. Its latency is tolerated as it does not destabilize the DSM feedback loop.

A. Architectural Design

Fig. 2 shows more details of the proposed system. The DSM employs a cascade-of-integrators with distributed feedforward (CIFF) loop filter with two active RC integrators and a 15-level Flash QTZ. The outer feedback path is closed using a 15-level resistive DAC (RDAC). A direct feedback path compensating the ELD of $0.5\,T_s$ is realized using a capacitive DAC (CDAC) feeding into the second integrator. No resonator is used because of its limited signal-to-quantization-noise ratio (SQNR) benefit due to the low OSR and finite loop-filter gain at the band-edge.

The second stage 4xTI SAR QTZ is based on the design of [15]. Both, the in-the-loop 15-level Flash QTZ and the SAR CDAC sample the second integrator's output V_{int2}. The Flash QTZ error is implicitly extracted by subtracting the Flash output from the sampled V_{int2} in the charge domain on the SAR CDAC. The asynchronous SAR (ASAR) QTZ realizes an implicit ISG and re-quantizes the amplified Flash QTZ error with 6-bit resolution. The complete QTZ operation is explained in detail in Section III-C.

The 2–0 MASH output D_{out} in Fig. 2 is finally formed by the sum of delayed thermo-to-binary-converted Flash output bits of the 1st stage and the TI SAR output bits of the second stage filtered by the NCF. The second-order DSM with 15-level Flash QTZ achieves an SQNR of approx. 50 dB. By adding the second stage, this can be improved by approx. 30 dB, resulting in an ideal SQNR ≈ 80 dB for the 2–0 MASH architecture of Fig. 2.

B. Noise Cancellation Filters

The digital NCF in Fig. 2 is realized by a 10-tap FIR filter representing the impulse response of the analog noise transfer function (NTF). Since the 2–0 MASH architecture and the targeted signal-to-noise ratio (SNR) relax the matching requirements on the NCF accuracy, no calibration is required. Its coefficients are derived from a nominal layout-extracted loop-filter impulse response simulation and are kept constant for all measurements. For testing flexibility, the NCF was implemented off-chip.

III. Circuit Implementation

A. Feedback DACs

The RDAC in the outermost feedback path in Fig. 2 consists of 14 unit elements. The Flash outputs are latched in the unit elements after half a clock cycle realizing the ELD of $0.5\,T_s$. The output driver is an inverter connected to the references $V_{refp/n}$, which are externally provided in this prototype. As unit-element mismatch in the RDAC leads to strong non-linearity of the overall CT DSM, static DAC error correction is implemented. It is realized by successively inserting an LFSR-based pseudo-random sequence through all unit elements. This allows for a digital correlation of the DSM output with the LFSR sequence enabling a deterministic estimation of all unit element mismatches and their digital correction [16].

The CDAC unit element for the ELD compensation DAC in Fig. 2 consists of a simple latch, which drives a capacitor to VDD/GND and offers a 4-bit ($\pm 20\,\%$) trim option to calibrate against process variation of the loop filter.

B. Loop Filter

Both integrators are realized as active RC integrators using two-stage Miller-compensated OpAmps with class-AB output stages. The OpAmps achieve a DC gain of 60 dB / 57 dB for the first and second OpAmp, respectively, and both feature a closed-loop unity-gain frequency of 3 GHz. The loop-filter RC time constants are trimmed at startup by adjusting C_{int1} and R_{int2} to counteract process variation [16].

C. 4-bit Flash and 6-bit 4xTI SAR QTZs

The Flash QTZ consists of 14 StrongARM latches with a switched-capacitor sampling front end to achieve inherent subtraction of input and reference voltages. Its reference levels are generated using a resistor ladder with a static current of 1 mA. A gain of 8/7 is implemented by scaling the Flash reference ladder to enable the residue extraction.

This is achieved by preloading the CDAC of the TI SAR QTZs as illustrated in Fig. 3. During the sampling phase, the second integrator's output V_{int2} is bottom-plate sampled on the 8-bit CDAC. After the 15-level Flash conversion of V_{int2} is finished, the 14 thermometer bits are preloaded on 14 thermometer-weighted capacitors of the CDAC and thereby subtracted from the sampled V_{int2} in the charge domain.

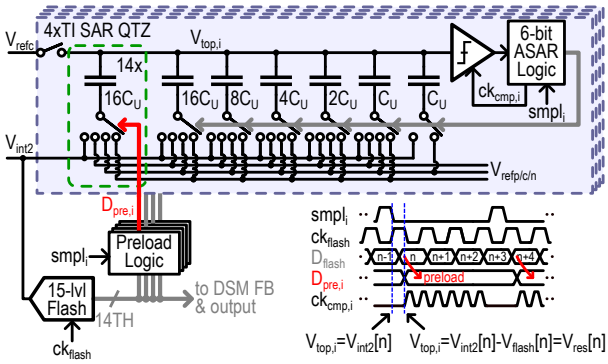

Fig. 3: Single-ended equivalent schematic of the internal 4xTI 6-bit SAR QTZ utilizing a 15-level Flash preload and Δ-length CDAC, based on [15].

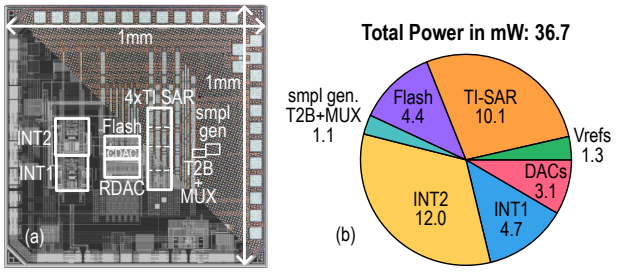

Fig. 4: (a) Chip photograph with layout overview. (b) Power breakdown.

This implicitly generates the Flash QTZ's residue on the CDAC top plate. The subsequent ASAR operation converts this residue signal, whereby its full-scale covers two least significant bits (LSBs) of the Flash full-scale. This enables to resolve an overranged Flash QTZ error up to $\pm 1\,\mathrm{LSB}|_{\mathrm{Flash}}$. Due to this weighting of the Flash vs. the ASAR part of the CDAC, an implicit ISG = 8 is realized.

For debugging purposes, the SAR references are supplied from off-chip, but are buffered on-chip. The sampling clocks $\mathrm{ck}_{\mathrm{Flash}}$ for the Flash and $\mathrm{smpl}_{\mathrm{i}}$ for the SAR QTZs are derived on-chip from the 2.4 GHz input clock.

IV. Measurement Results

The CT DSM prototype was fabricated in a 22 nm FDSOI technology and occupies an active area of 0.132 mm^2. It is clocked at 2.4 GHz achieving a bandwidth of 200 MHz with OSR = 6. A chip photograph and power breakdown are shown in Fig. 4. The reference voltages $V_{\mathrm{refp/n}} = 750\,\mathrm{mV} / 200\,\mathrm{mV}$ define the ADC differential peak-peak full scale of 1.1 V. To offer versatility for the measurements in this prototype, the references in each circuit block are separated and are either buffered on-chip (SAR) or provided externally (RDAC, Flash). All reference voltages across all circuit blocks are

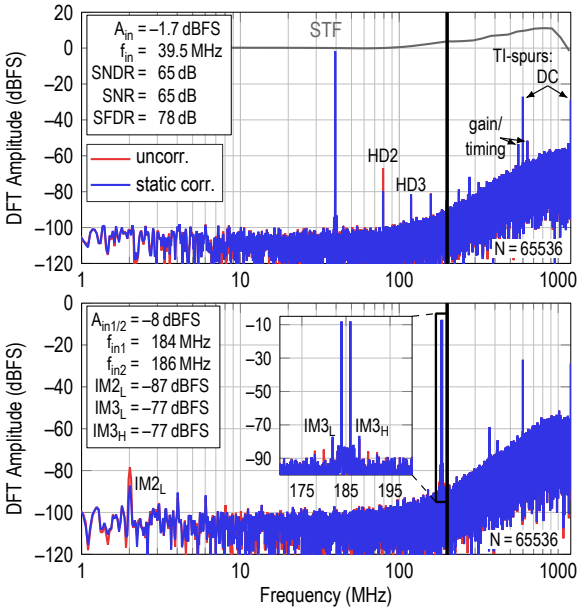

Fig. 5: Measured single-tone and two-tone output spectrum.

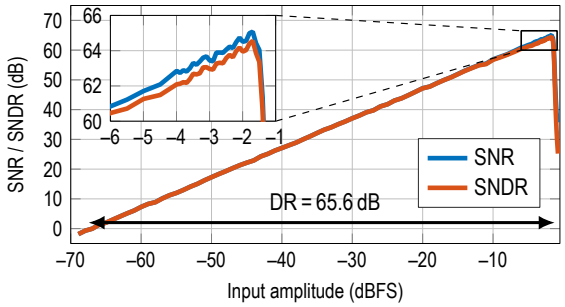

Fig. 6: Measured DR, SNR and SNDR with a 39.5 MHz input tone.

equal and within the supply rails and could be generated from the 0.9 V supply in future implementations.

Three chips were bonded into a QFN48 package and measured. Fig. 5 presents output spectra with a single-tone input signal at 39.5 MHz and a two-tone test near the band-edge, both with and without static RDAC correction.

The single-tone test reveals a SNDR of 65 dB. The spurious-free dynamic range (SFDR) is limited by the second-order harmonic caused by the thermometer-weighted outer RDAC. In a two-tone test, the CT DSM achieves an IM_3 of –77 dBFS. The out-of-band (OOB) spectrum shows TI spurs, which are expected due to uncorrected channel mismatch in the TI SAR QTZ. Although gain and timing mismatch spurs are visible at $\mathrm{f_s}/4 \pm \mathrm{f_{in}}$ and $\mathrm{f_s}/2 \pm \mathrm{f_{in}}$, the TI spurs are clearly dominated by DC offset channel mismatch, resulting in large spurs at $\mathrm{f_s}/2$ and $\mathrm{f_s}/4$. If these spurs became critical e.g. in presence of strong OOB blockers, a simple offset calibration of the TI SARs could be applied.

Fig. 6 shows the measured DR of 66 dB, as well as SNR/SNDR across different input signal amplitudes. The measured performance of 3 chip samples is shown in Fig. 7(a). Fig. 7(b) shows the robustness against a mismatch between analog loop filter and the digital NCF. For this, an analog NTF mismatch was introduced by intentionally de-tuning the first integrator's RC trim. Due to the Leslie-Singh architecture and the moderate SQNR requirements, the achievable in-band noise (IBN) is almost unaffected within a coefficient mismatch range of $\pm 10\,\%$.

Table I and Fig. 8 compare the proposed design with other wideband CT DSMs. It achieves a competitive $\mathrm{FoM_S}$ at the given bandwidth of 200 MHz with a low OSR of only 6 and, consequently, a low sampling frequency of only 2.4 GS/s.

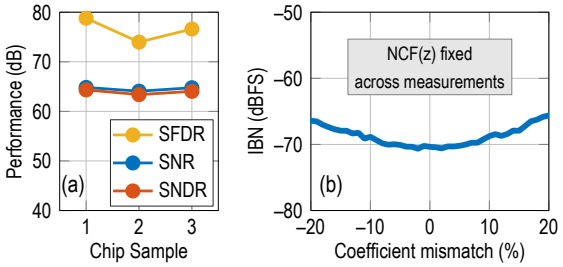

Fig. 7: (a) Measured performance of 3 chip samples and (b) achieved IBN in presence of loop filter coefficient mismatch.

TABLE I: PERFORMANCE COMPARISON WITH STATE OF THE ART CT DSM WITH >150 MHZ BANDWIDTH.

	This Work	[17]	[18]	[6]	[4]	[19]	[20]	[5]
Node (nm)	**22**	28	22	40	40	40	16	28
Area (mm^2)	**0.132**	0.126	0.06	0.21	1.34	0.45	0.155	1.4
DSM architecture	**2–0 MASH**	2xTI 3^{rd}-order	3^{rd}-order	1–1–1 MASH	2–1–1 MASH	3^{rd}-order	4^{th}-order	1–2 MASH
QTZ architecture	**Flash & 4xTI SAR**	2xTI Flash	Flash	Flash	2xTI Flash	2xTI Flash	Flash	Flash
QTZ #bits	**3.9–6**	4	4	3–3–3	3–3–3	3.8	5	4–4
Supply (V)	**0.9**	1.5/1.6/1.1	0.9/–0.5	1.8/1.1/1	1.8/1.1	1.1/1.95/–0.55	1.4/1.5/0.8	1/1.8/–1
f_s (GHz)	**2.4**	6.4	4.4	5	4	5	2.88	8
BW (MHz)	**200**	200	220	360	300	156	160	465
OSR	**6**	16	10	7	6.7	16	9	8.6
SNDR (dB)	**65**	72	62	65	60	64	65	68
DR (dB)	**66**	77	63	68	65	70	72	72
P (mW)	**36.7**	106	22	158	506	233	40	890
FoM_S (dB)	**162**	164	162	159	148	152	161	154

$FoM_S = SNDR + 10\log_{10}(BW/P)$

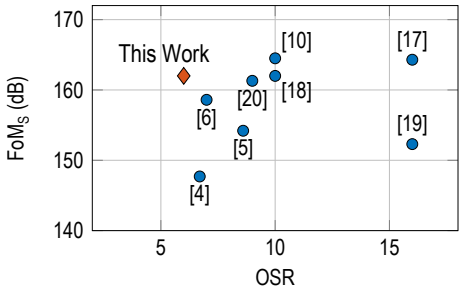

Fig. 8: FoM_S vs. OSR of state of the art wideband low-pass CT DSMs with a bandwidth >150 MHz and effective resolution $\geq$10-bit.

V. CONCLUSION

A 2–0 MASH CT DSM is realized with an ultra-low OSR of 6, achieving 200 MHz bandwidth with only 2.4 GHz sampling frequency. To maintain a high resolution, a 6-bit 4xTI SAR is employed as second stage, while a 15-level Flash operates as fast QTZ in the DSM. The Flash preloads the TI SAR, efficiently extracting the QTZ error and realizing an ISG. Operating from 0.9 V supply, the DSM achieves $FoM_S = 162$ dB, SFDR = 78 dB and DR = 66 dB. Its implementation allows excellent robustness against process, voltage and temperature variation, while the low OSR potentially allows future implementations to further maximize the achievable bandwidth of CT DSMs.

ACKNOWLEDGMENT

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