A Reconfigurable 16/20 GS/s 7/6 ENOB Voltage/Time Hybrid ADC With Embedded Time Amplifier and VTC Time Borrowing Achieving 150.6/148.1 dB Schreier FoM

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***Abstract*— This paper presents a direct radio-frequency (RF) sampling, dual-mode, 16/20-GS/s, 8× time-interleaved (TI) analog-to-digital converter (ADC) that employs one-bit voltage quantization, a time borrowing voltage-to-time converter (VTC), and a pipelined successive-approximation-register (SAR) time-to-digital converter (TDC) embedded with time amplifiers (TAs). The proposed architecture enables efficient reconfigurable dual-mode operation while maintaining low power consumption. The ADC prototype is fabricated in a 12-nm CMOS process and occupies an active area of 0.096 mm². The prototype achieves Schreier figures of merit (FoMs) of 150.6 dB and 148.1 dB at the Nyquist frequency in the 16-GS/s and 20-GS/s modes, respectively, improving ADC FoMs when reconfigured to a lower sampling rate by 2.5 dB.**

Keywords*— *Analog-to-digital converter (ADC), Voltage-to-time converter (VTC), Time-to-digital converter (TDC), time-domain ADC, Dual Mode ADC.

I. Introduction

There has been a growing demand for high-speed, reconfigurable ADCs that provide flexibility and performance adaptability for software-defined radio (SDR) applications, while maintaining high efficiency and cost-effectiveness [1-4]. Time-domain (TD) ADCs have emerged as a promising solution due to their high sampling rates, technology scaling, and area efficiency [1-4]. In [1], a reconfigurable 16-way TI TD-ADC employing a ring-oscillator-based TDC is presented; however, it suffers from limited per-channel speed and high power consumption. In [3], a reconfigurable flash/SAR TDC utilizing a highly linear voltage-controlled oscillator (VCO) is proposed, combining a SAR TDC for high resolution with a flash TDC for high sampling rates, but this approach becomes power-inefficient at high speeds. Alternatively, [4] introduces reconfigurable vernier TDCs that significantly increase sensitivity to mismatches. In addition, the achievable signal-to-noise ratio (SNR) of TD ADCs remains fundamentally limited by the linearity of the VTC and the jitter of the TDC [5-10]. This work employs several techniques to overcome these limitations and meet the required jitter specifications with minimal power overhead, while improving efficiency as the ADC is reconfigured to a lower sampling frequency. First, in 16GS/s mode, a voltage quantization is performed prior to TD quantization, thereby increasing ADC resolution and improving the achievable FoM. Second, by incorporating TAs into a pipelined SAR TDC, the input-referred jitter is reduced by the TA gain, offering better jitter/power trade-off. In addition, the proposed VTC time borrowing technique extends the TDC input dynamic range (T_{FS}) by reallocating time from the sampling phase to the VTC operation. Finally, a dynamic switch-off (DSO) TDC delay cell is proposed to disable unused output paths dynamically and further reduce power consumption.

II. ADC Architecture & Circuit Details

A. ADC architecture

The proposed dual-mode architecture, shown in Fig. 1, comprises 8 TI channels operating in two modes. In the 16 GS/s mode, voltage quantization precedes time-domain quantization to improve SNR and more efficiently utilize the timing budget. The input is sampled on the bottom plates S_P and S_N. In the 16 GS/s mode, a comparator driven by CLK_{CMP} compares the voltages of both S_P and S_N to determine which is higher, after which the top plate of the

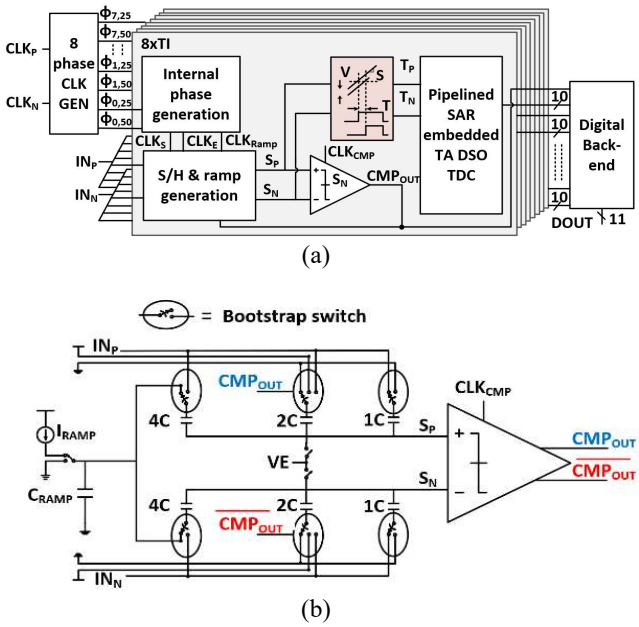

Fig. 1. (a) Proposed Dual Mode ADC architecture, (b) ADC S/H & ramp generation.

selected 2C capacitor is switched from *V*DD to *V*SS, generating a one-bit residue. A differential ramp is then generated on the residue through the 4C capacitor and applied to an edge detector, producing pulses T_P and T_N whose time difference is quantized by the TDC. In the 20 GS/s mode, the comparator is disabled and the voltage quantization is bypassed. Ramp generation and time-domain quantization follow sampling directly to achieve higher sampling speed.

B. Pipelined SAR TDC embedded Time Amplifier

The pipelined SAR TDC is distinguished by its efficiency and scalability, leveraging the advantages of both SAR and pipelined architectures [5-6]. However, to increase the TDC resolution given a fixed TDC input full scale (T_{FS}), it is required to reduce the Least Significant Bit (TDC_{LSB}). TDC SNR is limited by both quantization noise and accumulated TDC jitter, and can be expressed as:

$$SNR = \frac{\frac{T_{FS}^{\,2}}{8}}{\frac{TDC_{LSB}^{\,2}}{12} + \sigma_{OUT}^{\,2}} \tag{1}$$

Where σ_{out} is the accumulated Root-Mean-Square (RMS) jitter at the TDC output and can be written relative to the TDC_{LSB} as:

$$\sigma_{out} = \alpha * TDC_{LSB} \tag{2}$$

Where α denotes the output jitter normalized to the LSB, for a 3 dB SNR degradation, α can be approximated to 0.3. Combining (1) and (2) shows that reducing the TDC_{LSB} to improve resolution requires stringent jitter performance, thereby increasing power consumption. This tight tradeoff between resolution and power efficiency mandates innovation to resolve these challenges. The proposed 10-stage pipelined SAR TDC, shown in Fig. 2, incorporates TA, which significantly reduces the input-referred jitter of the preceding stages. The TDC consists of a three-bit pipeline SAR TDC, followed by a TA, a two-bit pipeline SAR TDC, followed by the second TA, then the last four-bit pipeline SAR TDC, and finally the comparator. The TDC includes 2 bits of redundancy, resulting in an effective resolution of 8 bits. The TA gain is implemented using

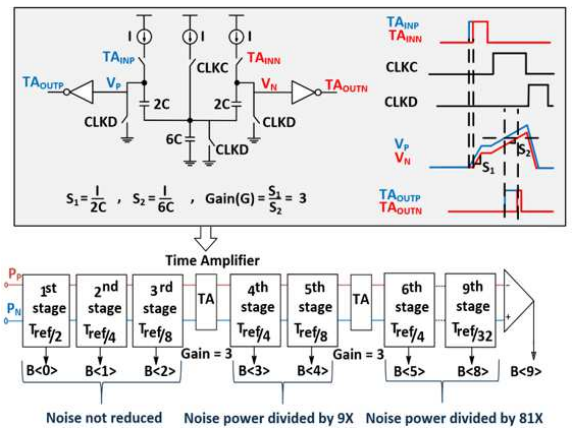

Fig. 2. Proposed Pipelined SAR TDC architecture.

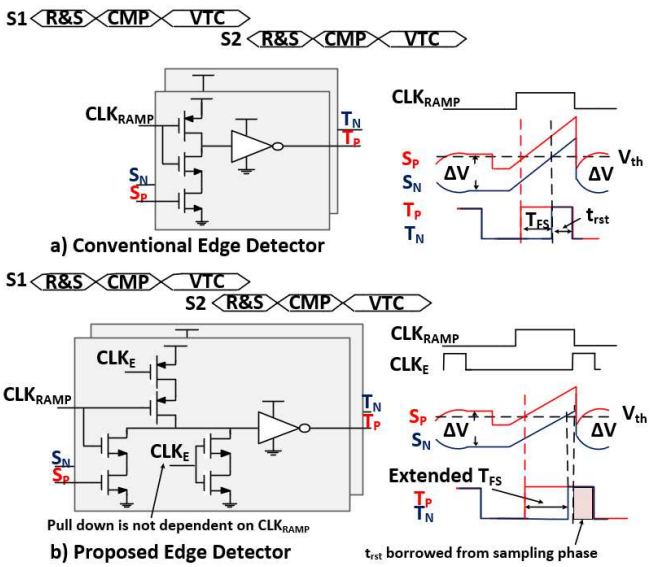

Fig. 3. VTC time borrowing technique.

capacitor ratios for good matching, exploiting different charging rates under a common current source, and is set to 3 to avoid residue saturation. Due to its 5-bit linearity limitation, the first TA is inserted after the first three stages. Moreover, the two TAs are designed to share a common interface, with both having unified preceding and later stages. For a given output jitter requirement, the TDC power consumption can be optimized by appropriately sizing the delay stages after the TA. Overall, the proposed architecture achieves a 37% reduction in total ADC power consumption compared to the conventional approach in [5-6].

C. Time borrowing VTC

VTC plays a crucial role in determining the overall performance of TD ADC. VTC operating frequency is limited by several factors, including the ADC sampling time, the extra time required before the rising edge of the earliest time pulse, TDC T_{FS}, and the time required to fully reset the VTC edge detector output (t_{rst}) [9]. In Fig.3 (a), a conventional edge detector uses the ramping clock CLK_{RAMP} as the reset signal of the VTC edge detector output. This reduces the achievable T_{FS}, thereby reducing the achievable signal power and limiting the TDC_{LSB}. Our proposed edge

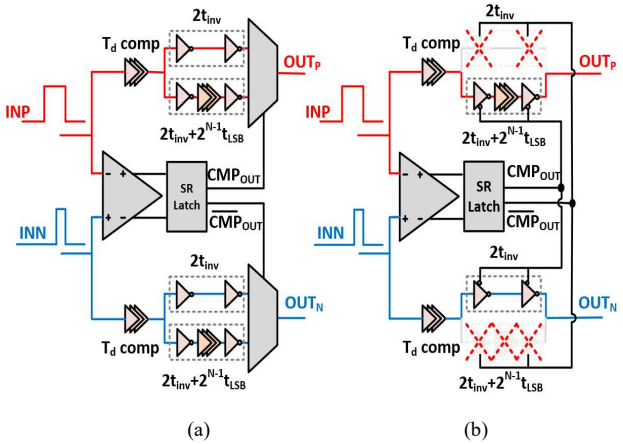

Fig. 4. (a) Conventional SAR TDC stage, (b) proposed SAR TDC stage.

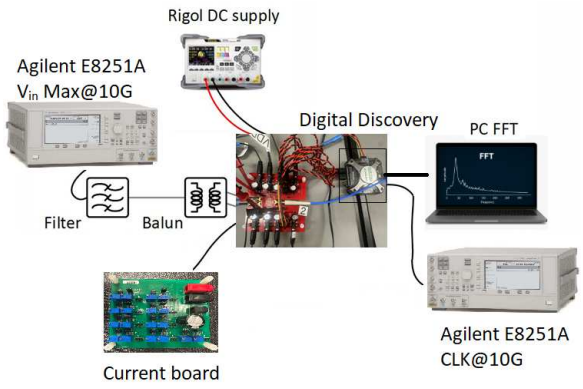

Fig. 5. Measurement setup.

detector, shown in Fig. 3 (b), utilizes the bottom-plate sampling switch clock (CLK_E) to borrow the t_{rst} time from the sampling phase, which is approximately 30 psec, thereby extending T_{FS}, relaxing the TDC jitter requirement, and reducing TDC power consumption. As a result, the proposed architecture increases T_{FS} by 37.5%, from 80 ps to 110 ps, thereby reducing total ADC power consumption by 34%.

D. Dynamic Switch-off (DSO) TDC delay cell

Fig. 4 illustrates the conventional reference time subtraction cell [6], in which the early input rising edge should pass through $2t_{inv} + 2^{N-1}\, t_{LSB}$ delay, and the late input rising edge should pass through $2t_{inv}$ delay only. However, both input pulses propagate through all delay elements and an output multiplexer (MUX). In the proposed delay cell, the output MUX is eliminated, and the inverters in both signal paths are replaced with tri-state inverters. The comparator output dynamically controls the tri-state inverters, disabling unnecessary delay paths. This approach reduces power consumption by 30% in the Most Significant Bit (MSB) stage, resulting in a 15% reduction in total TDC power consumption.

III. MEASUREMENT RESULTS

The measurement setup is shown in Fig. 5. The ADC was fabricated in a 12-nm CMOS process with an active area of 0.096 mm² (Fig. 10). The measured output spectrum (Fig. 6) is decimated by 1025. At low input frequencies, the ADC achieves 43.0/40.1 dB SNDR and 56.4/49.2 dB SFDR, while at the Nyquist frequency it achieves 41.8/39.3 dB SNDR and 55.8/48.5 dB SFDR in the 16/20-GS/s modes, respectively. Interleaving clock skew is calibrated using an on-chip delay line, and inter-channel gain and offset mismatches are corrected off-chip. Fig. 7 shows SNDR and SFDR versus input frequency, at both sampling modes, at 16GS/s sampling speed, ADC achieves >41.8 dB SNDR and >54 dB SFDR across input frequencies from 180MHz to 7.97GHz, at 20GS/s sampling speed, ADC achieves >39 dB SNDR and >48 dB SFDR across input frequencies from 180MHz to 9.5GHz. The measured linearity (Fig. 8) shows DNL within +0.95/−0.9 LSB and INL within +1.9/−2.3 LSB at 20GS/s mode. Fig. 10 presents the power breakdown, with the TDC accounting for 59% of the total power. As shown in Table I, compared to state-of-the-art high-speed ADCs in literature with SNDR>36 dB, the proposed dual-mode ADC achieves the highest FoM_S at 20 GS/s. At 16 GS/s, it attains a higher FoM_S than the 20 GS/s mode, with a 0.65 dB/GHz increase in FoM_S, demonstrating improved efficiency as the sampling rate decreases compared to [7] (Fig. 9). While [1] exhibits a similar efficiency slope, it suffers from higher power consumption and therefore lower overall efficiency.

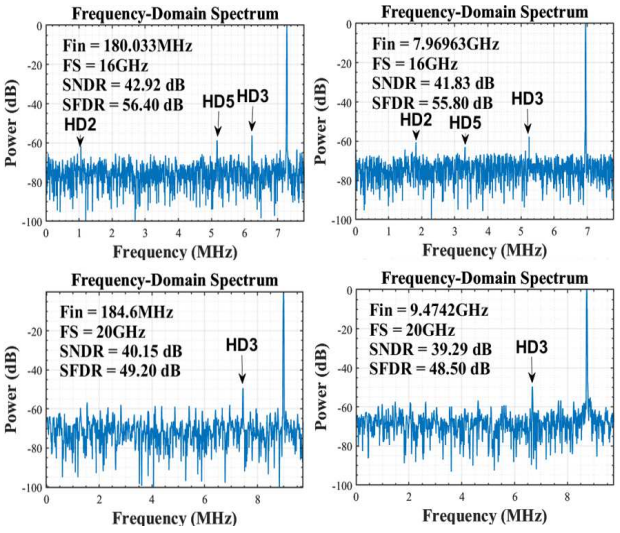

Fig. 6. Measured output spectrum at 16GS/s&20GS/s (a)at an input frequency of 180MHz, (b) Nyquist frequency.

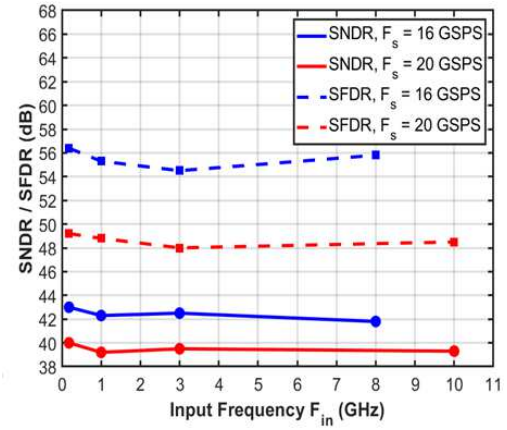

Fig. 7. Measured SNDR/SFDR at 16GS/s and 20GS/s across input frequencies.

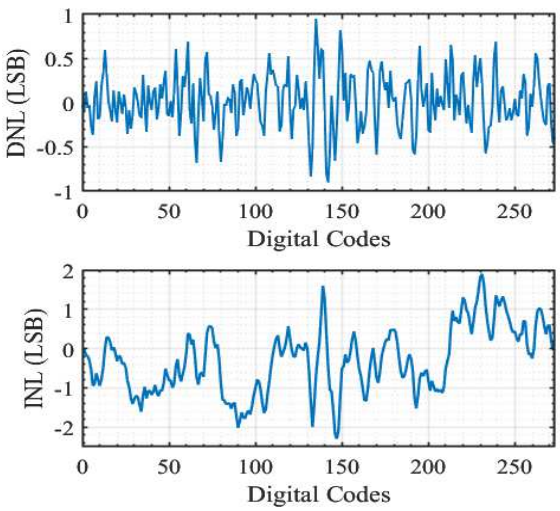

Fig. 8. Measured DNL &INL at Nyquist Frequency at 20GS/s.

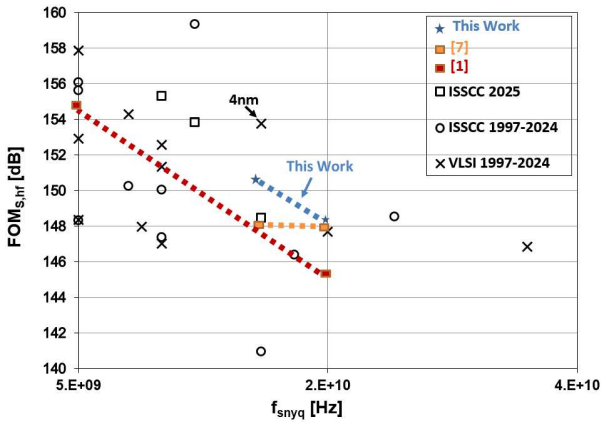

Fig. 9. Scherier FOM comparison with state-of-the-art ADCs.

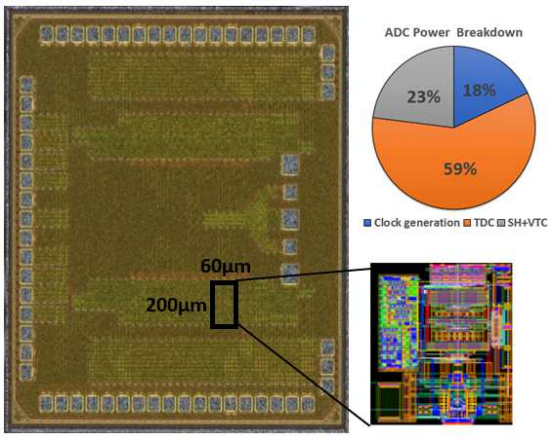

Fig. 10. The microphotograph with one-channel ADC layout.

IV. Conclusion

The proposed Dual Mode 16/20 GS/s ADC achieves enhanced efficiency at reduced sampling rate by employing 1-bit voltage quantization before time quantization. The jitter requirement for the TDC is relaxed by leveraging the VTC time-borrowing technique to maximize the achievable signal swing. Furthermore, an embedded TA-pipelined SAR TDC is implemented, thereby reducing the jitter requirements of subsequent stages. Finally, a DSO SAR TDC cell is incorporated, which minimizes the TDC's power consumption for a given target jitter. The proposed ADC achieves a Schreier FOM of 150.6 dB/148.1 dB at 16 GS/s and 20 GS/s, respectively.

TABLE I. Performance Summary and Comparison Table

	This Work		**M.Zhang VLSI 2021[7]**		**J.Wei Microelectonic Journal 2023[1]**	
Architecture	TI TD ADC		TI TD ADC		TI TDC ADC	
Technology	12nm		65nm		40nm	
F_S [GS/s]	20	16	20	16	20	5
TI-channels	8		8		16	
Resolution [b]	8	9	8		8	10
Supply [V]	0.9/0.8*		1		1.2	
SFDR@Nyq [dB]	48.5	55.8	52.5		45.7	56.5
Power [mW]	131	105	130	76	139.3	83.6
SNDR@Nyq [dB]	39.3	41.8	39	38	36.8	50.8
Area [mm^2]	0.096		0.223		NA	
FOM_S [dB]	**148.1**	**150.6**	147.8	148.2	145.4	155.6
FOM_W [fJ/c-s]	87	65	91	72.5	123.4	59
FOM_S Slope [dB/GHz]	**0.65**		0		0.67	

*S/H supply/Time Domain supply

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