MCFF: A 0.22fJ/Cycle 23-Transistor D Flip-Flop Featuring the Minimum Clock-load and Complete Redundant Transition Elimination in 28nm CMOS

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***Abstract*—An ultra-low power flip-flop named the Minimum Clock-load Flip-Flop (MCFF) is presented, which eliminates redundant transitions completely as well as maintains static and contention-free operations across a wide supply voltage range. In particular, an effective transition sensing (ETS) scheme is presented to eliminate clock- and data-related redundant transitions. Moreover, clock merge and replacement (CMR) strategies are proposed to minimize the clock load to two transistors, where one is used for the pull-up network, and the other is for the pull-down network. Finally, MCFF and prior flip-flops are fabricated in a 28nm CMOS process. Compared with prior works under the typical 10% data activity ratio, MCFF achieves a power reduction from 17.7% to 54.0% at 0.9V, and from 25.8% to 39.4% at 0.3V on average, respectively. As a result, MCFF is promising for Internet of Things (IoTs), wearable devices, and edge large language models (LLMs).**

***Keywords*—Effective hybrid load, clock load, flip-flop (FF), redundant transition, low power**

I. Introduction

As a fundamental sequential element in digital integrated circuits (ICs), D flip-flop (FF) accounts for more than 20% of dynamic power, or 50% random logic (both combinational and sequential logic) power consumption in a typical system-on-a-chip (SoC) [1-2]. Furthermore, the supply voltage (VDD) of many digital integrated circuits has been extended from the super-threshold to near-threshold regime to meet diverse applications. As a result, low-power D flip-flops that can work reliably at both nominal VDD and ultra-low VDD have gained a large amount of attention.

To avoid excessive dynamic power consumption and contention issues due to the large clock load and phase overlap between clock (CK) and antiphase clock (CKB) signal in a two-phase-clocking based FFs, single-phase-clocking FFs were presented in [3, 6], featuring reliable operations across a wide supply voltage range. However, these structures suffer from redundant clock-related transitions on internal clock node (functioning as CKB) or large clock load. As a result, [4-5] presented dedicated internal clock generator (ICG) structures to eliminate clock-related redundant transitions when input data keeps unchanged (Fig.1 bottom left).

Moreover, the power consumption of clock load transistors (4 to 6 in above structures) typically occupies more than 50% total power of FF, given the 100% activity ratio of clock signal and the 5%-15% activity ratio of data signal [5]. As a result, [7] presented an three clock-load based FF structure (CRFF) for less clock-related power, by adopting logic replacement strategy and conditional charge scheme. Nevertheless, the clock load transistors in above structures still consume over 50% of the total power consumption [7].

At the same time, with the reducing of clock-related power, the impact of total power due to data-related redundant transitions on internal nodes (Fig.1 bottom right) should not be ignored anymore.

To address above issues, we presents a 23-transistor ultra-low power D flip-flop named the Minimum Clock-load Flip-Flop (MCFF) in this paper, which achieves the minimum clock load of two transistors as well as eliminates both data- and clock-related redundant transitions completely. We prototype the MCFF and prior works in a 28nm CMOS process. Compared with prior works under the typical 10% data activity ratio, the measured power of MCFF is reduced

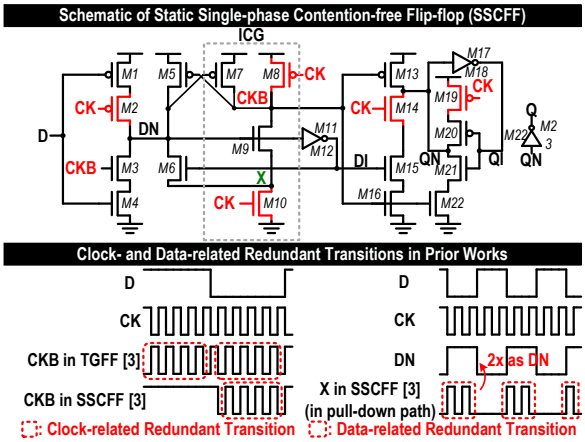

Fig. 1. Schematic of SSCFF (all clock-related signals are highlighted in red, and data node with redundant transitions are highlighted in green). The clock-related and data-related redundant transitions in TGFF and SSCFF are shown in the bottom.

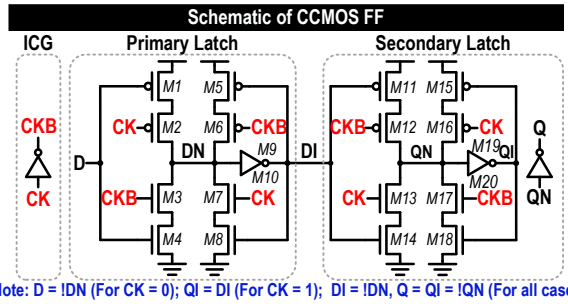

Fig. 2. The schematic of CCMOS (all clock-related signals are highlighted in red).

by17.7%-54.0% at 0.9V, 25.8%-39.4% at 0.3V, respectively.

The content of this paper is organized as follows. The design methodology and operations of the presented MCFF are described in Section II. Measurement results and comparison with prior works are shown in section III. Finally, Section IV provides the conclusion.

II. The Presented MCFF Structure

We select CCMOS [8] as a reference design which is shown in Fig.2, for the presented MCFF due to its good timing, power, and area characteristics. However, it contains a conventional inverter-based ICG and ten clock load transistors with a large amount of redundant clock-related transitions and additional dynamic power.

To eliminate clock- and data-related redundant transitions in CCMOS, we firstly present an effective transition sensing (ETS) scheme as shown in Fig.3, where the CKB will only be triggered when input data (D) transitions. ETS for Primary Latch and ETS for Secondary Latch. Thus, we develop a temporary ICG-V1 and final redundancy-free ICG structure, respectively. In Primary Latch, the waveform and truth table of the required CKB are shown in Fig.3 top. Thus, we can just trigger CKB for necessary data capture (CK=0, DN=0) and data retention (CK=1, DN=1) operations by employing a Nand gate as the truth table. And consequently, the intermediate ICG-V1 structure removes redundant clock-related transitions on CKB node when D is 1. Besides, we swap the transistor pair M24 and M26 functionally so that the CK signal can cut off the charging path from CKB to X, thereby removing the data-related redundant transitions (shown in Fig.1 bottom right) on node X.

In the Secondary Latch, we eliminates the redundant transitions on node CKB when D=Q=0 by holding CKB in all unnecessary cases with an extra node A1 to control the pull-up path of CKB, so that the CKB is triggered only for data retention when CK is 0 and D is not equal to Q (D = QN = 0). Consequently, the final redundancy-free ICG structure is presented as shown Fig.3 bottom right, which eliminate clock- and data-related redundant transitions completely.

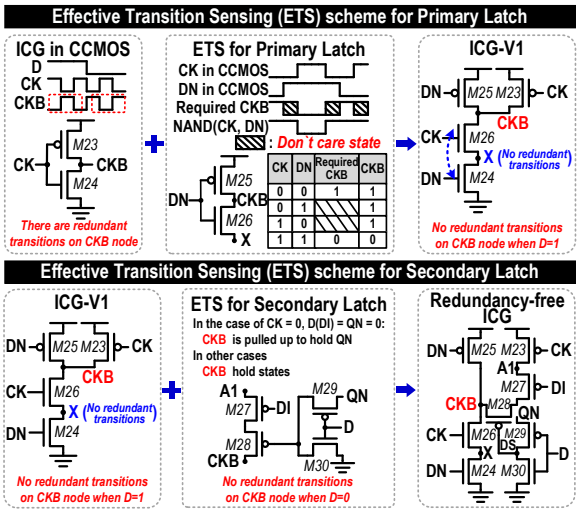

Fig. 3. Effective transition sensing (ETS) scheme for clock- and data-related redundant transitions elimination.

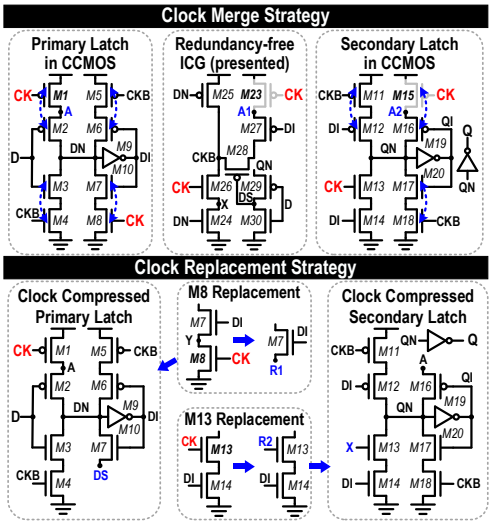

Fig. 4. The clock merge (M1, M15, and M23) (a) and replacement (M8 and M13) (b) strategies.

To reduce the clock load in CCMOS, we adopt clock merge and replacement (CMR) strategies across the redundancy-free ICG, primary latch and secondary latch as shown in Fig. 4. We first swap the position of transistor pairs on the same charging path in primary latch and secondary latch of CCMOS (M1 and M2, M3 and M4, M5 and M6, M7 and M8, M11 and M12, M15 and M16, and M17 and M18) (highlighted in blue in Fig.4 top) without changing the functionality of the charging path.

After swapping, we first adopt clock merge strategy across M1, M15 and M23. Since there are no charge sharing between node A, A1 and A2, these three nodes can be merged into A (highlighted in blue in the primary latch of CCMOS), and thereby M1, M15, and M23 can be merged into one transistor (named new M1 in the primary latch of CCMOS) without occurring data contention (Fig.4 top).

After that, we further apply clock replacement strategy on M8 and M13. we analyze the required logic value of the node Y between M7 and M8, and CK in M13 (named as node R1 and R2). We notice that the functionality of node DS and X is equivalent to the node R1 (source of M7) and R2 (gate of M13). Thus, M8 can be replaced by node DS, and M13 can be controlled by X instead of CK (Fig.4 bottom).

Consequently, the total clock load of redundancy-free ICG, clock compressed primary latch and secondary latch is reduced to the theoretically minimum of two transistors, where M1 is used for pull-up network, and M26 is for pull-down network.

Based on the above scheme and strategies, we further merge the equivalent transistors to compress transistor count. The final structure of presented MCFF with 23 transistors is shown in Fig.5. The transistors are sized consistently with standard FFs in the 28nm standard cell library, including both clock and data transistors. The detailed operations for data capture (Case 1 to Case 2 and from Case 5 to Case 6) and retention (other cases) are shown in Fig. 6, which means the MCFF can supports static and contention-free operation with clock- and data-related redundant transition elimination.

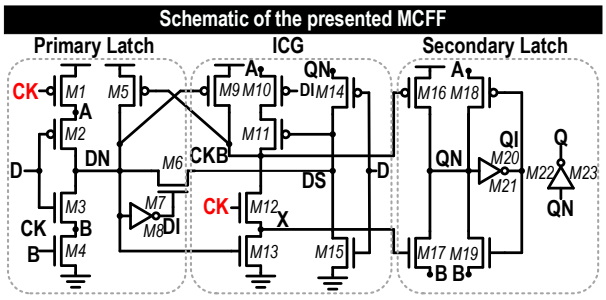

Fig. 5. The schematic of the presented MCFF.

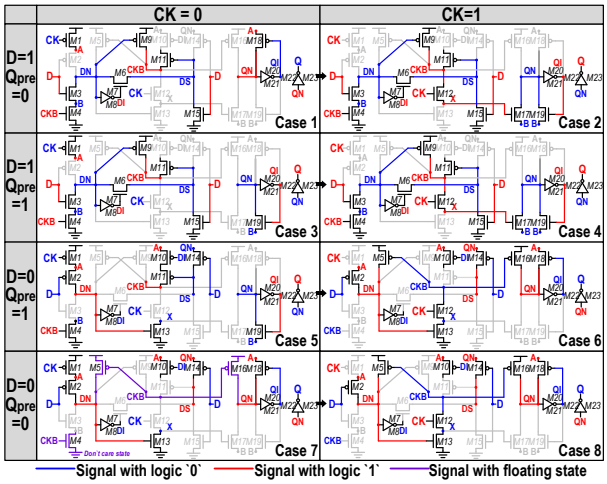

Fig. 6. The operations of MCFF including data capture operations (from Case 1 to Case 2 and from Case 5 to Case 6) and data retention operations (from Case 3 to Case 4 and from Case 7 to Case 8).

Fig. 7 shows 10k Monte Carlo simulations (global and local variations) for each FF structure with a supply voltage range from 0.20V to 1V, and 50FO4 clock period. The presented MCFF can work reliably from 0.3 to 1V, which is lower than or comparable to prior works.

III. Chip Measurement Results and Comparison

The presented MCFF and prior works [3-7] are prototyped in a 28nm CMOS process for functionality validation and performance evaluation. Fig. 8 shows their die photograph. The on-chip testing circuits, including

	TGFF	SSCFF	18TSPC	SCDFF	CSFF	REFF	CRFF	MCFF
1.00V	P	P	P	P	P	P	P	P
0.95V	P	P	P	P	P	P	P	P
0.90V	P	P	P	P	P	P	P	P
...	P	P	P	P	P	P	P	P
0.60V	P	P	P	P	P	P	P	P
0.55V	P (100%)	P (100%)	F (99.97%)	P (100%)	P (100%)	P (100%)	P (100%)	P (100%)
0.50V	P (100%)	P (100%)	F (99.70%)	P (100%)	P (100%)	P (100%)	P (100%)	P (100%)
0.45V	P (100%)	P (100%)	F (97.50%)	P (100%)	P (100%)	P (100%)	P (100%)	P (100%)
0.40V	P (100%)	P (100%)	F (91.83%)	P (100%)	P (100%)	P (100%)	P (100%)	P (100%)
0.35V	P (100%)	P (100%)	F (83.80%)	P (100%)	P (100%)	P (100%)	P (100%)	P (100%)
0.30V	P (100%)	P (100%)	F (74.35%)	P (100%)	F (99.98%)	P (100%)	F (99.99%)	P (100%)
0.25V	F (99.97%)	F (99.99%)	F (63.30%)	F (99.81%)	F (92.90%)	F (99.99%)	F (98.84%)	F (99.67%)
0.20V	F (96.17%)	F (97.81%)	F (46.31%)	F (82.91%)	F (83.37%)	F (97.68%)	F (95.33%)	F (96.80%)

Fig. 7. Monte-Carlo simulations with 10k, global and local variations.

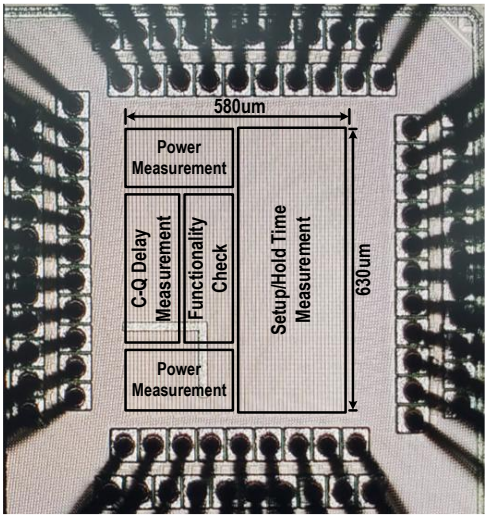

Fig. 8. Die photo of the prototype chip in a 28nm process.

functionality check circuits, C-Q delay measurement circuits, power measurement circuits and setup/hold time measurement circuits, are the same as those in [5, 7].

Fig. 9 summarizes the power measurement results of ten test dies. Compared with prior works under the typical 10% data activity ratio, MCFF achieves 17.7%-54.0% (25.8%-39.4%) power reduction at 0.9V (0.3V) on average (Fig. 9(a) and (b)). Sweeping the clock period from 30FO4 to 70FO4 and supply voltage from 0.3V to 0.9V, MCFF consumes 15.4%-54.0% (24.6%-43.1%) less power at 0.9V (0.3V) (Fig. 9(d) and (e)), and 15.8%-54.0% less power (Fig. 9(c)), respectively. In summary, the presented MCFF achieves the lowest power consumption across the data activity ratio range of 0-50%, supply voltage range of 0.3V-0.9V, and clock period range of 30FO4-70FO4. Considering the energy consumption per cycle, MCFF achieves the minimum energy of 0.22fJ/cycle at 0.35V under the clock period of 50FO4, which is 22.3% less than that of [7] (Fig.9(f)).

The minimum voltage and timing (C-Q delay, setup/hold time) results of ten test dies are shown in Fig. 10. Fig. 10(a) shows that MCFF (ten dies) can work correctly at the minimum supply voltage of 0.21V. Compared to TGFF [3],

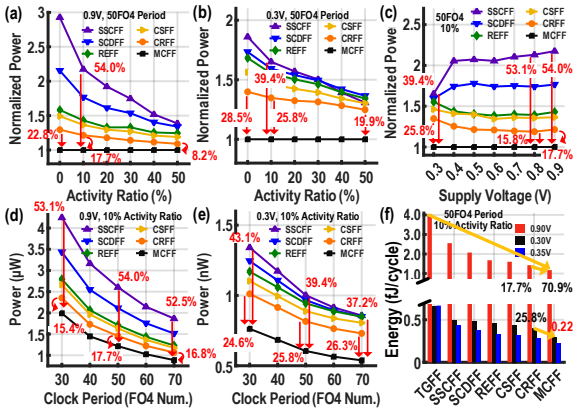

Fig. 9. The measured average power consumption of ten dies under different activity ratios at (a) 0.9V and (b) 0.3V, and different clock periods at (d) 0.9V and (e) 0.3V. The measured average power under different supply voltages and the energy are shown in (c) and (f), respectively.

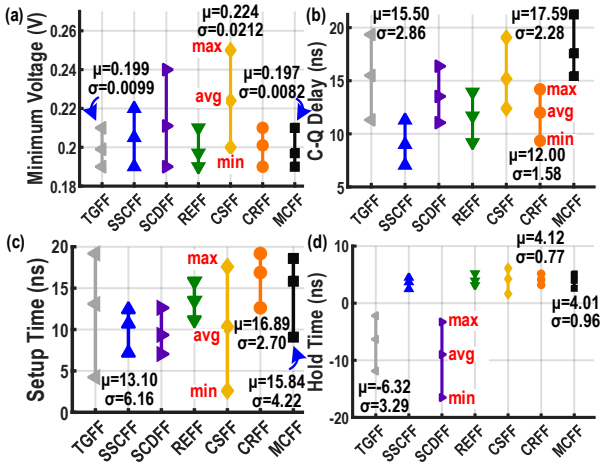

Fig. 10. The minimum voltage and timing measurement results of ten dies. (a) The minimum functional voltage. (b) C-Q delay at 0.3V. (c) Setup time at 0.3V. (d) Hold time at 0.3 V.

it achieves a 17.2% reduction in the standard deviation of the minimum supply voltage, indicating a narrower voltage distribution under process variations (Fig.10(a)).

Fig. 10(b)-(d) show the timing measurement results (C-Q delay, setup time, and hold time) of ten test dies at 0.3V. Compared with TGFF, MCFF achieves more centralized timing distributions under process variations, which has 20.3%, 31.5% and 70.8% smaller standard deviation for C-Q delay, setup time and hold time, respectively.

TABLE I shows the comparison table. MCFF achieves the minimum clock load of two transistors and complete elimination of redundant transitions, while supports static and contention-free operations across a supply voltage range from 0.21 to 0.9V. Compared with TGFF with the 0% and 10% data activity ratio, MCFF achieves up to 79.6% and 70.9% power reduction at 0.9V, respectively. Moreover, it achieves up to 12.1% area benefit.

TABLE I. THE COMPARISON TABLE OF PRESENTED MCFF WITH CONVENTIONAL TGFF AND STATE-OF-THE-ART LOW POWER FLIP-FLOPS.

		TGFF	SSCFF[3]	SCDFF[6]	CSFF[4]	REFF[5]	CRFF[7]	MCFF
		Std. Cell	ISSCC 2014	JSSC 2023	JSSC 2018	JSSC 2021	JSSC 2024	This Work
Transistor Count		24	24	26	24	25	23	23
Clock Load Transistor Count		12	5	6	5	4	3	2
Measured Min. VDD		0.21	0.22	0.24	0.25	0.21	0.21	0.21
Normalized Layout Size		1	1.07	1.13	1.13	1.2	1.07	1.07
Data @0.9V 50FO4	Power @ 0 activity ratio	3.86uW	2.30uW	1.69uW	1.17uW	1.24uW	1.02uW	0.79uW
	Power @ 10% activity ratio	4.12uW	2.60uW	2.11uW	1.63uW	1.71uW	1.45uW	1.20uW
	Measured C-Q Delay	48.2ps	42.8ps	40.3ps	45.0ps	44.7ps	39.3ps	65.0ps
	Measured Setup Time	5.7ps	30.8ps	30.2ps	11.4ps	16.6ps	25.6ps	20.5ps
	Measured Hold Time	-9.0ps	9.5ps	-24ps	-14.4ps	8.3ps	9.7ps	7.2ps
Data @0.3V 50FO4	Power @ 0 activity ratio	1.30nW	0.95nW	0.88nW	0.80nW	0.86nW	0.71nW	0.51nW
	Power @ 10% activity ratio	1.36nW	1.02nW	0.98nW	0.90nW	0.96nW	0.83nW	0.62nW
	Measured C-Q Delay	15.5ns	9.0ns	13.5ns	15.2ns	11.7ns	12.0ns	17.6ns
	Measured Setup Time	13.1ns	10.7ns	9.3ns	10.3ns	13.5ns	16.9ns	15.8ns
	Measured Hold Time	-6.3ns	3.7ns	-9.0ns	4.2ns	3.9ns	4.1ns	4.0ns

IV. CONCLUSION

This work presents a novel low-power 23-transistor MCFF structure, which completely eliminates redundant transitions by adopting effective transition sensing (ETS) scheme. It achieves the minimum clock load of two transistors through clock merge and replacement (CMR) strategies. Compared with prior works under the typical 10% data activity ratio, measurements results show that MCFF achieves power reduction ranging from 17.7% to 54.0% at 0.9V, and from 25.8% to 39.4% at 0.3V on average, respectively. Consequently, MCFF has a great potential for low power and ultra-low power scenarios such as Internet of Things (IoTs) and wearable devices.

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