A Robust 400-MS/s Pipeline-SAR with a Unified CMFB Tolerating ±25°/±3-dB Input Imbalance

Qide Cheng, Jiangfan Wen, Shenglong Zhuo, Miao Meng, Bingbing Yao, Lei Qiu
Tongji University, Shanghai, China
Email: yaobingbing@tongji.edu.cn, qiulei@tongji.edu.cn

***Abstract*—This paper focuses on the robustness of pipeline-SAR ADCs with inverter-based residue amplifiers (RAs). The key is a novel unified CMFB to maintain the RA performance, regardless of PVT drifts, inherent CM modulations caused by ADC quantization, and signal-dependent CM variations induced by imbalanced input. A novel inverter-based RA is also proposed to accelerate the RA amplification. Running at 400 MS/s with a 1.6-Vpp Nyquist input, the prototype ADC achieves 65.7-dB/86.8-dB SNDR/SFDR, yielding an excellent FoM_W of 5.9 fJ/c.-s. It demonstrates robust performance to PVT drifts, 0.3 V-0.8 V input CM range, ±25° phase or ±3-dB amplitude imbalance for a 1-Vpp input, and any other inevitable DC CM modulations.**

***Index Terms*—Analog-to-digital converter (ADC), inverter-based RA, unified CMFB, input imbalance, robustness**

I. Introduction

The performance of the inverter-based RA is firstly sensitive to PVT. However, another two issues (Fig. 1(a)), which also account for the sensitivity, are not seriously considered yet: 1) Input CM modulations caused by ADC quantization, including DC parameters, such as input CM, sampling CM and reference voltage, and high-order non-idealities, such as summing-node parasitics, sampling-switch charge injection and RA switching, etc.; 2) Signal-dependent (SD) RA offset induced by imbalanced input, originating from the practical baluns. To enhance the robustness, existing works mainly rely on embedded local and global CMFB [1]–[3]. Though simple and attractive, their disadvantages are usually overlooked (Fig. 1(b)): 1) Tradeoff with amplifier parameters, such as gain [1], bandwidth [2] or voltage headroom [1]–[3], burdening the signal path optimization; 2) Narrow tolerable range for RA input CM, leading to weak ability to tackle the inevitable CM modulations or even extreme PVT variations; 3) Absence of SD CM regulation (CMREG), leaving the SD offset behind; 4) Stringent CM constraints on input buffer, limiting its architectural flexibility; 5) Demanding test environment, necessitating manual fine-tuning of the test parameters.

II. DC CMFB

Fig. 2 details the proposed DC CMFB, which firstly differs in taking advantages of the free sampling CM. The target of the CMFB is to stabilize the RA output CM around its trip point during amplification. Specifically, the detection is executed by comparing RA output CM with the target V_{CM_DC} using

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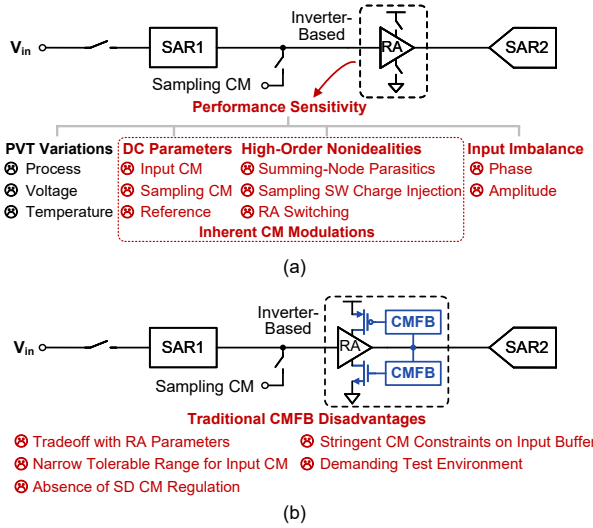


Fig. 1. (a) Performance sensitivity of the inverter-based RA in traditional Pipeline-SAR ADCs. (b) Disadvantages of the traditional CMFB scheme for inverter-based RA.

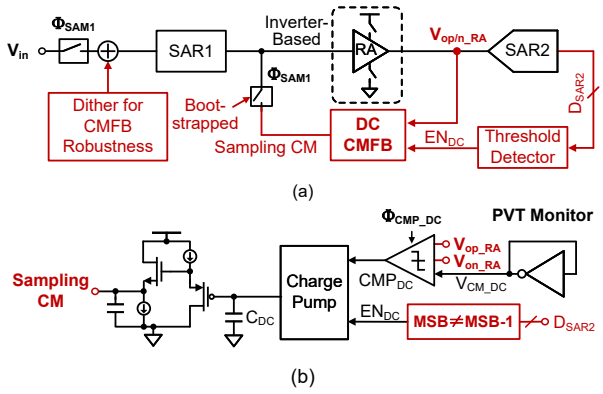


Fig. 2. (a) Block diagram and (b) detailed implementation of the proposed DC CMFB exploiting sampling CM.

CMP_{DC}, and the feedback loop is closed by adjusting the sampling CM through a charge pump (CP) and an integration capacitor C_{DC}, where V_{CM_DC} is generated by a PVT monitor. Critically, to suppress the SD offset of CMP_{DC} to a negligible level of ±2.4 mV in this work (Fig. 3), a threshold detector is proposed to categorize the input. As shown in Fig. 2(b), it

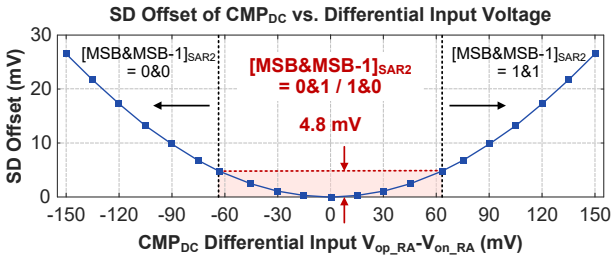


Fig. 3. Principle of the threshold detector.

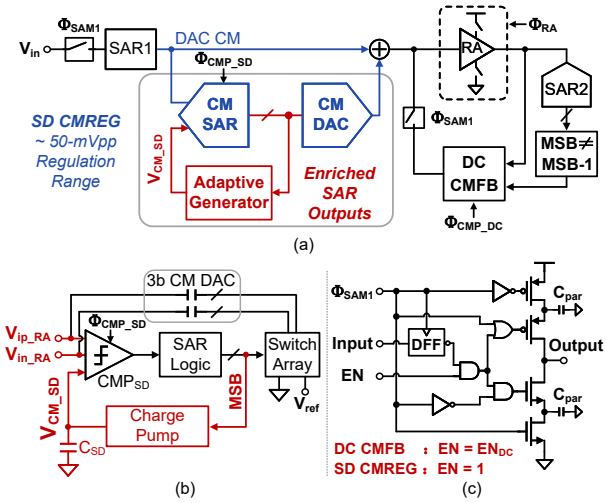


Fig. 4. (a) Block diagram of the proposed unified CMFB. (b) Detailed implementation of the SD CMREG with an adaptive V_{CM_SD} generator. (c) Detailed implementation of the employed charge pump.

is realized by judging whether its MSB and MSB-1 quantized by SAR2 are equal or not: if equal, the input is large and EN_{DC}=0; otherwise, it is small and EN_{DC}=1. The EN_{DC} is further utilized to enable or disable the sampling CM update. Meanwhile, to ensure the CMFB convergence regardless of input, a 3-bit dither is injected after sampling. Different from the traditional CMFB, the proposed structure outstands as follows: 1) No tradeoff with amplifier parameters, greatly relieving the signal path design; 2) The ability to absorb any DC or slow-changing CM modulation into sampling CM, fully resolving both the PVT drifts and the inherent input CM modulations; 3) Potential capability to achieve an ADC input CM range as wide as rail-to-rail, completely releasing the input buffer from CM constraints.

III. Unified CMFB

Fig. 4(a) shows the proposed unified CMFB. Besides the merits of the DC CMFB, it can further suppress the SD RA offset through an auxiliary SD CMREG to regulate the varying DAC CM to a target V_{CM_SD} during SAR1 conversion. However, the basic challenge is to coordinate the SD CMREG with the DC CMFB. Critically, the generation of V_{CM_SD} turns into the bottleneck. Taking a constant voltage generated

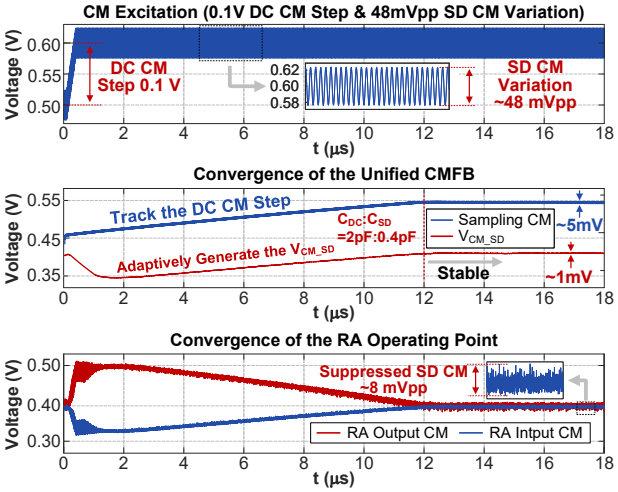


Fig. 5. Simulated transient waves of the unified CMFB excited with a 100-mV input CM step and a 48-mVpp SD CM variation.

outside the loop [4], such as V_{CM_DC}, incurs three issues: 1) Comparator CMP_{SD} offset; 2) CM modulations induced by CMP_{SD} kickback and RA switching; 3) Trip-point mismatch between RA and PVT monitor. Each would result in tens of millivolt errors and fail the SD CMREG.

To eliminate the potential issues, this paper proposes a low-cost adaptive V_{CM_SD} generator to construct a robust unified CMFB loop. The idea is inspired by reverse thinking and noting that, once V_{CM_SD} converges, the outputs of the CM ADC in SD CMREG should wander around its median. In other words, the appropriate V_{CM_SD} is bound to enrich the CM ADC outputs. Therefore, V_{CM_SD} could be adaptively acquired by iteration: if the binary output exceeds 100, increase V_{CM_SD}; otherwise, decrease it. It is further simplified to only judging whether the MSB of the digital output is 1 or 0 (Fig. 4(b)). Notably, the right convergence of the unified CMFB is guaranteed by splitting poles, which is realized by setting C_{DC}:C_{SD} to 2 pF:0.4 pF in this work. Fig. 5 shows the simulated transient waves of the unified CMFB excited with a 100-mV input CM step and a 48-mVpp SD CM variation. Assisted by the adaptive V_{CM_SD} generator, the SD CMREG, comprising a 3-bit CM ADC and DAC with a 50-mVpp range, can always regulate the varying DAC CM to the RA trip-point. Furthermore, the sampling CM and V_{CM_SD} absorb the 100-mV CM step smoothly within 12 μs, and finally, the RA output CM is stabilized to the desired 398 mV and the SD CM variation is suppressed within ±4 mV.

IV. ADC Implementations

Fig. 6 illustrates the ADC architecture and the corresponding timing diagram. Besides the proposed unified CMFB, it consists of a 7-b SAR1, an inverter-based RA, and a 9-b SAR2. The SAR1 employs bottom-plate sampling with 540-fF/side DAC, while the SAR2 adopts top-plate sampling with 65-fF/side DAC. The offset of CMP1 is aligned with the combined offset of RA and CMP2 [5]. A 3-bit dither

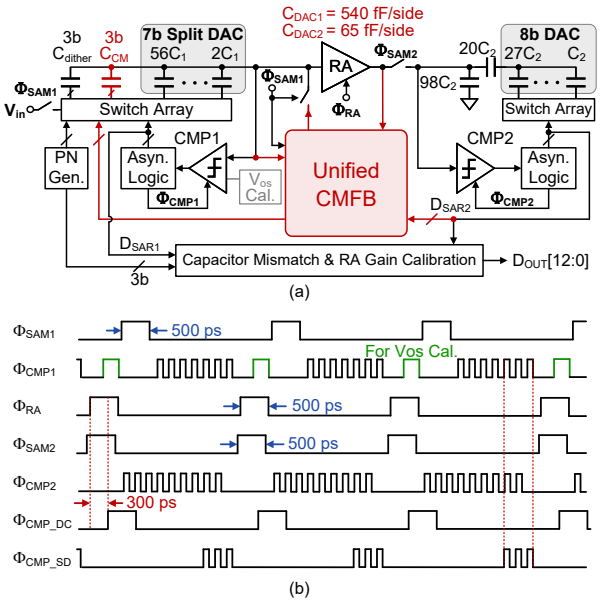


Fig. 6. (a) Overall architecture and (b) corresponding timing diagram of the proposed ADC.

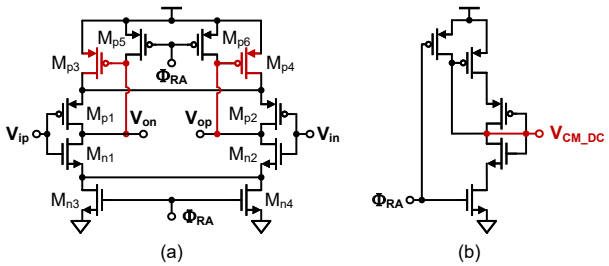
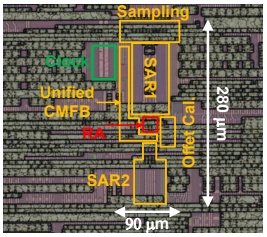


Fig. 7. Detailed implementations of the (a) proposed RA and (b) employed PVT monitor in DC CMFB.

is employed to ensure the convergence of both the unified CMFB and the offset calibration under different inputs. Lastly, as shown in Fig. 7(a) a novel inverter-based RA is proposed to accelerate the amplification. Compared with the traditional topology [4], it features only P-side output CM regulation, thus enabling halved voltage headroom and large bandwidth, which allows 500-ps RA settling time in this work. Notably, the reduced output CM rejection is out of concern, thanks to the proposed unified CMFB.

V. Measurement Results

The proposed ADC is fabricated in 28-nm CMOS. It occupies an active area of 0.022 mm^2 and consumes a total power of 3.73 mW at a 0.9-V supply (Fig. 8), in which the unified CMFB accounts for 8.8% of the total power and 7.7% of the active area. The capacitor mismatch and the RA gain are calibrated off-chip. No fine-tuning of any design parameter is required during test. Fig. 9 and Fig. 10 shows the measured output spectra, DNL, INL and dynamic range. Under a 199.8-MHz input with 1.6 Vpp, the ADC



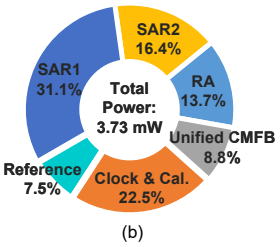


Table I: Critical Performance Summary

Sampling Rate [MS/s]	400
Resolution [bits]	13
Process [nm]	28
Sampling DAC [pF/side]	0.54
Input Swing [Vpp]	1.6
SNDR @LF [dB]	66.2
SFDR @LF [dB]	90.1
SNDR @Nyq. [dB]	**65.7**
SFDR @Nyq. [dB]	**86.8**
Power [mW]	3.73
FoM$_W$ [fJ/c.-s.]	5.9
Core Area [mm^2]	0.022
Input CM Range [V]	**0.3 - 0.8**
Phase Imbalance [deg]	**±25**
Amp. Imbalance [dB]	**±3**
PVT Robust	√
Input Buffer Friendly	√
Balun Friendly	√
Inherent DC CM Modulation Tolerable*	√

* Induced by ADC quantization

Fig. 8. (a) Die micrograph, (b) power breakdown, and critical performance summary of the prototype ADC .

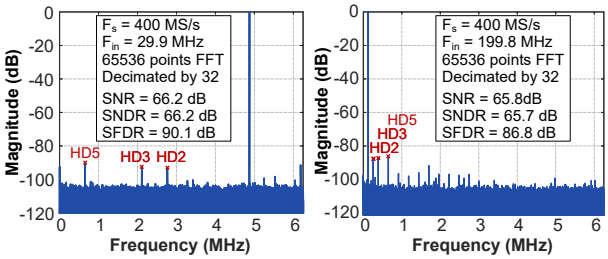


Fig. 9. Measured ADC output spectra at 400-MS/s sampling rate.

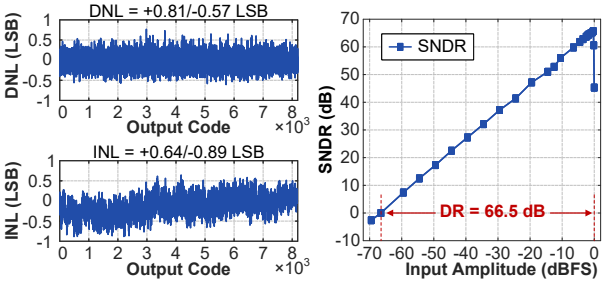


Fig. 10. Measured DNL, INL, and dynamic range at 400-MS/s sampling rate.

achieves 65.7-dB/86.8-dB SNDR/SFDR, yielding an excellent FoM$_W$ of 5.9 fJ/c.-s. Fig. 11 shows the performance under different conditions, demonstrating its robustness to chip, sampling rate, supply voltage and temperature variations. Fig. 12 shows the ADC performance across phase and amplitude imbalance at 1-Vpp differential input, with the tolerable range greatly improved from 10°/1 dB to 25°/3 dB, thanks to the proposed unified CMFB. Impressively, the ADC attains consistent performance across 0.3 V-0.8 V input CM range, even superposed with 8° phase and 1-dB

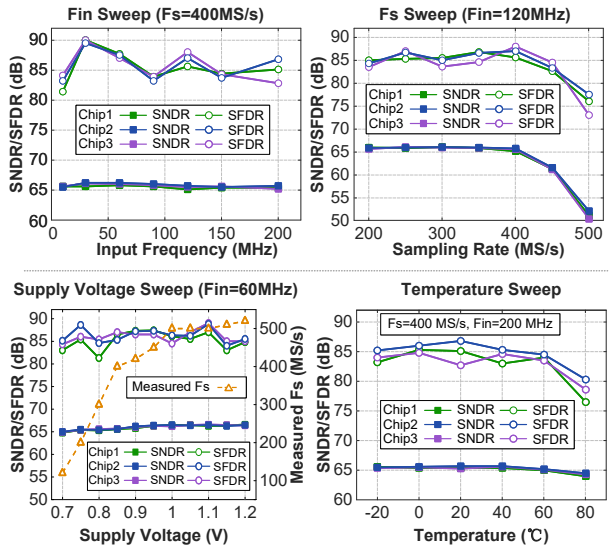


Fig. 11. Measured ADC performance under different conditions.

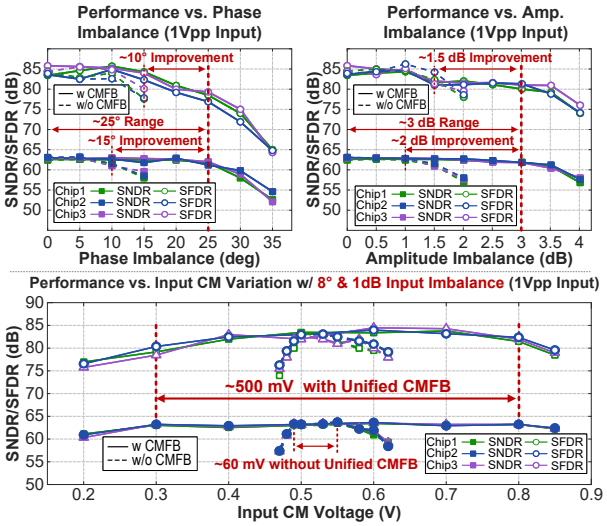


Fig. 12. Measured ADC performance versus phase and amplitude imbalance with or without the proposed unified CMFB, and the performance against input CM variation.

amplitude imbalance, which has never been demonstrated before. All above validate the effectiveness of the unified CMFB. Table I (Fig. 8) summarizes the ADC performance, and Table II compares it with the state-of-the-arts. The prototype ADC achieves the best SFDR and a competitive SNDR, primarily enabled by the proposed unified CMFB, which ensures robust RA performance and significantly relaxes the input buffer and balun requirements, thus enabling a superior-performance sampling network. In addition, both the proposed high-bandwidth RA and lightweight sampling DAC lead to excellent power-and-area efficiency. Furthermore, the novel CMFB concepts are also applicable to other

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work	ISSCC'26 M.R. [6]	VLSI'25 R.T. [3]	VLSI'24 C.C. [7]	ESSERC'24 R.J. [8]	JSSC'18 D.L. [4]
Process [nm]	**28**	28	28	22	40	14
Archi-tecture	**Pipe-SAR**	Pipe-SAR	Sub-ranging	Pipe-SAR	Pipe-SAR	SAR
Resolution [bits]	**13**	12	14	13	13	12
Fs [MS/s]	**400**	500	560	475	300	300
Samp. DAC [pF/side]	**0.54**	0.32	—	2	1.088	1.6
Input Swing [Vpp]	**1.6**	1.8	1.7	2	—	0.8
SNDR @Nyq.[dB]	**65.7**	63.4	72.1	65.9	67.1	60.5
SFDR @Nyq.[dB]	**86.8**	81	79.1	73	79.3	78.5
Input CM Range [mV]	**±250**	—	—	±130	—	±60
Power [mW]	**3.73**	2.69	9.76	6.29	3.32	3.3
FoM_W [fJ/c.-s.]	**5.9**	4.5	5.3	8.3	6.0	12.7
Active Area [mm^2]	**0.022**	0.011	0.078	0.038	0.03	0.006

inverter-based RAs, such as ringamp, to improve the practical usability of corresponding ADCs.

VI. CONCLUSION

This paper proposed a unified CMFB that addresses the issues caused by PVT sensitivities, inherent CM modulations, and SD CM variations of inverter-based RA. A high-bandwidth RA is also proposed to enable fast conversion. The prototype ADC shows robust performance across 0.3V-0.8V input CM range and tolerates extreme input imbalance of ±25° or ±3 dB, while achieving an excellent FoM_W of 5.9 fJ/c.-s.

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