A 50-Gb/s D-band Zero-IF Transceiver for Wireless and Dielectric Waveguide Communication in 28-nm CMOS

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***Abstract*—This paper presents a D-band zero-IF (ZIF) transceiver (TRX) fabricated in 28-nm CMOS. To optimize the D-band radio-frequency front-end (RF-FE), a slotline-based power-combined power amplifier (PA) and a low noise amplifier (LNA) adopting an embedded network core are implemented in the transmitter (TX) and receiver (RX) to improve output power and noise figure (NF) of TRX, respectively. The proposed TRX integrates a phase-locked loop (PLL) along with a ×12 local oscillator (LO) multiplication chain, where the quadrature D-band LO signal is generated by a phase-tunable coupled transmission line (CTL) -based differential hybrid coupler. The inverter-based architectures are adopted to realize baseband continuous-time linear equalization (CTLE) and variable gain amplifier (VGA). Measurement results show that the proposed TRX achieves a data rate of 50 Gb/s by 16QAM in an over-the-air (OTA) link. Over a dielectric waveguide (DWG) channel, a data rate of 30Gb/s QPSK link was demonstrated at 0.5m.**

***Keywords—CMOS, D-band, transceiver, zero-IF, over-the-air, dielectric waveguide*.**

I. Introduction

The sub-terahertz (sub-THz) regime, particularly the D-band (110-170 GHz), offers outstanding bandwidth advantages that can potentially support several tens and even over 100 Gbps data transmission, addressing the ever-growing need for faster wireless connectivity [1]. To further exploit the spectral resources in the D-band, the zero-IF (ZIF) architecture has attracted increasing attention [2], [3]. Compared to heterodyne architecture, the ZIF architecture avoids the bandwidth limitation of low intermediate frequency, thereby maximizing the utilization of the D-band front-end bandwidth. The wideband design of D-band systems imposes more stringent requirements on the RF front-end. Meanwhile, in D-band wideband systems, local oscillator (LO) noise, including phase noise and noise floor, can substantially degrade communication performance, making the design of high-quality LO links essential in fully integrated system applications [4].

This work presents a 50-Gb/s D-band zero-IF transceiver (TRX). To overcome the gain degradation in active amplification stages and excessive insertion loss in passive power combiners in the D-band RF front-end, an embedded network active gain-boosting technique and a slotline-based power-combined passive matching technique are implemented in the RF front-end. To suppress LO phase noise and noise floor, the TRX integrates a low-noise phase-locked loop (PLL) along with a ×12 LO multiplication chain based on the injection-locking technique, providing high-quality D-band LO signals.

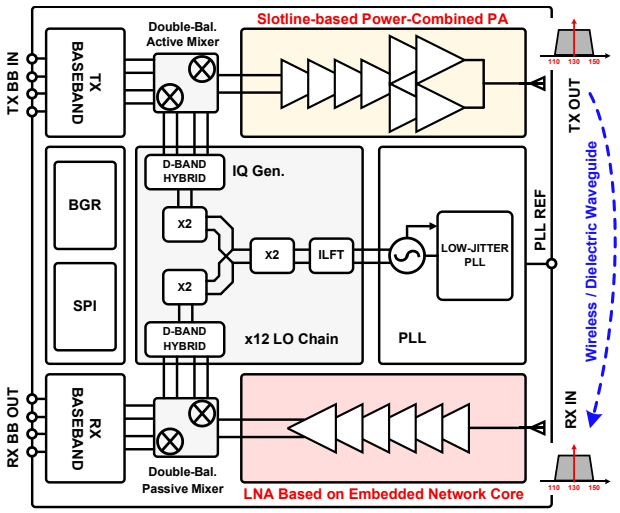


Fig. 1. Top-level architecture of the proposed D-band ZIF TRX.

Additionally, the integrated broadband baseband circuitry provides effective on-chip equalization, thereby obviating the need for external off-chip processing to achieve high-speed data transmission.

II. System Architecture

Fig.1 illustrates the top-level architecture of the proposed D-band ZIF TRX. The transmitter (TX) consists of a slotline-based power-combined PA, an active double-balanced up-conversion mixer, and a two-stage RC source-degeneration CTLE. On the receiver (RX) side, the system features an LNA with an embedded network core, a passive double-balanced down-conversion mixer, and a broadband inverter-based baseband equalization circuit. Double-balanced mixer topologies are leveraged to enhance port-to-port isolation and suppress LO leakage. To synthesize D-band quadrature differential LO signals, the proposed TRX integrates a low-jitter PLL followed by a ×12 frequency multiplication chain. An injection-locked frequency tripler (ILFT) is employed at the input stage of the multiplier chain to optimize phase noise and suppress the noise floor. A phase-tunable CTL-based D-band quadrature hybrid coupler (QHC) is utilized at the output of the ×12 multiplier chain to directly generate the D-band quadrature differential LO signals required for the zero-IF system architecture. The TX and RX share an on-chip LO generation network, thereby achieving transceiver LO synchronization.

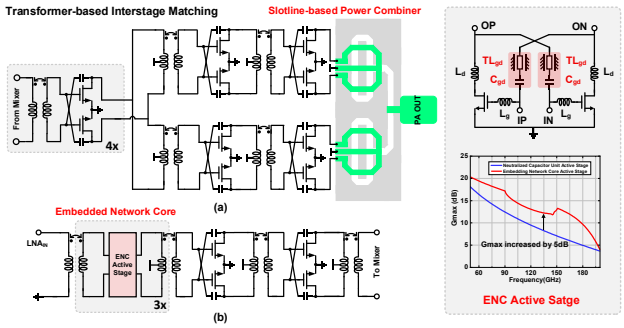


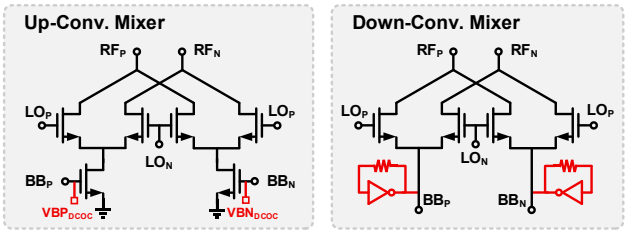
Fig. 2. Schematic of (a): the proposed D-band power combining PA; (b): the proposed D-band LNA and embedded network core active stage.

III. Circuit Implementation

A. D-band PA and LNA

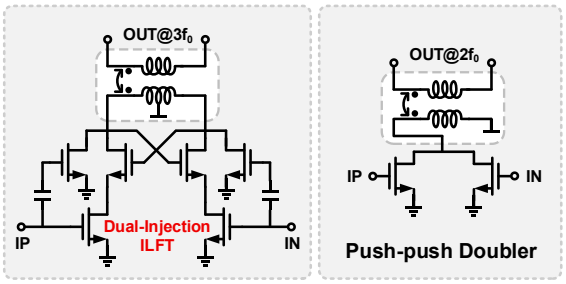
D-band front-end designs are constrained by performance bottlenecks in both active and passive domains. Regarding active circuits, the significant reduction in the intrinsic gain (G_{max}) of transistors leads to insufficient gain performance. For the passive components, the decrease in transformer coil inductance, coupled with increased parasitic effects, makes it difficult to effectively minimize insertion loss. These issues inevitably degrade the signal-to-noise ratio (SNR) of the RF front-end, directly impacting overall system performance. To enhance TX output power, this work adopts a slotline-based power combined PA as shown in Fig. 2(a). Due to its lower insertion loss and superior common-mode rejection compared to transformers, the slotline structure effectively boosts the output power level. Consequently, the two-way power-combined PA achieves a simulated saturated power exceeding 12 dBm.

Low intrinsic gain in D-band active devices often compromises the noise figure (NF) of LNAs. This work utilizes a novel embedded network core (ENC) active stage to implement the D-band LNA, as shown in Fig. 2(b). In contrast to the traditional capacitive-neutralized differential common-source (CS) stages, the proposed ENC incorporates a high-order embedded network based on transmission lines and capacitors, thereby significantly boosting the intrinsic gain of the active unit. Simulation results indicate that the intrinsic gain of the ENC stage is 5 dB higher than that of the neutralized CS counterpart. Consequently, the ENC-based D-band LNA enhances the cascaded gain and suppresses the NF of the RX, achieving the simulated minimum NF of 7 dB.



(a) (b)

Fig. 3. Schematic of (a) up-conv. mixer and (b) down-conv. mixer.



(a) (b)

Fig. 4. Schematic of multiplier: (a) tripler and (b) doubler.

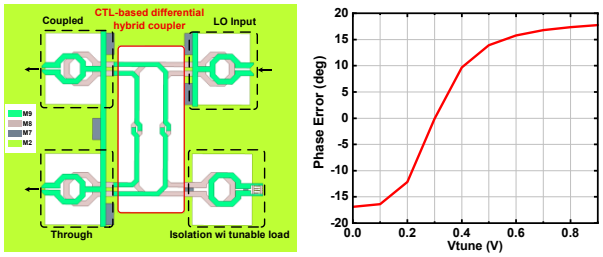


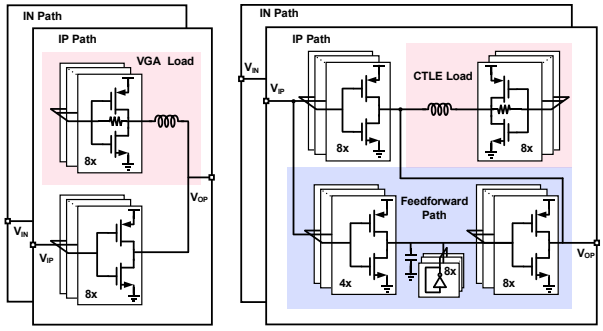
Fig. 5. CTL-based quadrature hybrid coupler and phase error at 130-GHz versus tuning voltage at the isolation port.

B. D-band TX/RX Mixers

Fig. 3 shows the D-band mixer designs in the TRX. Double-balanced topologies are adopted for both TX and RX to ensure superior all-port isolation and minimal LO leakage. In the TX path, an active mixer is utilized to enhance link gain, featuring a DC-offset cancellation (DCOC)-based biasing scheme at the baseband input. This scheme effectively compensates for the switching performance degradation caused by unbalanced biases at the differential baseband terminals arising from process corner variations. For the RX, a passive mixer is selected to optimize linearity. Furthermore, an inverter-based active inductor load is introduced between the passive mixer output and the baseband input. The active inductor design not only provides the necessary DC bias for the passive mixer but also significantly extends the operating bandwidth.

C. LO Generation

As shown in Fig. 1, the LO generation scheme integrates a low-jitter PLL, an ILFT, two push-push frequency doublers, and a CTL-based differential quadrature hybrid coupler. The PLL utilizes an LC delay circuit as a coarse digital-to-time converter (DTC) to suppress DTC-induced phase noise, thereby minimizing the overall clock jitter. To synthesize the D-band LO signal, a ×12 frequency multiplication chain is implemented by cascading an ILFT and two push-push frequency doublers. Compared to conventional non-linear multiplication, the use of injection-locking techniques in this chain provides enhanced harmonic rejection and improved DC-to-RF efficiency, ensuring high spectral purity for the TRX system. To broaden the injection-locking range (ILR), this work employs a dual-injection technique at both the source and drain terminals of the transistors. The architecture of the proposed ILFT is illustrated in Fig. 4(a). Furthermore, the frequency doublers leverage the



(a) (b)

Fig. 6. Schematic of RX baseband (a) VGA and (b) CTLE.

inherent non-linearities of a push-push configuration to extract even-order harmonics, as shown in Fig. 4(b).

ZIF architecture requires the generation of quadrature LO signals directly at the carrier frequency, rendering a high-performance quadrature LO generation scheme essential for overall system integrity. This work adopts a differential QHC based on a coupled transmission line structure, as illustrated in Fig. 5. The differential QHC is implemented with a symmetric topology utilizing the M9 and M8 metal layers. The complete layout includes the CTL-based differential hybrid coupler and impedance matching networks for all ports. To mitigate quadrature phase errors induced by process corner variations, a tunable impedance load, comprised of transistors and transformer, is incorporated at the isolation port. By varying the tuning voltage, precise calibration of the quadrature phase imbalance is achieved. The simulation results of quadrature phase error calibration are presented in Fig. 5, demonstrating a tuning range exceeding ±15°, which provides sufficient margin to maintain high I/Q isolation across various process corners.

D. Baseband Circuits

The architecture of the RX baseband circuit is depicted in Fig. 6. An inverter-based topology is adopted to provide both equalization and amplification for the down-converted baseband signal. The gain is regulated through transconductance unit-cell scaling, a method that enhances gain stability against process variations. To compensate for high-frequency loss, on-chip equalization is realized via a feed-forward compensation path. Additionally, the integration of active inductors and peaking inductors in the load stages significantly extends the -3 dB bandwidth to 17.5 GHz, ensuring robust performance for wideband baseband signals.

IV. Measurement Results

Fig. 7 shows the die micrograph of the TRX, fabricated in 28-nm CMOS with a total die area of 2.82 × 1.47 mm^2. In all measured environments, the chip is wire-bonded to the PCB carrier board. The continuous-wave (CW) measurement setup and corresponding results are illustrated in Fig. 8. To characterize the RF FE performance of the TX and RX, the WR6.5 waveguide probe and VDI frequency extension system are utilized. The external PLL reference clock is provided by the signal generator R&S SMA 100B. All measured results are

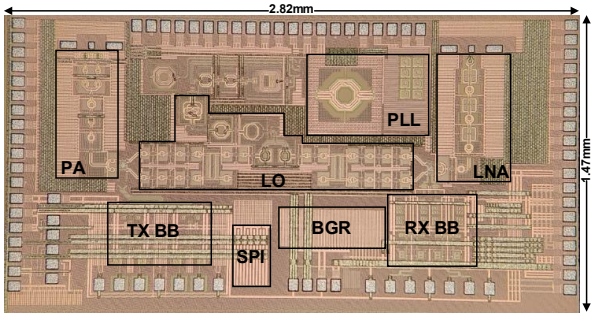


Fig. 7. TRX chip micrograph.

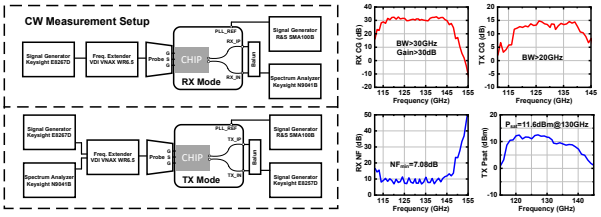


Fig. 8. TRX chip CW measurement setup and results.

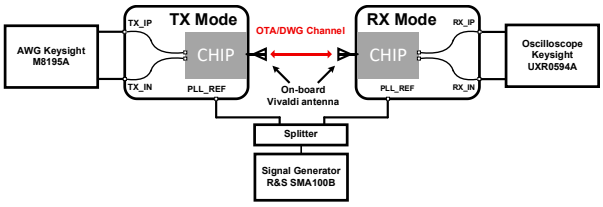


Fig. 9. OTA/DWG measurement setup of TRX chip.

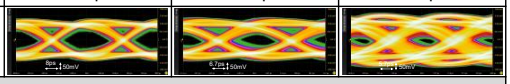
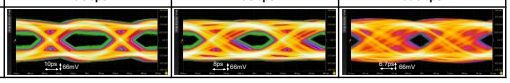
OTA Link			
Data Rate	25Gbps	30Gbps	35Gbps
Eye Diagram QPSK			
DWG Link@50cm			
Data Rate	20Gbps	25Gbps	30Gbps
Eye Diagram QPSK			

Fig. 10. Eye diagrams of QPSK modulation in OTA/DWG link.

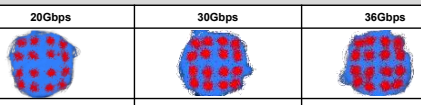
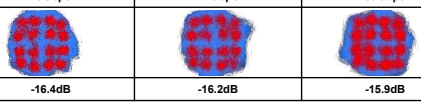
OTA Link			
Data Rate	20Gbps	30Gbps	36Gbps
Constellation 16QAM			
EVM_{RMS}	-18.2dB	-17.4dB	-16.9dB
Data Rate	40Gbps	44Gbps	50Gbps
Constellation 16QAM			
EVM_{RMS}	-16.4dB	-16.2dB	-15.9dB

Fig. 11. Measured constellations and EVM_{RMS} of 16QAM modulation in the OTA link.

Table 1. Performance comparison of the state-of-the-art D-band transceivers.

	This work		RFIC'24 [2]		JSSC'23 [3]		JSSC'23 [5]	JSSC'24 [6]		RFIC'22 [7]	
Process	**28 nm CMOS**		22nm FDSOI		28nm CMOS		22nm FinFET	28nm CMOS		45nm RFSOI	
Frequency (GHz)	**130**		135		135		140	141		LB: 143.6, UB: 152.3	
Integration Level	**ZIF TRX**		ZIF TX		ZIF TX+RX		ZIF RXFE+ADC	Super-Het TRX		Super-Het TX+RX	
BW (GHz)	**TX: 23, RX: 32**		14		TX:15, RX:16		21	TX:21, RX:18		Total: 18	
TX P_{sat} (dBm)	**11.6**		11		0		N/A	13.1		EIRP: 16(LB), 10(UB)	
RX NF (dB)	**7.08**		N/A		6		12.4*	9.3		10	
Link Channel	**OTA**	**DWG**	Probe		OTA	DWG	Probe	OTA		OTA	
Modulation	**16QAM**	**QPSK**	16QAM	64QAM	16QAM		16QAM	QPSK	16QAM	16QAM	64QAM
Data Rate (Gb/s)	**50**	**30**	56	30	32	24	128^	24	48	56	48
EVM_{RMS} (dB)	**-15.9**	**N/A**	-17	-25	N/A		-15.2	-15	-15.5	-14	-20
Distance (m)	**0.02**	**0.5**	N/A		0.02	1	N/A	0.01		0.03	
Power (mW)	**1100**		928		287		249	1716	1816	1020	

*simulated result ^with offline DSP

presented after de- embedding.

For the RX FE measurement configuration, the D-band input signal is generated by a ×12 frequency extension module, followed by a D-band attenuator to prevent receiver saturation. The input power is precisely calibrated at the probe interface. The down-converted RX baseband signal is routed through grounded coplanar waveguide (GCPW) lines on the PCB and analyzed using a Keysight N9041B spectrum analyzer. The measured RX conversion gain exceeds 30dB across a bandwidth of 32 GHz, spanning from 115 to 147 GHz. The RX NF is measured using the cold-source method. The NF remains below 12 dB from 115 to 145 GHz, achieving a minimum NF of 7.08 dB at 126 GHz. In the TX measured setup, the output is characterized using a D-band down-conversion link comprising a WR6.5 probe, a frequency extension module in receiver mode, and a Keysight E8267D signal generator providing the frequency extension module LO. The measured TX conversion gain achieves 15 dB peak gain across a bandwidth of 23 GHz, spanning from 117 to 140 GHz. The saturated output power P_{sat}, measured with a VDI Erickson PM5B power meter, reaches a maximum of 12.5 dBm at 127 GHz.

Fig. 9 shows the over-the-air (OTA) and dielectric waveguide (DWG) measured environments. A Vivaldi antenna on Megtron6 substrate is wire-bonded to the TRX and integrated onto an FR4 carrier board. For QPSK modulation characterization, NRZ signals are applied to the I/Q paths. The measured eye diagrams for the OTA link and DWG link are shown in Fig. 10. The OTA link was evaluated at a 2-cm distance, achieving a peak data rate of 35 Gb/s, while the 50-cm DWG link achieved 30 Gb/s. To further evaluate high-order modulation performance, 16QAM constellation measurements were conducted using a Keysight M8195A AWG for signal generation and a Keysight UXR0594A oscilloscope for demodulation. The measured constellation results in the OTA link are shown in Fig. 11. The OTA link achieves a maximum data rate of 50 Gb/s with an EVM_{RMS} of -15.9 dB.

V. Conclusion

A D-band ZIF transceiver for both over-the-air (OTA) and dielectric waveguide (DWG) communication is reported. Key innovations include a slotline-based power combiner and an embedded-network active stage, designed to overcome the gain and power constraints of D-band front-ends. The LO generation utilizes an ILFT-based multiplication chain and a CTL-based QHC for precise quadrature signal synthesis. With a fully integrated PLL and analog baseband, the TRX achieves a peak data rate of 50 Gb/s with 16QAM in the OTA link and 30 Gb/s with QPSK in the DWG link, validating its efficacy for next-generation high-capacity backhaul and short-range communication.

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