A 248 μW 0.2–2.23 GHz Inductorless Low-Noise Amplifier With G_m-Boosting and Dual Active Shunt-Feedback

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***Abstract*—A differential wideband common-gate (CG) low-noise amplifier (LNA) using a complementary current reuse structure with g_m-boosting and dual active shunt feedback is proposed. In a conventional CG LNA with active shunt feedback, the noise figure (NF) and power consumption are mainly limited by the transconductance of the CG transistor and the feedback gain under the input matching condition. In the proposed work, dual active shunt feedback is utilized to add degrees of freedom in the choice of the transconductance as well as reduce the current dissipation of the CG transistor. Moreover, by employing the capacitive cross-coupling (CCC) based g_m-boosting technique, both the noise contribution and current dissipation of the CG transistor can be reduced by half theoretically. Fabricated in 28 nm CMOS, the LNA achieves a voltage gain of 14.8 dB with a 3-dB bandwidth of 0.2 to 2.23 GHz, a minimum NF of 4.15 dB at 1.1 GHz and an IIP3 of -7 dBm at 1 GHz. It consumes 248 μW from a 0.8 V supply and occupies a very compact active area of 0.009 mm^2.**

***Keywords*—Inductorless, wideband, CMOS low-noise amplifier (LNA), g_m-boosting, shunt feedback, current reuse.**

I. Introduction

With the proliferation of portable wireless devices, the design of low-power wideband low-noise amplifiers (LNAs) has been an active research topic [1]-[9]. Herein, the power consumption (P_{DC}) is constrained within 0.5 mW in works [2]-[3] targeting ultra-low power (ULP) applications. In general, for a common-gate (CG) LNA, the required transconductance of the CG transistor can be calculated as $1/R_S$ for the input matching ($R_{in} = R_S$), where R_{in} is the input impedance and R_S is the source impedance. In this case, the noise contribution of the CG transistor is fixed to be γ, where γ is the excess noise coefficient, resulting in a tight relationship among input matching, noise figure (NF) and P_{DC}. Usually, there are two popular techniques to reduce the power consumption without sacrificing the input matching: the shunt feedback and current reuse. The former aims to lower the required transconductance under the input matching condition at the cost of NF while the latter aims to increase the transconductance without consuming extra current dissipation at the cost of supply voltage. By using these two techniques, work [2] achieves a minimum NF of 4.9 dB with a current dissipation of 0.4 mA from a 1 V supply. Instead of the load resistor, load inductor is utilized in work [3] to lower the supply voltage. As a result, it achieves a minimum NF of 4.5 dB with a current dissipation of 0.4 mA from a 0.4 V supply. However, three on-chip inductors are used, resulting in a large silicon area. Thus, under ULP constraint, it is still challenging to achieve a good trade-off among the input matching, NF and silicon area.

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TABLE I. Comparison of Characteristics

	CG LNA with active shunt feedback	Proposed CG LNA with active shunt feedback and g_m-boosting
R_{in}	$\frac{1}{g_{m1}(1+A)}$	$\frac{1}{g_{m1}(1+A+B)(1+C)}$
g_{m1} for input matching	$\frac{1}{(1+A)R_S}$	$\frac{1}{(1+A+B)(1+C)R_S}$
F with input matched	$1+\gamma(1+A)+\frac{R_S}{R_1}(2+A)^2$	$1+\frac{\gamma(1+A+B)}{1+C}+\frac{R_S}{R_1}(2+A+B)^2$

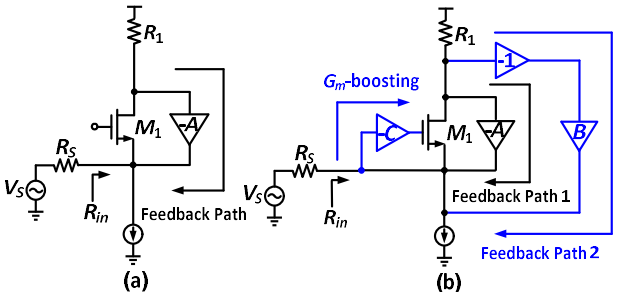
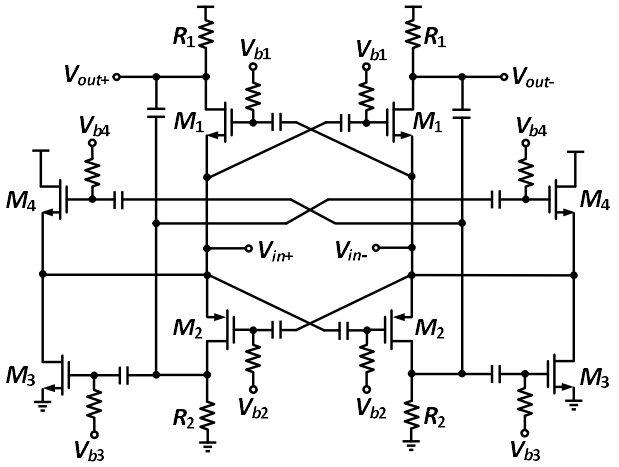


Fig. 1. Diagram of (a) the CG LNA with active shunt feedback, (b) proposed CG LNA with dual active shunt feedback and g_m-boosting.

Fig. 1(a) shows the conventional CG LNA with shunt feedback, where the CG LNA can be regarded as the case when the feedback gain $A = 0$. Thanks to the negative feedback, the required g_{m1} for the input matching is reduced by a factor of $(1 + A)$, where g_{mx} is the transconductance of M_x ($x = 1 – 4$). However, the low power consumption is achieved at the cost of NF: 1) Due to the negative feedback, the noise contribution of the CG transistor M_1 is increased by a factor of $(1 + A)$. 2) In addition to the noise contribution of the CG transistor, the load resistor R_1 also contributes the noise to the NF of the LNA. To reduce it, a large value of R_1 is of necessity. However, a large R_1 leads to a large voltage drop across R_1, which results in a high supply voltage. 3) To effectively suppress the noise contribution of R_1 without sacrificing the supply voltage, it is desirable that the current dissipation of the CG transistor is controlled as low as possible, which greatly increases the design complexity by using one negative feedback path.

To solve these issues, an inductorless CG LNA with dual active shunt feedback and g_m-boosting is proposed for ULP applications. The aim is to maximize the negative feedback gain to minimize the power consumption without sacrificing input matching and NF. As shown in Fig. 1(b), it uses two negative feedback paths to add more flexibility in determining the required g_{m1} for input matching. Meanwhile, the g_m-boosting technique is employed to further reduce the current dissipation and noise contribution of CG transistor simultaneously. To clearly show the impact of dual negative



M_1	15 μm/30 nm	M_2	6 μm/30 nm	R_1, R_2	1.5 kΩ
M_3	4 μm/60 nm	M_4	4 μm/60 nm	I_D	310 μA

Fig. 2. Schematic of the differential LNA in current reuse structure.

feedback and g_m-boosting on the input matching and NF, the comparison of characteristics of CG LNAs are summarized in Table I. The detailed theoretical analysis and measurement are given in Section II and III, respectively. Finally, Section IV concludes this paper.

II. The Proposed LNA

A. Basic Idea

Fig. 2 shows the schematic of the proposed differential LNA with dual active shunt feedback and g_m-boosting using a complementary current reuse structure with detailed design values. Herein, the negative feedback path 1 is realized by transistor M_3, which provides a conventional feedback gain A used in works [2]-[3]. To add degrees of freedom in the choice of the transconductance as well as reduce the current dissipation of the CG transistor, an extra negative feedback path 2 is used in this work. The output signal of the CG LNA is inverted and then applied to the gate terminal of transistor M_4, which generates a negative signal at the input. The negative feedback path 2 is therefore created, which provides an extra feedback gain B. As mentioned earlier, although the negative feedback relaxes the transconductance requirement of the CG transistor for input matching, it degrades the noise performance. To suppress the noise contribution of the CG transistor, the g_m-boosting technique is employed in this work to reduce the current dissipation and NF simultaneously. In practice, the realization of g_m-boosting can be active and passive. The active approaches introduce extra noise, which deteriorates the noise performance under ULP constraints. The passive approaches can be realized through differential capacitive cross-coupling (CCC) and on-chip transformers. The former is chosen in this work as the latter requires large silicon area and therefore is not suitable for the area-sensitive applications. It is worth noting that the boosted gain C is limited to unity by using CCC-based g_m-boosting technique. In this case, the complementary current reuse structure is adopted in this work to further reduce the current dissipation. As a result, compared with previous works, this work achieves the lowest current dissipation of 310 μA with the lowest NF of 4.15 dB thanks to the dual active shunt feedback, g_m-boosting and current reuse.

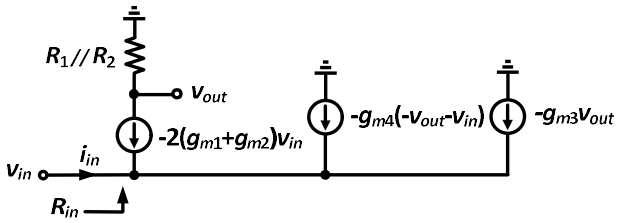


Fig. 3. Equivalent small-signal model for input impedance and gain analysis.

B. Input Impedance and Gain

To calculate the input impedance, R_{in} and gain, A_v of the LNA, the equivalent small-signal model is shown in Fig. 3. By applying Kirchhoff's current law at v_{in} and v_{out}, we have:

$$\begin{cases} v_{out} = 2(g_{m1}+g_{m2})(R_1 // R_2)v_{in} \\ i_{in} = \dfrac{v_{in}}{R_{in}} = 2(g_{m1}+g_{m2})v_{in} + g_{m3}v_{out} + g_{m4}(v_{out}+v_{in}) \end{cases} \tag{1}$$

Solving these equations yields

$$\begin{cases} \dfrac{v_{out}}{v_{in}} = 2(g_{m1}+g_{m2})(R_1 // R_2) \\ \dfrac{1}{R_{in}} = 2(g_{m1}+g_{m2})\left(1 + g_{m3}(R_1 // R_2) + g_{m4}(R_1 // R_2) + \dfrac{g_{m4}}{2(g_{m1}+g_{m2})}\right) \end{cases} \tag{2}$$

According to equation (2), the feedback gain A and B in this work can be expressed as $A = g_{m3}(R_1 // R_2)$, $B = g_{m4}(R_1 // R_2) + g_{m4}/2(g_{m1} + g_{m2})$, which is approximated as $B = g_{m4}(R_1 // R_2)$ in this work since $g_{m4} \ll 2(g_{m1} + g_{m2})$ in the practical design. For example, g_{m4} is set as 0.574 mS and $2(g_{m1} + g_{m2})$ is set as 9.4 mS in this work to achieve a low NF, which is detailed in Section II-C. In this case, under the input matching condition, the input impedance and gain can be simplified as:

$$R_{in} = \frac{1}{2(g_{m1}+g_{m2})(1+A+B)} = R_S \tag{3}$$

$$A_v = \frac{R_1 // R_2}{(1+A+B)R_S} = G_m(R_1 // R_2) \tag{4}$$

Equation (3) indicates the required $g_{m1} + g_{m2}$ for the input matching here is $1/2(1 + A + B)$ of that of a pure CG LNA. Meanwhile, a large value of A and B facilitates small g_{m1} and g_{m2} for the input matching. However, it is achieved at the cost of the equivalent transconductance, G_m. Equation (4) indicates the G_m under the input matching condition is $1/(1 + A + B)$ of that of a pure CG LNA. Thus, there exists a trade-off among the current dissipation, gain and bandwidth. In the practical design, raising A and B is realized by raising g_{m3}, g_{m4} and the parallel resistance $R_1 // R_2$. The former leads to an increased DC current of M_3 and M_4. While the latter leads to a reduced bandwidth of the LNA as well as increased voltage drop across load resistors. Especially, assuming $R_1 = R_2 = R$, the voltage drop doubles while the equivalent parallel resistance is halved when raising R, which increases the requirement on the supply voltage.

Based on the above analysis, both the values of A and B are chosen below unity in this work. By setting g_{m3} = 0.643 mS, g_{m4} = 0.574 mS, $R_1 = R_2$ = 1.5 kΩ, the value of A and B can be calculated as 0.48 and 0.43, respectively. In this case, an S_{11} below -20 dB can be achieved, which indicates a good input matching condition is obtained.

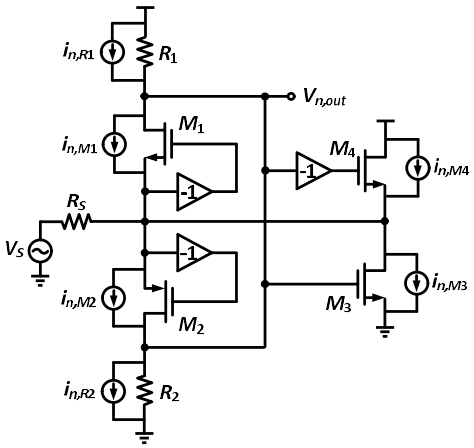


Fig. 4. Noise sources in the LNA.

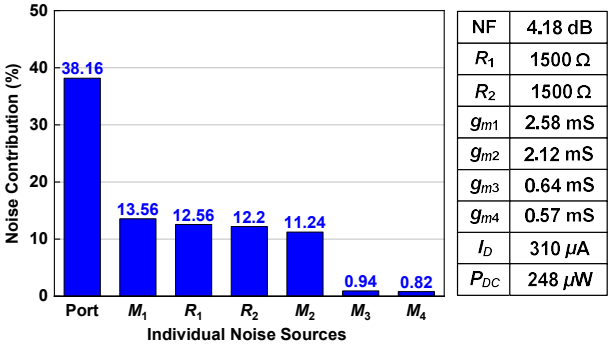
C. Noise Analysis

Fig. 4 shows the simplified single-ended diagram of the LNA highlighting the main noise sources, where only the thermal noise is considered for simplicity. Herein, the thermal channel noise of M_1, M_2, M_3 and M_4 is modeled as the current source $i_{n,M1}$, $i_{n,M2}$, $i_{n,M3}$ and $i_{n,M4}$, respectively, and the thermal noise of R_1 and R_2 is modeled as the current source $i_{n,R1}$ and $i_{n,R2}$, respectively. These noise sources are uncorrelated, and hence the output voltage noise $v_{n,out}$ denotes the total noise generated by $i_{n,M1}$, $i_{n,M2}$, $i_{n,M3}$, $i_{n,M4}$, $i_{n,R1}$ and $i_{n,R2}$. Then the noise factor of the LNA can be calculated as

$$F = 1 + \frac{\gamma(1+A+B)}{2} + \gamma g_{m3} R_S + \gamma g_{m4} R_S + \frac{R_S}{R_1 // R_2}(2+A+B)^2 \quad (5)$$

The second term denotes the simplified $F_{M1} + F_{M2}$, which is the noise contribution of the M_1 and M_2. Obviously, it is reduced by a factor of 1/2 by employing the g_m-boosting technique. The third and fourth term denote the noise contribution of M_3 and M_4, which is proportional to g_{m3} and g_{m4}, respectively. Thus, small values of g_{m3} and g_{m4} are desirable to limit their noise contributions. The last term denotes the simplified $F_{R1} + F_{R2}$, which is the noise contribution of R_1 and R_2. To decrease this term, a large value of $R_1 // R_2$ is desirable. For example, $R_1 // R_2$ can be set over 10 times of R_S to effectively limit its noise contribution.

To clearly show the relationship between transconductance and noise contribution, simulation is performed. The simulated thermal noise contributions from individual components at 1 GHz are shown in Fig. 5. Firstly, the total noise contribution of M_1 and M_2 accounts for 24.8%. Thanks to the g_m-boosting and dual negative feedback techniques, the required g_{m1} and g_{m2} are as small as 2.58 and 2.12 mS, respectively, which requires a small DC current of 130 μA. In this case, even with a large load resistance $R_1 = R_2 = 1.5$ kΩ, the voltage drop across each resistor is only 195 mV, and hence the supply voltage is chosen as 800 mV in this work. Secondly, thanks to large value of R_1 and R_2, their noise contribution can be effectively suppressed, which accounts for 24.76%. Thirdly, the noise contribution of M_3 and M_4 can be ignored by minimizing g_{m3} and g_{m4}. It is because that the feedback gain is mainly determined by R_1, R_2, g_{m3} and g_{m4}. Due to the large value of R_1 and R_2, a small g_{m3} (0.64 mS) and g_{m4} (0.57 mS) can be chosen in this work. As a result, a simulated NF of 4.18 dB is achieved at 1 GHz with a current dissipation of 310 μA.



NF	4.18 dB
R_1	1500 Ω
R_2	1500 Ω
g_{m1}	2.58 mS
g_{m2}	2.12 mS
g_{m3}	0.64 mS
g_{m4}	0.57 mS
I_D	310 μA
P_{DC}	248 μW

Fig. 5. Simulated thermal noise contributions from individual components at 1 GHz in this work.

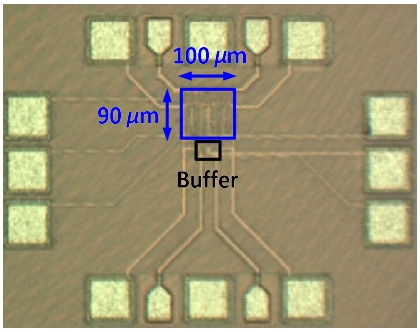


Fig. 6. Die photograph of the fabricated LNA.

III. Measurements

The proposed differential CG LNA was fabricated in a standard 28 nm CMOS technology. It draws 310 μA from a 0.8 V supply, consuming a power consumption of 248 μW. Fig. 6 shows the die photo of the fabricated LNA, where a CS buffer with a unity gain is used for measurement purpose. As highlighted in the die photo, the active area of the LNA is 100 μm × 90 μm, excluding the output buffer.

The chip was measured on-wafer using a probe-station. To measure the S-parameters, the input and output signals are applied using two G-S-G-S-G differential RF probes. As shown in Fig. 7, the measured S_{11} is well controlled below -12 dB up to 4 GHz. The LNA achieves an S_{21} of 14.8 dB with a 3-dB bandwidth of 0.2 to 2.23 GHz. The trend of the measured NF agrees well with that of the post-layout simulation result over the entire working band. The measured NF achieves a minimum value of 4.15 dB at 1.1 GHz and varies from 4.15 to 5.24 dB in the 2.03-GHz bandwidth. It deteriorates at lower frequencies below 0.2 GHz mainly due to the flicker noise. By applying two tones with 10 MHz spacing, an IIP3 of -7 dBm is measured at 1 GHz, where the gain is 14.1 dB.

Table II benchmarks the performance of the proposed work with the state-of-the-art low-power wideband LNAs. Three Figures of Merit (FoM I [10], FoM II [10] and FoM III [1]) are used for comparison purpose. The achieved FoM I is slightly lower than that of work [3] when only considering the gain, bandwidth, power consumption and NF. It is because that load inductor rather than resistor is utilized in work [3], resulting in an ultra-low voltage (ULV) of 0.4 V. Indeed, the current dissipation (310 μA) of this work is still lower than that (400 μA) of work [3], and the load resistor of this work can also be replaced with an inductor for ULV applications at the cost of silicon area. When taking the linearity and silicon

TABLE II. PERFORMANCE SUMMARY AND COMPARISON

	CMOS Tech.	Freq. Range (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	Type/ Num. of inductors	Active Area (mm^2)	FOM I	FOM II	FOM III
This Work	**28 nm**	**0.2–2.23**	**11.8–14.8**	**4.15–5.24**	**-7**	**0.8**	**0.248**	**D/0**	**0.009**	**28.98**	**14.98**	**55.89**
[2] TMTT'16	130 nm	0.1–2.2	9.3–12.3	4.9–6	-11.5	1	0.4	S/0	0.0052	20.30	-2.70	42.98
[3] JSSC'16	130 nm	0.6–3.1	10–13	4.5	-12	0.4	0.16	S/3	0.39	31.68	7.68	15.86
[4] TVLSI'15	90 nm	0.1–7	9.6–12.6	5.5–6.5	-9 @ 5 GHz	0.5	0.75	S/2	0.23	23.75	5.75	18.52
[5] JSSC'21	28 nm	0.02–4.5	12–15.2	2.09–3.2	-4.62	1	4.5	S/1	0.03	19.34	10.10	40.56
[6] ISSCC'22	28 nm	0.25–3	16.6–19.6	2.7	-8.5	1	3.4	S/0	0.0078	19.05	2.05	44.20
[7] ESSCIRC'23	28 nm	0.25–3.7	7.2–10.2	2.4	4.1	1.2	7.9	D/0	0.021	5.65	13.85	47.40
[8] ESSERC'24	28 nm	0.25–2.7	14.7–17.7	2.9–3.7	-6.8	0.6	1.59	S/0	0.0076	21.90	8.30	50.69
[9] TCAS-I'24	28 nm	0.2–2.85	17–20	2.9-3.6	-12.3	0.6	1.74	S/0	0.0048	24.10	-0.50	45.88

S single-ended topology, D differential topology

$$\text{FoM I} = 20\log_{10}\left(\frac{\text{BW[GHz]}\cdot\text{Gain[abs]}}{P_{\text{DC}}[\text{mW}]\cdot(F_{\text{min}}-1)}\right),\ \text{FoM II} = 20\log_{10}\left(\frac{\text{BW[GHz]}\cdot\text{Gain[abs]}\cdot\text{IIP3[mW]}}{P_{\text{DC}}[\text{mW}]\cdot(F_{\text{min}}-1)}\right),\ \text{FoM III} = 20\log_{10}\left(\frac{\text{BW[GHz]}\cdot\text{Gain[abs]}\cdot\text{IIP3[mW]}}{P_{\text{DC}}[\text{mW}]\cdot(F_{\text{min}}-1)\cdot A[\text{mm}^2]}\right)$$

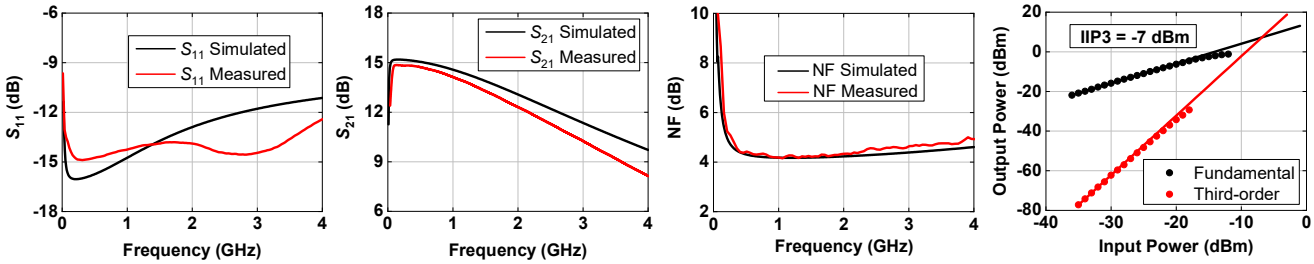


Fig. 7. Measurement and post-layout simulation results of S_{11}, S_{21}, NF, and measured IIP3 at 1 GHz.

area into consideration, this work achieves the highest FoM II and FoM III among the previously reported low-power LNAs.

IV. CONCLUSION

This paper presents an inductorless differential wideband CG LNA with dual negative shunt feedback and g_m-boosting for ULP applications. Herein, the dual negative shunt feedback is used to minimize the required transconductance of the CG transistor for input matching. The CCC-based g_m-boosting technique is used to theoretically reduce both the noise contribution and current dissipation of the CG transistor by half. Moreover, the complementary current reuse structure is adopted to increase the equivalent transconductance without consuming extra current dissipation and therefore further reduce the power consumption performance. Fabricated in 28 nm CMOS, this work shows competitive performance with respect to state-of-the-art low-power wideband LNAs.

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