A –112 dBc THD+N, 20 kHz Tracking-Bandwidth Class-H Headphone Amplifier with SIBO Converter

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***Abstract*—Conventional Class-G/H headphone amplifiers are limited by the current constraints of the SIBO converter, resulting in insufficient tracking bandwidth, degraded efficiency, and increased distortion, while rapid switching and supply variations further introduce EMI and crossover distortion. Therefore, this paper proposes a Class-H headphone amplifier with an SIBO converter integrated with burst-and-restore capacitors (BREC) to enhance tracking speed and enable energy recycling, achieving a 20-kHz tracking bandwidth. Moreover, a pass-gate current controller (PGCC) suppresses EMI, and a symmetric supply-independent bias control (SSBC) reduces distortion. Fabricated in 28-nm CMOS, the design achieves a THD+N of −112 dBc and 21% lower power consumption at 10 mW, demonstrating improved efficiency and linearity.**

Keywords—Class-H audio amplifier, EMI-reduced gate driver, Energy recycling, Envelope tracking, Low EMI, Low THD+N, Power efficiency, Quiescent current control, Supply-independent bias, Wideband tracking

I. Introduction

The rapid growth of portable devices, such as smartphones and wireless headphones, demands highly efficient, low-distortion, and compact audio amplifiers. Since audio playback is frequently used, amplifier efficiency directly impacts battery life and user experience. While Class-G amplifiers improve efficiency by switching among discrete supply rails [1]–[3], their limited voltage levels prevent continuous audio envelope tracking. To address this, Class-H amplifiers enable continuous envelope tracking, further reducing power loss while maintaining linearity; however, their efficiency heavily depends on tracking bandwidth and switching accuracy. In [4], a conventional single-inductor bipolar-output (SIBO) converter was adopted as the power stage in a Class-H headphone amplifier, demonstrating improved efficiency. However, its tracking performance is fundamentally constrained by the energy and current limits described in (1) and (2). Equation (1) indicates that the inductor energy per switching cycle must exceed the combined energy required for charging the output capacitors and supplying the load. Equation (2) further shows that achieving faster up-tracking requires a higher peak inductor current $I_{L,peak}$. Although increasing $I_{L,peak}$ enhances tracking speed, it also introduces larger input current ripple, leading to severe electromagnetic interference (EMI) and potential input voltage instability.

$$E_L > \Delta E_{Cout,P} + \Delta E_{Cout,N} + E_{out} \tag{1}$$

$$I_{L,\text{peak}} > 2\frac{V_{out}}{V_{IN}}\left(2C_{out}\frac{dV_{out}}{dt} + \frac{P_{out}}{V_{out}}\right) \tag{2}$$

On the other hand, the down-tracking speed is limited by the available discharge current, as described in (3), where the load current (I_{load}) and quiescent current (I_q) determine the falling slew rate. This inherently restricts how fast the supply voltage can follow a decreasing audio envelope. As a result, insufficient up- and down-tracking speeds lead to signal clipping, distortion, and efficiency degradation, as illustrated in Fig. 1.

$$|SR_{down}| = \frac{I_{load} + I_q}{C_{out}} \geq \left|\frac{dV_{out}}{dt}\right| \tag{3}$$

Furthermore, since the supply voltage in Class-H operation continuously varies with the audio envelope, maintaining balanced bias currents in the output stage is critical. Without proper control, a mismatch in the quiescent currents of complementary power transistors can induce crossover distortion, significantly degrading total harmonic distortion plus noise (THD+N).

This work presents a Class-H audio amplifier that addresses the aforementioned challenges by utilizing an SIBO converter as the supply modulator. To extend tracking bandwidth without increasing EMI, a burst-and-recycle energy capacitor (BREC) scheme is integrated into the supply path. Additionally, a pass-gate current controller (PGCC) is employed to suppress EMI at the SIBO outputs. Furthermore, a fully symmetric, supply-independent bias current controller is introduced to stabilize the quiescent current of the Class-AB output stage under varying supply voltages, thereby reducing crossover distortion and enhancing overall linearity.

II. Proposed SIBO Converter with BRECs

Fig. 2 shows the architecture of the proposed Class-H headphone amplifier, where the SIBO converter is powered by a 1.8-V input supply (V_{IN}). It generates a fixed negative rail (V_{SS}) for the analog audio circuits, as well as two envelope-tracking outputs ($V_{out,P}$ and $V_{out,N}$), providing the positive and negative supply voltages for the stereo headphone output stage.

Fig. 3 illustrates the proposed SIBO converter integrated with the BREC technique. The BREC consists of two capacitor banks, BREC,P and BREC,N, dedicated to positive and negative voltage operations, respectively. During up-tracking, the selected capacitor bank supplies energy to $C_{out,P}$ or $C_{out,N}$ through switches S_9 or S_{10} in burst mode, enabling a rapid voltage increase without additional conducted EMI at V_{IN}. During down-tracking, the capacitor banks recover excess energy through the SIBO converter, effectively reducing power loss and enhancing overall efficiency.

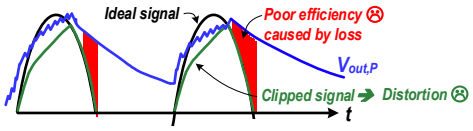


Fig. 1. Signal distortion and efficiency loss caused by insufficient tracking bandwidth of the positive supply voltage $V_{out,P}$.

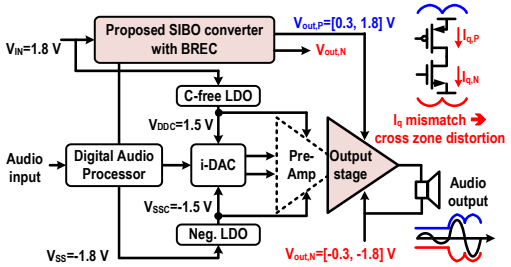


Fig. 2. System architecture of proposed Class-H audio amplifier.

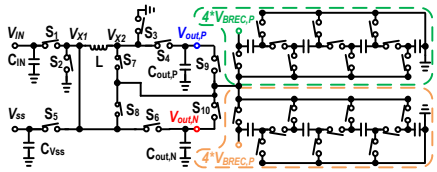


Fig. 3. Proposed SIBO converter with the BREC technique.

A. Pre-store Phase Under Light-Load Conditions

Under light-load conditions, the SIBO converter operates in discontinuous conduction mode (DCM), where the inductor current (I_L) periodically falls to zero, creating idle intervals between switching cycles. As illustrated in Fig. 4, a pre-store phase ($\Phi_{Prestore}$) is inserted during these zero-current intervals to utilize the otherwise unused time. The BREC,P and BREC,N shares similar operation. During $\Phi_{Prestore}$, the BREC,P and BREC,N capacitor banks are reconfigured as auxiliary energy storage nodes. Through the same switching sequence as the conventional Φ_1–Φ_2 operation, charge is transferred from the input through the inductor and selectively stored in the BREC capacitors. This operation does not interfere with the main output regulation since it occurs only when I_L=0, thereby avoiding additional current stress or EMI on V_{IN}. The energy accumulated in BREC,P/N during $\Phi_{Prestore}$ is later released during burst-mode operation to support rapid voltage transitions at $C_{out,P}$ or $C_{out,N}$. As a result, the pre-store mechanism effectively prepares auxiliary energy in advance, enabling faster up-tracking response without increasing peak inductor current or degrading overall efficiency.

B. Up-tracking Speed Enhancement

When the required output voltage increases rapidly, conventional boundary conduction mode (BCM) operation may not provide sufficient current to meet the desired up-tracking speed. To overcome this limitation, a burst mode is activated. As illustrated in Fig. 5 (a), taking $V_{out,P}$ as an example, switch S_9 is turned on to establish an auxiliary charging path from BREC,P to $V_{out,P}$. The pre-stored energy in BREC,P is then directly transferred to the output capacitor, enabling a rapid voltage rise without drawing large instantaneous current from V_{IN}. As a result, the burst operation avoids additional conducted EMI and remains decoupled from the normal switching behavior of the SIBO converter, thereby maintaining stable system operation.

To further enhance flexibility, the BREC is implemented using four capacitors that can be configured into multiple selectable voltage levels. If only a single capacitor were used, its voltage would quickly equalize with $V_{out,P}$ after a single burst event, limiting further tracking capability. Instead, by connecting capacitors in series to form n×$V_{BREC,P}$, the controller dynamically selects the optimal voltage level for each burst cycle. As shown in Fig. 5 (b), this multi-level selection enables fast yet controlled voltage transitions, effectively reducing overshoot, suppressing pop noise, and minimizing energy loss while maintaining high tracking accuracy.

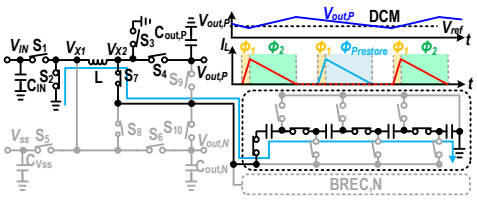
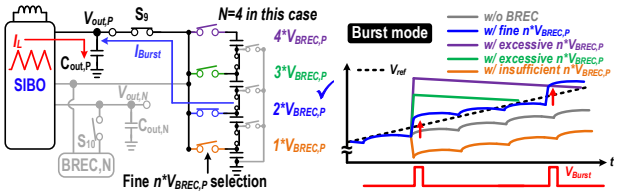


Fig. 4. Current path of charging BREC,P in $\Phi_{Prestore}$ with timing diagram.



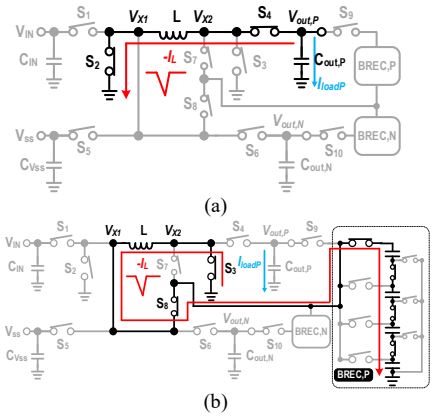
(a) (b)

Fig. 5. (a) Burst-mode operation during rapid output voltage increase. (b) Waveforms illustrating the selection of different n×$V_{BREC,P}$ levels.

C. Down-Tracking Speed Enhancement

When the output signal drops rapidly, the load current alone may be insufficient to discharge $V_{out,P}$ effectively, resulting in excess energy dissipation in the Class-AB output stage and reduced overall efficiency. To address this issue, dedicated recycle and restore phases ($\Phi_{Recycle}$ and $\Phi_{Restore}$) are introduced to manage energy flow during down-tracking, ensuring that the energy stored in the output capacitors is efficiently recovered rather than wasted. A hysteretic control scheme is adopted to precisely determine the timing of energy recycling, enabling fast response and stable operation.

When $V_{out,P}$ exceeds a predefined threshold, $\Phi_{Recycle}$ is activated. During this phase, switches S_2 and S_4 are turned on, allowing energy from $C_{out,P}$ to be transferred back to the inductor while simultaneously pulling down $V_{out,P}$, as shown in Fig. 6 (a). Once $V_{out,P}$ falls to the target level, $\Phi_{Restore}$ is initiated, as illustrated in Fig. 6 (b). In this phase, switches S_3 and S_8 are turned on to transfer the stored inductor energy into BREC,P until the inductor current I_L returns to zero. The recovered energy is then reused in subsequent burst operations to improve efficiency. A similar mechanism is applied to BREC,N, ensuring symmetric energy recycling for both supply rails.



(a) (b)

Fig. 6. (a) Current path of recycle phase $\Phi_{Recycle}$ from $C_{out,P}$ to L. (b) Current path of restore phase $\Phi_{Restore}$ from L to BERC,P.

III. Circuit Implementation

A. Pass-Gate Current Control

The BREC-based charging scheme enables efficient energy delivery to $V_{out,P/N}$ for envelope tracking, but abrupt activation of S_9 and S_{10} in Fig. 3 causes large inrush currents, leading to EMI noise and THD+N degradation. Conversely, slow switching reduces EMI but results in poor tracking and higher conduction loss, creating a trade-off between speed, EMI, and efficiency. To resolve this, a pass-gate current controller (PGCC) is proposed in Fig. 7. Each of S_9 and S_{10} uses back-to-back MOSFETs (M_{S1}, M_{S2}) to prevent energy leakage. The PGCC employs dual current paths: a fast

charging current (I_{fast}) for quick activation and a slow charging current (I_{slow}) for controlled turn-on. A sensing transistor (M_{sense}) detects when $S_{9/10}$ begin conducting and disables I_{fast}, allowing only I_{slow} to complete the transition smoothly.

B. Fully Symmetric, Supply-Independent Bias Control

During Class-H operation, the fluctuating supply voltages ($V_{out,P/N}$) make a conventional Class-AB bias sensitive to supply variations, causing channel-length modulation, I_q mismatch, degraded PSRR, and increased THD+N near zero crossing. To address this, a fully symmetric, supply-independent bias control is proposed to maintain balanced quiescent currents.

As shown in Fig. 8, two techniques are employed: (1) two individual OTAs regulate the drain voltages of M_{P1} and M_{N1} at the output common-mode level, minimizing channel-length modulation and enhancing PSRR; (2) the bias currents through M_{bN1} and M_{bP2} are stabilized at I/2 to ensure identical conduction in M_{bP} and M_{bN}, eliminating P/N imbalance. Consequently, the circuit achieves stable biasing, improved PSRR, and reduced THD+N under dynamic supply variations, compared with state-of-the-arts.

IV. Experimental Result

Fig. 9 shows the die photo of the proposed Class-H headphone amplifier, which integrates a SIBO converter with BRECs, dual stereo current DACs, positive/negative LDOs for the analog front end, a pre-amplifier, and a Class-AB output stage. The chip is fabricated in 28-nm CMOS, occupying an active area of 3400 × 1750 μm², and evaluated with a single-ended 16 Ω load.

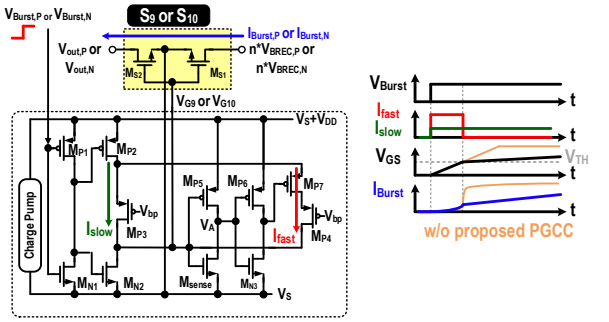


Fig. 7. Proposed PGCC, timing diagram, and the reduced high-frequency EMI.

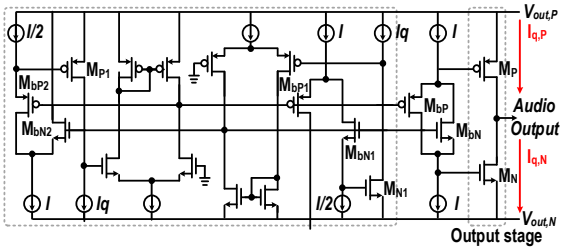


Fig. 8. Class-AB output driver with fully symmetric, supply-independent bias current control.

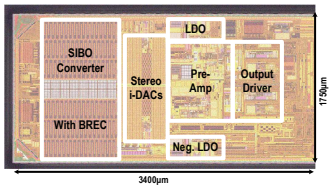


Fig. 9. Chip micrograph of proposed Class-H headphone amplifier.

As shown in Fig. 10, the total-path efficiency was measured across various output power levels using a 1 kHz sinusoidal input. The proposed amplifier achieves substantially higher efficiency than prior designs across both light- and heavy-load conditions. At 10 mW output, efficiency improves from 48% to 61% compared to [1], and reaches 81% at the maximum 62-mW output, demonstrating excellent energy utilization over the entire power range.

Fig. 11 shows the transient waveforms of $V_{out,P}$ and $V_{out,N}$ under 20-kHz and 62-mW output conditions. In Fig. 11(a), without the proposed BREC-based energy recycling, the supply rails fail to track the audio envelope precisely, leading to additional power loss. By contrast, with BREC operation enabled, as shown in Fig. 11 (b), $V_{out,P}$ and $V_{out,N}$ accurately follow the audio envelope even under high-frequency, high-power operation. This precise tracking minimizes the power consumption of the Class-AB output stage, resulting in a measurable improvement in overall efficiency.

Fig. 12 illustrates the supply power across different audio output signal frequencies. With the proposed energy-recycling mechanism, the supply power at a 62-mW output and 20-kHz frequency is reduced from 93 mW to 86 mW, achieving an 8% reduction. This improvement arises because the energy-recycling mechanism captures and reuses the excess energy that would otherwise be dissipated in the Class-AB output stage during burst-mode operation. As a result, the power drawn from V_{IN} is reduced, leading to enhanced overall efficiency.

Fig. 13 demonstrates that, with the proposed PGCC, accurate and fast envelope tracking is sustained even under a 62-mW, 20-kHz operating condition. Meanwhile, the EMI levels of both V_{IN} and $V_{out,P}$ remain below 60 dBμV. These results confirm that the PGCC effectively suppresses high-frequency EMI, thereby minimizing interference with surrounding circuits and preventing degradation of THD+N performance in the audio output.

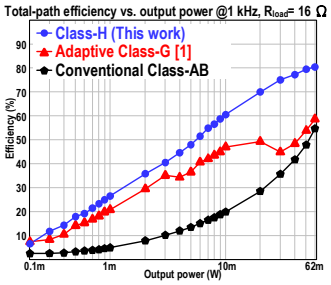
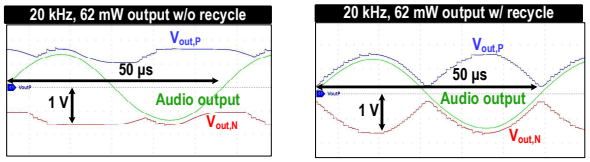


Fig. 10. Total-path efficiency versus output power level.



(a) (b)

Fig. 11 (a) Transient waveforms without energy recycle mechanism (b) Transient waveforms with energy recycle mechanism.

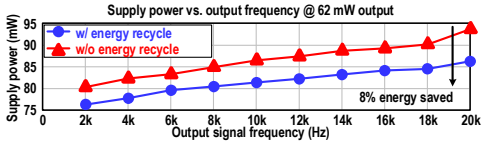
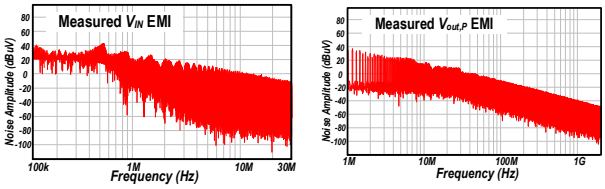


Fig. 12. Supply power verse output signal frequency at 62mW output.



(a) (b)

Fig. 13. Measured EMI under heavy load, high frequency audio output at (a) 1.8V V_{IN}. (b) $V_{out,P}$ of the SIBO converter.

Fig. 14 shows that, with the proposed fully symmetric and supply-independent bias control, the quiescent current is maintained at approximately 1.3 mA, with less than 1% variation over a supply range from ±0.3 V to ±1.8 V. This balanced biasing ensures tight matching between $I_{q,P}$ and $I_{q,N}$, effectively suppressing supply-induced noise and reducing crossover distortion, thereby improving THD+N and overall linearity. The measured THD+N achieves its best performance at an output power of 62 mW with a 1-kHz input, reaching –112 dBc, as shown in Fig. 15(a). This result validates the effectiveness of the proposed bias control in minimizing distortion and preserving high linearity. At a higher output frequency of 20 kHz, however, the more aggressive BREC-based tracking in the SIBO converter introduces additional supply ripple to the Class-AB output stage. As a result, the THD+N slightly degrades to –109 dBc, as illustrated in Fig. 15(b).

Table I summarizes the performance comparison with prior works. Among the reported designs, only the proposed Class-H audio amplifier achieves accurate envelope tracking up to 20 kHz without incurring additional EMI. Compared with [1], the use of Class-H operation enables the proposed design to deliver the same output power while significantly reducing supply power consumption. Moreover, by employing supply-independent bias current control, the proposed amplifier attains improved THD+N performance, achieving a 2.4× enhancement in linearity FoM compared to [4].

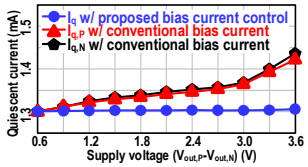


Fig. 14. Variation of the quiescent current with proposed bias current control under supply voltage changes from ±0.3 V to ±1.8 V.

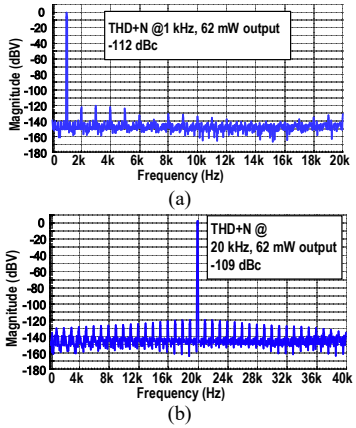


Fig. 15. Audio output signal FFT spectra at (a) 1-kHz, 62-mW output, (b) 20-kHz, 62-mW output.

V. Conclusions

The proposed Class-H headphone amplifier effectively overcomes the limitations of conventional SIBO-based designs by enhancing tracking bandwidth, reducing distortion, and improving efficiency. Through the integration of BREC for fast tracking and energy recycling, PGCC for EMI suppression, and SSBC for bias stabilization, the design achieves a 20 kHz tracking bandwidth with −112 dBc THD+N and 21% lower power consumption. These results demonstrate a well-balanced solution for high-efficiency, low-distortion audio amplification in portable applications.

TABLE I. Performance Summary

	This work	JSSC' 16 [1]	ISSCC' 24 [4]
Supply (V)	1.8	1.8	1.8
PMU topology	SIBO with BREC	Multi-mode Charge pump	SIBO
Type	Class-H	Class-G	Class-H
Output type	SE	SE	SE
Load (Ω)	16	16	16
Peak output power (mW)	62	62	62
Tracking bandwidth (Hz)	20k	-	3k
@ Lowest THD+N, 1 kHz			
Output voltage (V_{pp})	2.82	1.13	2.82
Output power (mW)	62	10	62
THD+N / THD (dBc)	-112/-115	-95/-	-108/-112
Power consumption @1 kHz output (mW) (Driver only, per channel)	(*2)	(*1)	
@ 0 W output power	0.82	1.23	2.3
@ 0.1 mW output power	1.1	1.42	3.7
@ 1 mW output power	32.8	4.54	7.3
@ 10 mW output power	16.4	20.9	28.7
*4FoM(THD)	259124	22349	107316

*1The power consumption in [1] and [2] are estimated from the efficiency plots.
*2The quiescent current of the class AB output stage and the decoder and controller are 1.3 mA @ 1.8 V/channel and 2.5 mA @ 1.8 V/channel, respectively.
*4FoM (THD)=$P_{out,max}$/[Quiescent power*THD (%)]

Acknowledgement

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References

[1] S.-H. Wen *et al.*, "A Load-Adaptive Class-G Headphone Amplifier With Supply-Rejection Bandwidth Enhancement Technique," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2241–2251, Oct. 2016.

[2] Maxim Integrated, *Low-Power, Low-Offset, Dual Mode, Class-H DirectDrive Headphone Amplifier*, Rev. 3, Aug. 21, 2012. [Online]. Available:https://www.analog.com/media/en/technical-documentation/data-sheets/MAX97200.pdf

[3] S. Galal *et al.*, "A 60 mW Class-G Stereo Headphone Driver for Portable Battery-Powered Devices," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 8, pp. 1921–1934, Aug. 2012.

[4] S.-H. Wen *et al.*, "A −108 dBc THD+N, 2.3 mW Class-H Headphone Amplifier With Power-Aware SIMO Supply Modulator," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, pp. 384–386, Feb. 2024.

[5] S. Chaput, D. Brooks, and G.-Y. Wei, "A 3-to-5 V input, 100 Vpp output, 57.7 mW, 0.42% THD+N highly integrated piezoelectric actuator driver," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, pp. 360–361, Feb. 2017.

[6] J.-S. Bang *et al.*, "A 2-Tx digital envelope-tracking supply modulator achieving 200-MHz channel bandwidth and 93.6% efficiency for 2G/3G/LTE/NR RF power amplifiers," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, pp. 236–237, Feb. 2022.