An SFDR-Enhanced Cryo-CMOS Interface ASIC for FDM-based Qubit Control and Readout

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***Abstract*—A frequency-division multiplexing (FDM)-based qubit interface ASIC requires a high spurious-free dynamic range (SFDR) RF-front end (FE) to enable multi-qubit control and readout while preventing spectral leakage between adjacent channels. This work presents a 28 nm cryo-CMOS RF-FE ASIC featuring three key innovations for SFDR enhancement: (i) A dual-amplifier intermodulation cancellation (DAIC) TX driver that co-optimizes the DC operating point and gain ratio to suppress IM3 and IM5 concurrently; (ii) a fully differential inverter-based RF amplifier employing a feed-forward cross-coupling path to enhance the common-mode and power-supply rejection ratios; and (iii) a vector-combination co-tuning calibration scheme for optimizing the local-oscillator and image rejection ratios (LORR/IMRR). Measured at 3.5 K, the receiver FE delivers a 74.3 dB peak gain and an 84 K noise temperature over 6.2–8.4 GHz, consuming 2 mW/qubit. The Transmitter FE achieves >57 dB SFDR with 62 dBc IM3, 61 dBc IM5, and 57/58 dB LORR/IMRR at 1.4 mW/ qubit, outperforming prior state-of-the-art designs by 13 dB in SFDR.**

Keywords—cryogenic CMOS, quantum computing, distortion cancellation, feed-forward cross-coupling, enhanced SFDR.

I. Introduction

The rapid advancement of cryogenic electronic interfaces is paramount for realizing fully integrated, high-fidelity, and scalable solid-state quantum computing architectures. To mitigate interconnect complexity and per-qubit power consumption, FDM has emerged as a promising technique that exploits its inherent spectral efficiency for multi-qubit control and readout [1], [2], [3], [4]. The FDM-based qubit interface generates multi-tone driving and readout pulses to manipulate and measure multiple qubit states simultaneously.

However, FDM-based multi-tone signals inherently exhibit a high peak-to-average power ratio, inducing severe intermodulation (IM) distortion. Specifically, third-order (IM3) and fifth-order (IM5) intermodulation products may leak into adjacent channels, causing spurious excitation of unaddressed qubits and severely degrading gate fidelity. Since a stringent 99.999% single-qubit gate fidelity mandates an SFDR exceeding 54 dB [5], [6], suppressing these distortions is critical. Furthermore, LO feedthrough and image sidebands are critical impairments that must be suppressed to maintain signal integrity [7], [8]. While prior works have primarily focused on mitigating IM3 distortion [1], [4], [9], IM5 has also become a bottleneck for FDM-based systems. Along the amplification path, pseudo-differential inverter-based RF amplifiers are widely utilized in cryo-CMOS qubit interface circuits for their power efficiency and high linearity at low temperature [2], [3], [10], [11]. They are highly susceptible to supply and common-mode perturbations, which inject undesirable power-ripple sidebands and crosstalk noise into susceptible quantum control signals.

Consequently, realizing a robust multi-tone cryo-CMOS RF-FE demands co-optimization of IM3/IM5 distortions, power-supply rejection ratio/common-mode rejection ratio (PSRR/CMRR), and LORR/IMRR. To address these bottlenecks, this work presents a novel SFDR-enhanced RF-FE featuring three key innovations: (i) A DAIC TX-driver with co-optimization of bias operating points and gain ratios to suppress IM3 and IM5 distortions. (ii) A fully-differential RF amplifier that integrates a feed-forward cross-coupling path to concurrently boost CMRR and PSRR. (iii) A vector-combination calibration technique within the TX mixer to improve both LORR and IMRR. Ultimately, the proposed RF-FE ASIC achieves an IM3/IM5 suppression of 62/61 dBc, alongside 57 dB LORR and 58 dB IMRR. These results demonstrate a 13 dB improvement in overall SFDR compared to prior art, paving the way for next-generation high-fidelity quantum computation.

II. Architecture and Circuit Implementation

Fig. 1 shows the architecture of the proposed SFDR-enhanced RF-FE ASIC for FDM-based multi-qubit control and readout. In the transmitter (TX) path, a 10-800 MHz multi-tone low-intermediate-frequency baseband signal is filtered, up-converted by the LPF and TX mixer, amplified by a two-stage RF amplifier, and driven to the qubits by a TX driver. Conversely, in the receiver (RX) path, the reflected signal is pre-amplified by a low-noise amplifier (LNA) and cascaded RF amplifiers, down-converted by an RX mixer, post-amplified and filtered by an analog baseband (ABB) circuit, and subsequently processed for qubit state-readout. The system supports three operational modes: XY-control mode (S1 on), readout mode (S2 and S3 on), and loop-back calibration mode (S2 and S4 on).

Crucially, to systematically enhance SFDR, the architecture targets specific bottlenecks along the signal chain: At the up-conversion source, the TX mixer employs a vector-combination calibration scheme to optimize LORR and IMRR. Subsequently, to shield the high-gain path from environmental noise, the RF amplifier implements a feed-forward cross-coupling topology to boost CMRR and PSRR, thereby preventing noise-induced degradation. Finally, handling the maximum signal swing, the TX driver integrates the DAIC technique to suppress IM3/5 distortions, resolving the ultimate linearity bottleneck.

A. Proposed DAIC-based IM3/IM5 Cancellation

Conventional IM-cancellation techniques typically focus solely on IM3, leaving IM5 as a bottleneck for SFDR. As depicted in Fig. 2(a), the conventional technique implements a dual-amplifier architecture, where the main amplifier operates in class-AB for high output power, while the auxiliary path operates in class-C to generate specific nonlinear components.

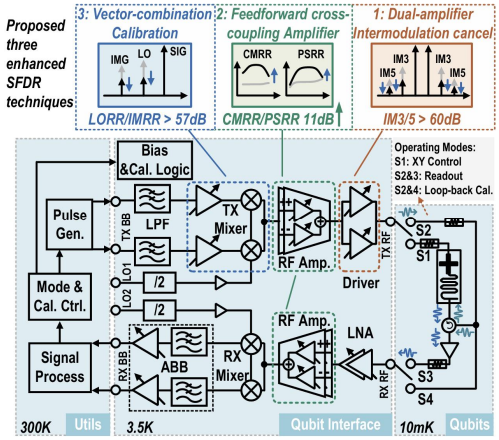

Fig. 1. Architecture of the proposed qubit interface RF-FE, featuring three SFDR enhancement techniques.

The conventional IM-cancellation technique eliminates IM3 by tuning the auxiliary amplifier's operating point to generate a third-order transconductance (g_{m3}) term that opposes that of the main amplifier. However, optimizing for IM3 cancellation often leads to suboptimal IM5 and compromises overall linearity.

To address this deficiency, this work proposes a novel DAIC-based technique that enables the concurrent cancellation of IM3 and IM5. As shown in Fig. 2(b), the DAIC-based TX driver comprises two cascode amplifiers constructed from multiple unit cells, with their outputs combined via an output transformer. The two primary cancellation mechanisms are presented in Fig. 3: (i) IM5 is suppressed by tuning the bias voltages V_{G_AB} (main amplifier) and V_{G_C} (auxiliary amplifier) to their respective g_{m5} zero-crossing points. This eliminates the fifth-order nonlinearity contributions from both paths. (ii) IM3 is canceled by optimizing the gain ratio (N_1/N_2) between the auxiliary and main amplifier paths to counteract the combined g_{m3} terms, thus achieving concurrent IM3/IM5 suppression.

B. Proposed Cross-coupling Amplifiers

As shown in Fig. 4(a), inverter-based pseudo-differential RF amplifiers are widely utilized in cryo-CMOS circuits due to their power efficiency and high linearity. However, this topology is inherently sensitive to supply and common-mode noise. Even minor supply perturbations or common-mode crosstalk can severely degrade the overall SFDR. Furthermore, cascading multiple stages leads to unintended feedback loops through the shared power supply, potentially causing instability or oscillation. Fig. 4(b) shows the topology of the proposed RF amplifiers. The key innovation is a specially designed feed-forward cross-coupling path. The path senses the input common-mode interference and supply noise from the main signal path, generating corresponding compensation signals with opposite polarity. This technique reinforces the differential signal while providing inverse responses for common-mode and supply noise. Crucially, this enhancement incurs only a modest power overhead, as the components in the feed-forward cross-coupling path can be minimally sized.

As shown in Fig. 5, simulated results display that while the conventional design exhibits CMRR and PSRR near 0 dB, the proposed RF amplifier achieves improvements of up to 18 dB in CMRR and 11 dB in PSRR.

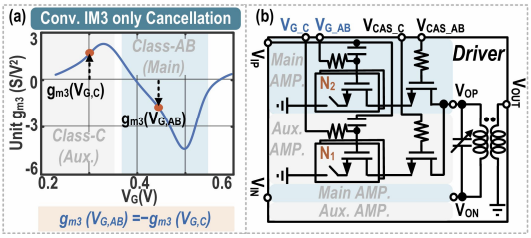

Fig. 2. (a) Conventional IM3-only cancellation. (b) TX driver with the proposed DAIC technique.

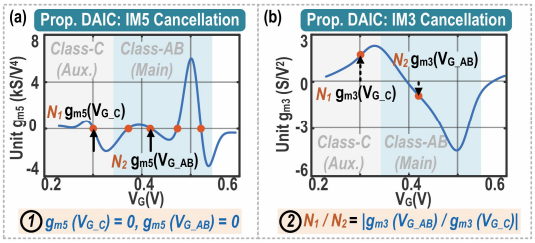

Fig. 3. Proposed DAIC-based cancellation mechanisms: (a) IM5 cancellation by zero g_{m5} biasing. (b) IM3 cancellation by gain-ratio tuning.

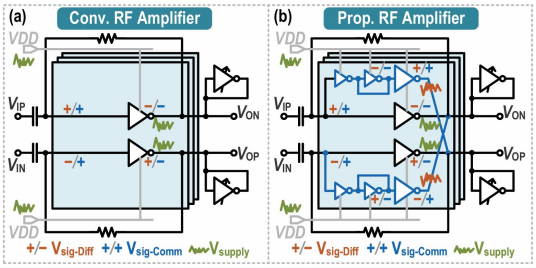

Fig. 4. Inverter-based RF Amplifier Topologies: (a) Conventional pseudo-differential design. (b) Proposed fully-differential design with cross-coupling path.

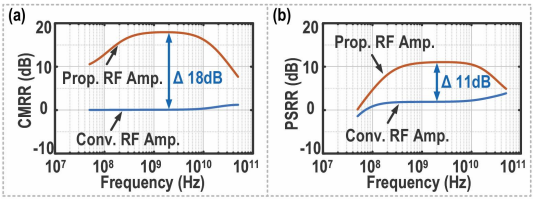

Fig. 5. Simulated results of (a) CMRR and (b) PSRR for the conventional and proposed amplifiers.

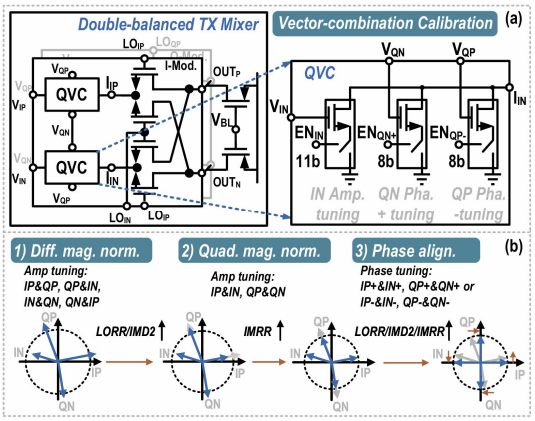

Fig. 6. (a) Double-balanced TX mixer with quadrature vector combiners (QVCs). (b) Three-step calibration scheme based on vector combination.

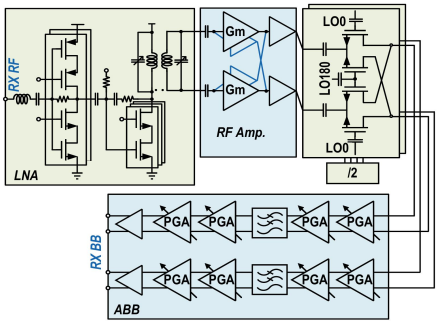

Fig. 7. Architecture of the readout receiver.

C. Vector Combination Calibration of LORR/IMRR

In a double-balanced mixer, insufficient LO feedthrough or image sideband rejection can severely constrain the SFDR. Fig. 6(a) illustrates the proposed TX mixer integrated with four quadrature-vector combiners (QVCs). Each QVC utilizes three programmable transconductance branches that weight and sum baseband voltages for I/Q amplitude and phase corrections. For example, a single QVC integrates an 11-bit primary branch for input amplification and magnitude adjustment, along with two 8-bit quadrature branches that enable fine phase tuning. Fig. 6(b) depicts the three-step calibration scheme based on vector combination: 1) Differential magnitude normalization minimizes differential magnitude mismatches to reduce LO leakage. 2) Quadrature magnitude normalization equalizes the quadrature amplitude to enhance IMRR. 3) Phase alignment cancels quadrature phase errors to improve LORR and IMRR.

Fig. 7 presents the architecture of the readout receiver, comprising a two-stage LNA of an inverter-based amplifier and a cascode amplifier with a transformer load, an RF amplifier with feed-forward cross-coupling path, an RX mixer, and an ABB. The ABB integrates a four-stage PGA offering 0-40 dB gain and a 10-800 MHz LPF.

III. Measurement Results

The qubit interface RF-FE ASIC is fabricated in a 28 nm bulk CMOS technology and characterized at 3.5 K inside a dilution refrigerator. The chip micrography and cryogenic measurement setup are shown in Fig. 8. Fig. 9 illustrates the detailed measurement setups for the three operating modes: XY control, state readout, and loop-back calibration.

Fig. 10(a) presents the single-tone TX output spectrum at 5.535 GHz, where a 35 MHz IF is up-converted by a 5.5 GHz LO. After two rounds of calibration, both LORR and IMRR exceed 60 dB, yielding an SFDR of >57 dB across a 250 MHz span. In Fig. 10(b), the two-tone spectrum at 4880/4881 MHz demonstrates that the DAIC technique achieves a -19 dBm output power while achieving 64 and 63 dB suppression for IM3 and IM5, respectively. Over the output power range of -27 to -16 dBm, the average IM3 and IM5 suppressions are improved by 35 dB and 7 dB, respectively, as shown in Fig. 10(c)- (d). Frequency-swept measurements from 1.5 to 9 GHz (Fig. 11(a)-(b)) show average IM3 and IM5 suppressions of 55 dB and 58 dB, confirming the significant SFDR enhancement provided by the DAIC. Furthermore, measurements across five chips (Fig. 11(c)-(d)) show average LORR and IMRR values of 61 dB and 62 dB, representing improvements of 41 dB and 40 dB over uncalibrated baselines.

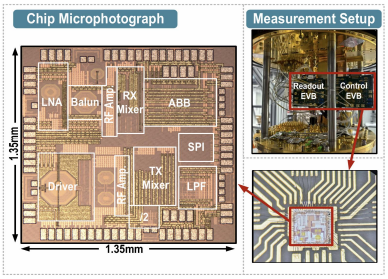

Fig. 8. Chip micrograph and measurement setup.

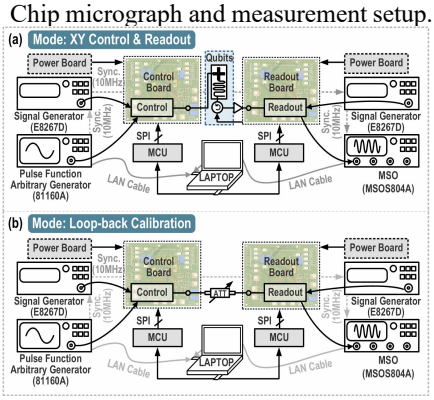

Fig. 9. Detailed Measurements setup for (a) XY control and state-readout, and (b) loop-back calibration.

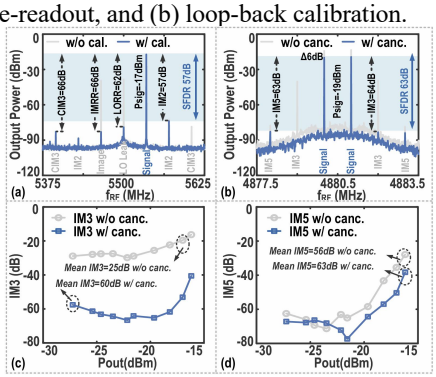

Fig. 10. Measured results of (a) the single-tone output spectrum, (b) the two-tone output spectrum. (c) IM3, and (d) IM5 versus output power.

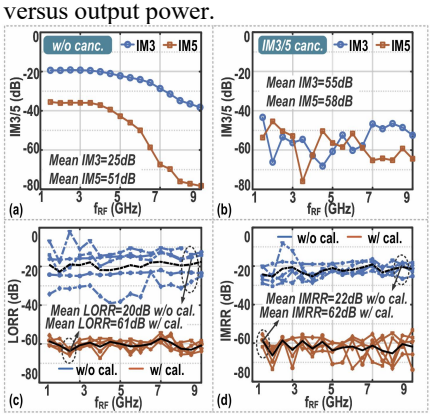

Fig. 11. Measured IM3 and IM5 versus frequency (a) without and (b) with the proposed DAIC technique. (c) Calibrated LORR and (d) IMRR across five chips.

The readout receiver's performance is characterized in Fig. 12(a) -(c). It achieves a peak conversion gain of 74.3 dB and a minimum noise temperature of 84 K over 6.2-8.4 GHz. Linearity measurements indicate an IP1dB of -70 dBm and an IIP3 of -66 dBm at 7.5 GHz. Fig. 12(d) provides the power breakdown with a power consumption of 80.3 mW.

TABLE I. Comparison with state-of-the-art designs

Specification		This Work	ISSCC'24[11]	ISSCC'22[4]	ISSSC'22[6]	ISSCC'21[2]	ISSCC'21[8]	ISSCC'21[3]	ISSCC'20[1]
Qubit Type		Transmon	Transmon	Transmon	Transmon	Spin Qubit	Transmon	Spin	Transmon& Spin Qubit
Test Temp.(K)		3.5	3.5	3.5	3	4	3.5	4.2	3
Technology		28nm Bulk	28nm Bulk	40nm Bulk	14nm FinFET	22nm FinFET	40nm Bulk	40nm Bulk	22nm FinFET
TX Freq. Band(GHz)		1-6	4-6	4.5-8	4.5-5.5	11-17	N/A	N/A	2-20
TX IM3/5 Cancellation		Yes	No	No	No	No	N/A	N/A	No
TX IM3/5(dB) @Power		62/61 @-21dBm	N/A	52[c]/- @-22dBm	N/A	50/- @-17dBm	N/A	N/A	50/- @-18dBm
LORR/IMRR/IM2 Calibration		Yes	Yes	No	Yes	No	N/A	N/A	No
LORR/IMRR/IM2/CIM3 (dB) @Power		57/58/57/69 @-18dBm	43/44/-/- @-28dBm	37/42/-/- @-22dBm[d]	60/48/50/40 @-18dBm[d]	N/A	N/A	N/A	36/45/45/- @-18dBm
SNR @25MHz BW.(dB)		52	50[c]	N/A	N/A	50	N/A	N/A	48
IF Bandwidth(MHz)		736	1400	400	300	2000	1400	2000	1000
RX Freq. Band(GHz)		6.2-8.4	5.4-6.8	5-7.25	N/A	0.2-0.6	5-6.5	6-8	N/A
RX Bandwidth(GHz)		2.2	1.4	2.25	N/A	0.4	1.5	2	N/A
RX Gain(dB)		74.3	65	47	N/A	40~90	70	58	N/A
[a]Min. Noise Temp.		85	129.2	83.6	N/A	43	39.2	43	N/A
RX IIP3(dBm)		-66	-65	-35	N/A	-69	-72	-50.8	N/A
Area(mm^2)		1.8	4.6	6.96	1.61	16	2.8	0.68	4
Power/qubit (mW)[b]	Control TX	1.4	4.3	0.49	23	5.2	N/A	N/A	N/A
	Readout RX	2	5.5	20	N/A	9.3	1.5	1	1.7

[a] Referred at 290K, [b]#Channels = IF BW./30MHz, [c] SNR normalized from 50MHz to 25MHz, [d] Estimated from the figures.

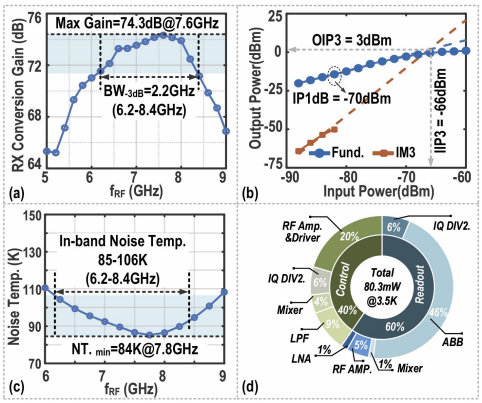

Fig. 12. Measured (a) conversion gain, (b) linearity (IP1dB and IIP3). (c) Simulated noise temperature. (d) Measured power breakdown of the qubit interface ASIC.

Table I compares this work with state-of-the-art interface ASICs, highlighting 13 dB SFDR improvement.

IV. Conclusion

This work presents a 3.5 K RF-FE interface ASIC for FDM-based multi-qubit control and readout. To maximize linearity and wideband spectral purity, the architecture integrates three core innovations: a DAIC-based driver for simultaneous IM3/IM5 cancellation, an RF amplifier with dedicated feed-forward cross-coupling paths for CMRR/PSRR enhancement, and a vector-combination calibration scheme for LORR/IMRR optimization. Targeting 25 qubits, the TX-FE achieves 62 dBc IM3, 61 dBc IM5, 57 dB LORR, and 58 dB IMRR while consuming just 1.4 mW/qubit. The RX-FE delivers 74.3 dB peak conversion gain and a 2.2 GHz bandwidth while consuming 2 mW/qubit, establishing a robust foundation for scalable, high-fidelity qubit interfaces.

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