Fully Integrated In-Situ PTAT-Based Junction Temperature Sensing for GaN Gate-Injection Transistors in 180 nm CMOS

Jan Grobe, Erik Wehr, Tom Herzog, Ralf Wunderlich and Stefan Heinen
Integrated Analog Circuits and RF Systems, RWTH Aachen University
Aachen, Germany
mailbox@ias.rwth-aachen.de

***Abstract*—An integrated junction temperature monitor in an active gate drivers for GaN gate-injection transistors (GITs) is presented. The circuit implements a PTAT voltage generator by reusing the hold current required for driving GITs while preserving the original device performance. The extracted temperature-sensitive electrical parameter is based on robust, well-established mechanisms used in bandgap references and CMOS temperature sensors. The implemented concept does not require additional external components and operates with commercially available transistors. Differential mirrored sampling allows for rejection of constant and linearly changing drain currents, reducing the drain current influence by 93 %. The gate driver was fabricated in a 180 nm CMOS SOI technology and achieves a resolution of 260 mK over a −25° to 150° temperature range and requires an area of 0.068 mm².**

***Index Terms*—junction temperature, wide-bandgap, GaN, gate-injection transistor (GIT), temperature-sensitive electrical parameter (TSEP), active gate driver (AGD)**

I. Introduction

Device health monitoring plays a significant role in sustainable and cost-effective operation of power converters [1]. Tracking key parameters for health monitoring such as $R_{ds,on}$ or V_{th}, however requires knowledge of the devices junction temperature to compensate temperature-dependent effects. Furthermore, estimating the remaining device lifetime reduces the need for premature replacement in which temperature is also a key factor. Another application area of junction temperature monitoring is the optimization of switching transitions using active gate driving. An active gate driver (AGD) can influence the turn-on and turn-off behavior of the power transistor by actively controlling the gate current [2, 3]. The main optimization goal of the AGD is to reduce drain-voltage overshoot and EMI. To constrain the optimization by keeping the device losses minimal while reducing EMI, the junction temperature can be used as an indicator for the losses of the power device.

Different temperature-sensitive electrical parameters (TSEPs) have been evaluated for temperature monitoring in power devices [4]. Usage of the on-state resistance has been proposed, but proves difficult for GaN HEMTs due to their voltage-dependent dynamic $R_{ds,on}$ and requires high-voltage evaluation circuitry [5]. The threshold voltage has a significant temperature dependence, but is not easily measurable when fast turn-on or turn-off transients are desired and typically has high process variation [6]. Another method uses the internal gate resistance as a TSEP. In [7], the resistance is measured in the off state while the gate is excited at its resonant frequency. This method, however, faces challenges with the high resonant frequency of GaN devices. For Schottky-gate transistors, the gate leakage is often used as a TSEP [8]. This parameter however typically underlies significant process variation. Using the gate characteristic of GaN gate-injection transistors (GITs) as a TSEP has been proposed in [9], in which the gate current is measured at a fixed voltage. However, most of these approaches either require extensive calibration or additional discrete evaluation circuitry. In this work, a fully integrated online junction temperature measurement for GaN GITs is presented, which uses a PTAT voltage generated from the gate voltage using a modulated gate current as a TSEP.

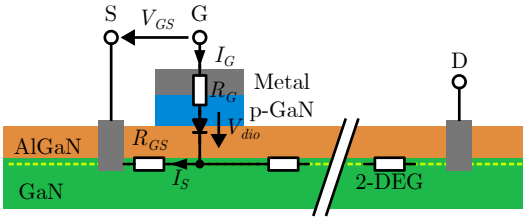

Fig. 1. Internal construction of gate-injection transistors.

GaN power transistors are primarily implemented using two gate configurations: Schottky-gate and gate-injection transistors. Schottky-gate transistors offer a virtually isolated gate which can be driven like a standard MOSFET. GITs feature an ohmic contact instead of a Schottky type as shown in Fig. 1. While turn-on and turn-off of these devices are similar to other insulating gate transistors, the on-state requires a gate current to achieve a sufficient gate-source voltage and thus on-resistance. In discrete designs with conventional gate-drivers, this is typically achieved by a combination of resistors and a capacitor in the drive path [10]. This gate diode characteristic is exploited in this work to sense the device's junction temperature.

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II. Temperature Sensing Concept

Temperature sensors based on p-n junctions generally use the diode forward voltage, which is complementary to the absolute temperature (CTAT) or the difference of two diode voltages with different current densities which is proportional to the absolute temperature (PTAT) [11].

The gate-source voltage V_{GS} of a GIT device containing a p-n junction can be approximated for moderate forward bias currents by the following equation:

$$V_{GS} \approx \underbrace{n\frac{kT}{q}\ln\frac{I_G}{I_{sat}}}_{V_{dio}} + \underbrace{(I_D+I_G)R_{GS}+I_G R_G}_{V_{err}}. \quad (1)$$

Where n is the diode ideality-factor, I_G the gate current, I_{sat} the diode saturation current, I_D the GIT's drain current, R_G the internal gate resistance and R_{GS} the gate to source channel resistance.

Due to the connection of the gate to the channel as seen in Fig. 1, the gate-source voltage is offset by the voltage drop over the channel resistance R_{GS} between gate and source. Furthermore, the internal gate resistance R_G adds another error term. This is the main reason why evaluation of a single measurement sample of the gate voltage is insufficient. To overcome the error generated by a constant drain current, the gate voltage is sampled differentially at two points with different gate currents I_{hold} and I_{mod}:

$$\Delta V_{GS} = \underbrace{n\frac{kT}{q}\ln m}_{\Delta V_{Dio}} + \underbrace{I_{hold}(1-\frac{1}{m})(R_G+R_{GS})}_{\Delta V_{err}} \quad (2)$$

with the modulation factor

$$m = \frac{I_{hold}}{I_{mod}}. \quad (3)$$

The resulting ΔV_{GS} exhibits PTAT behavior. This eliminates the process parameter I_{sat} and reduces the influence of the absolute drive current I_{hold}, which would have to be trimmed otherwise.

Since the sampling points for I_{hold} and I_{mod} are separated in time, a change of drain current during this interval introduces an error V_{err} dependent on the drain current change during the sampling interval as shown in Fig. 2. A linear change of current over time is the most common case, since it is generated by a constant voltage across an inductance which is present in buck converters, boost converters and various other switching converter topologies. By using a time-mirrored differential sampling approach, constant and linearly varying drain currents can be fully compensated for. This is achieved by mirroring the sample points t_{p1} and t_{n1} around t_{mid}, resulting in t_{p2} and t_{n2}. The respective positive and negative samples are then averaged.

The temporary reduction of drive current introduced during the modulation interval is tolerable with GITs, because their on-resistance changes little with gate current. For the used GIT, a modulation from 3 mA to 0.96 mA increases the $R_{ds,on}$ by approximately 2.4 % [6].

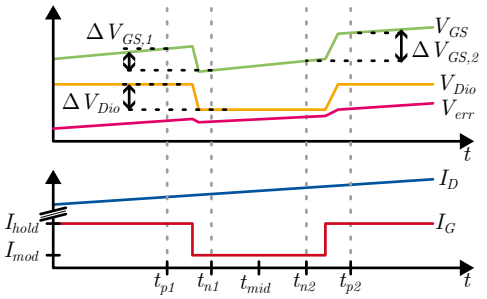

Fig. 2. Visualization of sampling and error sources.

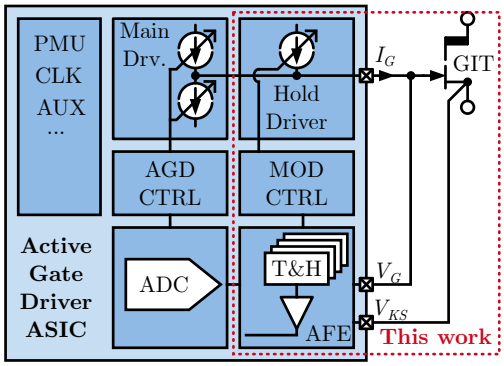

Fig. 3. Block diagram of the AGD with temperature sensing.

III. System Overview and Circuit Implementation

The proposed circuit is implemented as part of a digital AGD ASIC manufactured in a 180 nm HV CMOS SOI technology. A simplified block diagram is presented in Fig. 3. Integrating the temperature monitor into the gate driver saves silicon area by reusing existing architecture. The AGD uses adjustable current sources in its main driver stage to actively control the power transistor's gate-source voltage during the turn-on and turn-off transitions. The driver stage is programmable in 150 ps and 32 mA steps. After the transistor is turned on, the main driver is disabled, since a high continuous current would damage the gate and not yield any further $R_{DS,on}$ improvement. The implemented burst sampling ADC is primarily used to measure the gate and drain waveform and adjust the driving current pattern accordingly. It features an ADC core with 1.4 mV LSB resolution, which is used to digitize the generated PTAT voltage.

This work implements the hold current driver and an Analog-Front-End (AFE). The hold driver generates the required current to drive the GIT during the on-state and enables modulation of the current to implement temperature sensing. The AFE samples and amplifies the gate voltage before it is digitized by the ADC.

A. Analog Front End

An overview of the AFE is presented in Fig. 4. The four sampling steps are implemented using four track-and-hold elements using C_{p1} - C_{n2}. The sampling NMOS switches M1 - M4 are closed initially and opened at the corresponding

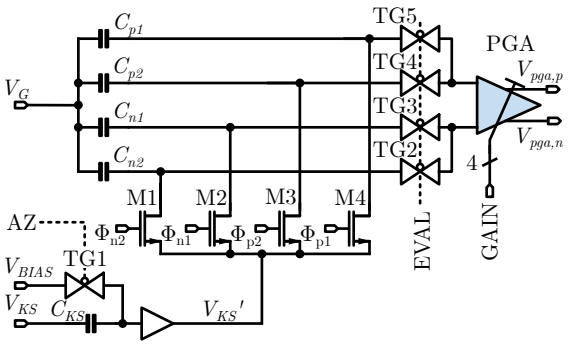

Fig. 4. Schematic of the AFE.

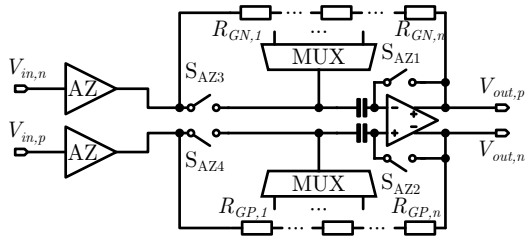

Fig. 5. Schematic of PGA.

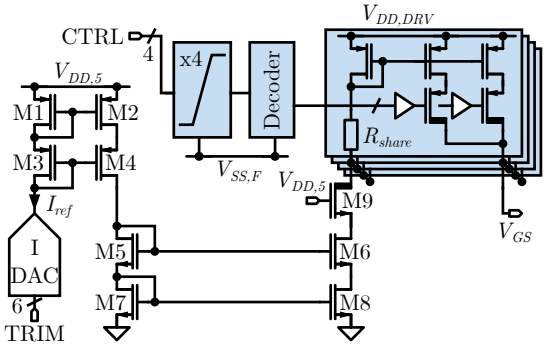

Fig. 6. Schematic of the modulating hold driver.

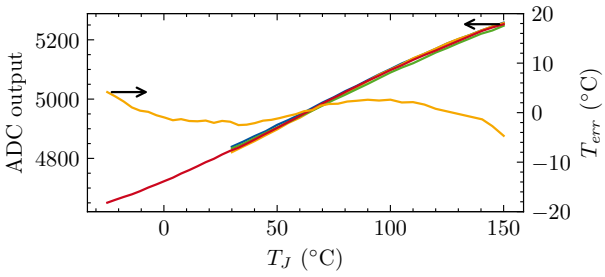

Fig. 7. ADC output of the temperature sweep with four DUT samples.

sampling points. In the track phase, the sampling switches charge the capacitors to $V_G - V_{KS}'$. V_{KS}' is generated by sampling V_{BIAS} and AC-coupling the Kelvin source voltage onto it. This ensures a defined mid-range common-mode voltage at the input of the PGA and enables differential sampling of V_{GS}. After all four sampling switches are opened, the positive and negative samples are averaged via the EVAL signal controlling transmission gates TG2 - TG5.

To maximize the usable ADC resolution, a programmable gain amplifier (PGA) is implemented as presented in Fig. 5. The PGA core is implemented using a fully-differential two-stage miller compensated operational amplifier with switchable compensation and resistive feedback. The differential inputs of the op-amp can be connected to different taps of two resistor ladders R_{GN} and R_{GP} using a mux, setting the gain from 1 to 15 in 16 steps. To reduce offset and low-frequency noise of the PGA, auto-zeroing is performed by closing S_{AZ1} - S_{AZ4}. This also sets an appropriate input common-mode range for the op-amp. Since the PGA core has a significant input current, two auto-zero buffers are employed, which are implemented as two-stage Miller compensated operational amplifiers using conventional auto-zeroing.

B. Hold Current Driver

The hold current driver's primary function is to supply the GIT gate with a small current during the on-phase. By integrating the capability to modulate the gate driver current, only switches for the segmented output stage have to implemented. Its schematic is presented in Fig. 6. To accommodate GITs of different sizes, the driver uses a 6-bit current DAC for its reference current I_{ref}, which results in an output current range from 0.9 mA to 55 mA with 875 µA resolution. The reference current is scaled by three current mirrors by a total factor of 9216. The final stage operates with a variable supply voltage $V_{DD,DRV}$ of up to 20 V and requires a floating reference supply $V_{SS,F}$ to drive the final output transistors. The output stage is split into four drivers with two switchable current sources each. By individually switching the DMOS output switches, which are controlled through level shifters, the output current is adjustable from $\frac{0}{8}$ to $\frac{8}{8}$ in $\frac{1}{8}$ steps.

Since the temperature measuring concept relies on the ratio of two currents, only relative accuracy between modulation steps is required. To ensure good current matching of the four output stages, current sharing resistors R_{share} are employed for each stage. Monte Carlo simulations show a 3-σ ratio error of 0.41 % between full and minimal $\frac{1}{8}$ current setting.

IV. Measurements

The system is characterized using a commercially available GIT transistor (Infineon IGLD60R190D1 [6]) as the DUT. The DUT's temperature is controlled via a thermoelectric temperature controller, while the temperature is measured at the top of the case with added thermal insulation to reduce heat flux through the transistor molding, which would introduce measurement errors.

The ADC output over a temperature range of −25 °C to 150 °C is shown in Fig. 7. The circuit shows a mean resolution of 260 mK per LSB over the specified range. To quantify the non-linearity, the difference T_{err} between the measured data and a linear fit is plotted. The shown non-linearity can be explained by the non-ideality of the diode not covered by Eq. (1). The measurement was repeated for four different

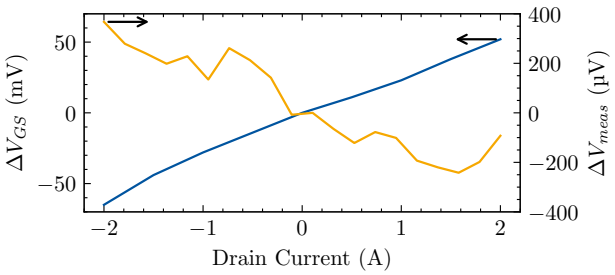

Fig. 8. Drain current rejection measurement.

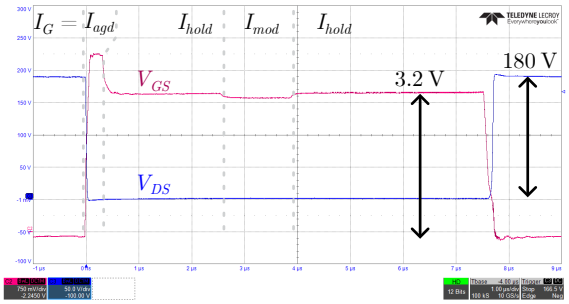

Fig. 9. Online junction temperature measurement.

samples of the DUT which show a maximum measured temperature deviation of ±1.4 °C at 80 °C.

The rejection of the drain current is shown in Fig. 8. In this measurement, a DC current is injected into the GIT drain, while the temperature is kept constant. The gate-source voltage shows a strong dependence of 19.5 mV A^{-1} while the sensed voltage shows virtually no change with approximately −138 µV A^{-1} which corresponds to a reduction of 93 %. This translates to an error of −0.4 °C A^{-1}.

Online junction temperature measurement is demonstrated in a 50 V to 180 V boost converter as shown in the measurement presented in Fig. 9. The transistor gate is initially charged with a current dictated by the AGD. During this phase, switching losses and electromagnetic interference can be balanced by changing the gate driver current. After the voltage transition of the GIT, the AGD turns off and leaves the hold driver to deliver the modulated hold current. Here the temperature sensor is employed for loss sensing. While changing the AGD's driver current from 192 mA to 96 mA, the temperature increases from 77.4 °C to 80.5 °C. This change is measured by the junction temperature monitor and is used in finding an optimal driver current.

V. Conclusion

An integrated junction temperature measurement circuit for GaN gate-injection transistors was presented. The circuit is based on a PTAT voltage generated from the GIT's gate, which is sampled during the transistor's on-state. The temperature sensing method can be used in online operation with minimal additional circuitry or power consumption due to the inherent hold current requirement of GITs, eliminating additional external circuity, decreasing system cost and increasing reliability.

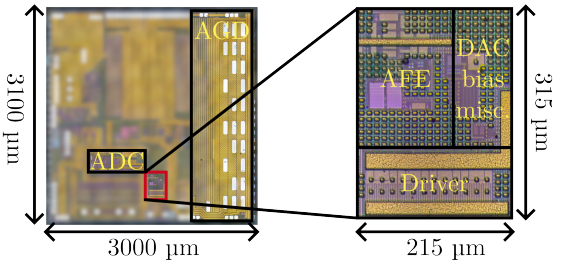

Fig. 10. Micrograph of ASIC and sense circuit.

Due to the differential sensing, the circuit shows a high level of robustness against process variations of the GIT transistor and the sensing circuit itself. Furthermore, drain current influences are almost fully suppressed. Measurements of multiple GIT samples show a low error of ±1.4 °C, eliminating the need for calibration of each individual GIT. The circuit achieves 260 mK resolution and requires an area of 0.068 mm^2.

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